mosaic

Mosaic Semiconductor Inc.

128K x 8 UV EPROM Monolithic

MUM8128W-17/20/25

Issue 2.1 : March 1989

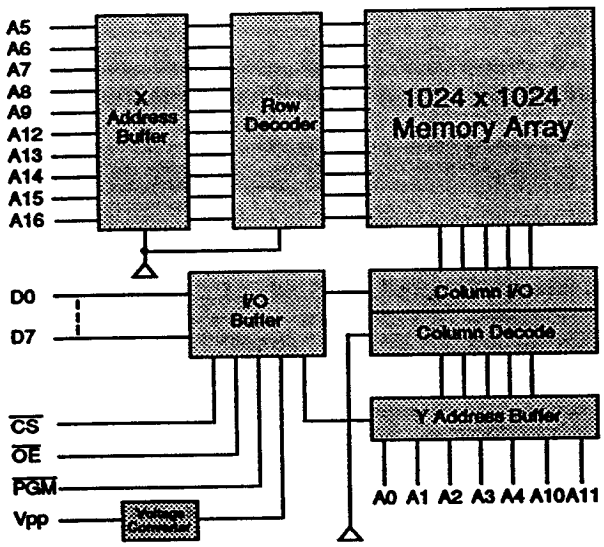
PRELIMINARY

131,072 x 8 CMOS High Speed UV EPROM

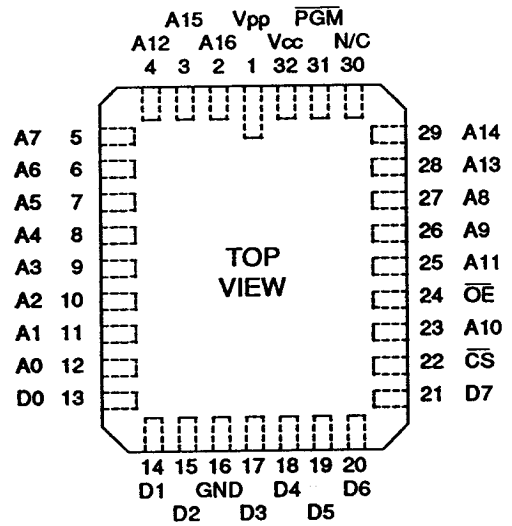
Features

Access Times of 170/200/250 ns
Vpp Program Voltage 12.5V
JEDEC 32 pad LCC Footprint and Pin-out
Low Power Operation 50mW (typ.)
Low Power Standby 5µW (typ.)
High Performance Programming Available, including Page Mode
Directly TTL compatible
May be Processed to MIL-STD-883C(suffix MB)

Block Diagram



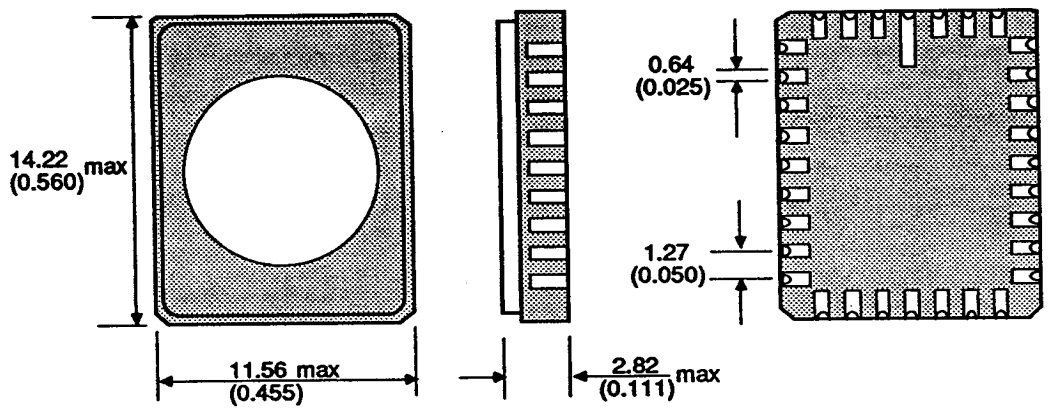
Pin Definitions



Pin Functions

A0-A16	Address Inputs
D0-D7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
Vpp	Programming Voltage
$\overline{PGM}$	Programming Enable
NC	No Connect
Vcc	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches)



Absolute Maximum Ratings (1)

Supply Voltage (2)	V_{CC}	-0.6 to +7	V
Programming Voltage	V_{PP}	-0.6 to +13	V
Input Voltage (2),(3)	V_{in}	-0.6 to +7	V
Operating Temperature	T_{opr}	-60 to +140	°C
Storage Temperature	T_{stg}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of The deviceat those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) Pulse Width:-1 v for 50ns
(3) With Respect to GND

Recommended Operating Conditions

		min	*typ*	*max*	
DC Logic Supply Voltage	V_{CC}	4.75	5.0	6.3	V
DC EPROM Program Voltage	V_{PP}	12.2	-	12.5	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+1	V
Input Low Voltage	V_{IL}	0.3	-	0.8	V
Operating Temperature(1)	T_a	0	-	70	°C
	T_{ai}	-40	-	85	°C (8128I)
	T_{am}	-55	-	125	°C (8128M,8128MB)

Note:(1) Programming would normally take place at 25°C

Operating Modes

The Table below show the logic inputs required to control the operating modes of the MUM8128W EPROM.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{PGM}$	*Vpp*	*Vcc*	*Outputs*
Read	0	0	1	5V	5V	Data out
Output Disable	0	1	1	5V	5V	Floating
Standby	1	X	X	5V	5V	Floating
Program	0	1	0	12.5V	6V	Data in
Program Verify	0	0	1	12.5V	6V	Data out
Page Data Latch	1	0	1	12.5V	6V	Data in
Page Program	1	1	0	12.5V	6V	Floating
Program Inhibit	0	0	0	12.5V	6V	Floating
	0	1	1	12.5V	6V	
	1	0	0	12.5V	6V	
	1	1	1	12.5V	6V	

1 = V_{ih}
0 = V_{il}
X = Don't Care

Device Identifier Mode

The Identifier Mode allows the reading out of binary codes, which identify manufacturer and type of device, from the outputs of this EPROM. By this mode, the device can be automatically matched to the correct programming algorithm using a suitable EPROM Programmer.

PINS / IDENTIFIER	$\overline{PGM}$	A9	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code	V_{ih}	12.0V	V_{il}	0	0	0	0	0	1	1	1	07
Device Code			V_{ih}	0	0	1	1	1	0	0	0	38

Note that pins A1 - A8, A10 - A16, $\overline{CS}$ and $\overline{OE}$ are all held at V_{il}

READ OPERATION

DC Electrical Characteristics (T_a=0 to±70°C,V_{CC}=5V±5%)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{in}	V_{in}=5.25V	-	-	2	µA
Output Leakage Current	I_{out}	V_{out}=5.25V	-	-	2	µA
V_{PP} Leakage Current	I_{PP}	V_{PP}=5V	-	1	20	µA
Standby Power	I_{sb1}	$\overline{CS}$ = V_{ih}	-	-	1	mA
Supply Current	I_{sb1}	$\overline{CS}$=V_{CC} ±0.3V, I_{out}=0mA	-	1	20	µA
Operating Power	I_{cc1}	f=1MHz, I_{out}=0mA	-	-	15	mA
Supply Current	I_{cc2}	f=5MHz, I_{out}=0mA	-	-	30	mA
Input Low Voltage	V_{il}	Note (1)	-0.3	-	0.8	V
Input High Voltage	V_{ih}	Note (2)	2.0	-	V_{CC}+1	V
Output LowVoltage	V_{ol}	I_{ol}=2.1mA	-	-	0.4	V
Output HighVoltage	V_{oh}	I_{oh}=-400µA	3.7	-	-	V

Notes (1) -1.0V for pulse width ≤ 50 ns
(2) Vcc+1.5V for pulse width ≤20 ns. If V_{ih} is over the specified max. value, READ operation cannot be guaranteed.

Capacitance (T_a=25°C,f=1MHz)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{in}	V_{in}=0V	-	10	pF
Output Capacitance:	C_{out}	V_{out}=0V	-	15	pF

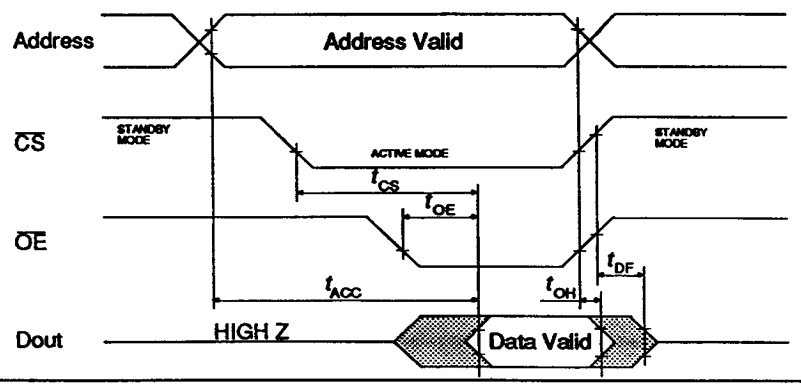
AC Timing Characteristics

		-17		*-20*		*-25*		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Address to Output Delay	t_{ACC}	-	170	-	200	-	250	ns
$\overline{CS}$ to Output Delay	t_{CS}	-	170	-	200	-	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	10	70	10	70	10	100	ns
$\overline{OE}$ or $\overline{CS}$ High to Output Float	t_{DF}	0	50	0	50	0	60	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ (whichever occurred first)	t_{OH}	0	-	0	-	0	-	ns

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V.
* Input rise and fall times: ≤ 20ns.
* Input and Output timing reference levels: 0.8V and 2.0V.
* Output load : 1 TTL gate plus 100 pF.

Read Cycle Timing Waveform



PROGRAMMING OPERATION

DC Electrical Characteristics (T_a= 25°C ±5°C, V_{CC}= 6V±0.25V, V_{PP} = 12.5V ±0.3V)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{in}	V_{in}=5.25V	-	-	2	µA
Operating Power Supply Current	I_{cc}		-	-	30	mA
V_{PP} Supply Current	I_{PP1}	Single Byte Programming	-	-	40	mA
	I_{PP2}	Page Mode Programming	-	-	50	mA
Input Low Voltage	V_{il}	Note (5)	-0.1	-	0.8	V
Input High Voltage	V_{ih}	Note (6)	2.2	-	V_{CC}+0.5	V
Output LowVoltage (Verify)	V_{ol}	I_{ol}=2.1mA	-	-	0.45	V
Output HighVoltage (Verify)	V_{oh}	I_{oh}=-400µA	2.4	-	-	V

Notes (1) V_{CC} must be applied before V_{PP} and removed after V_{PP}.
(2) V_{PP} must not exceed 13V including overshoot.
(3) Device reliability may be affected if device is installed or removed while V_{PP}= 12.5V
(4) The transitions Vil to 12.5V or 12.5V to V_{il} are not allowed while CS = Low.
(5) -0.6V for pulse width ≤ 20 ns.
(6) If V_{ih} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics

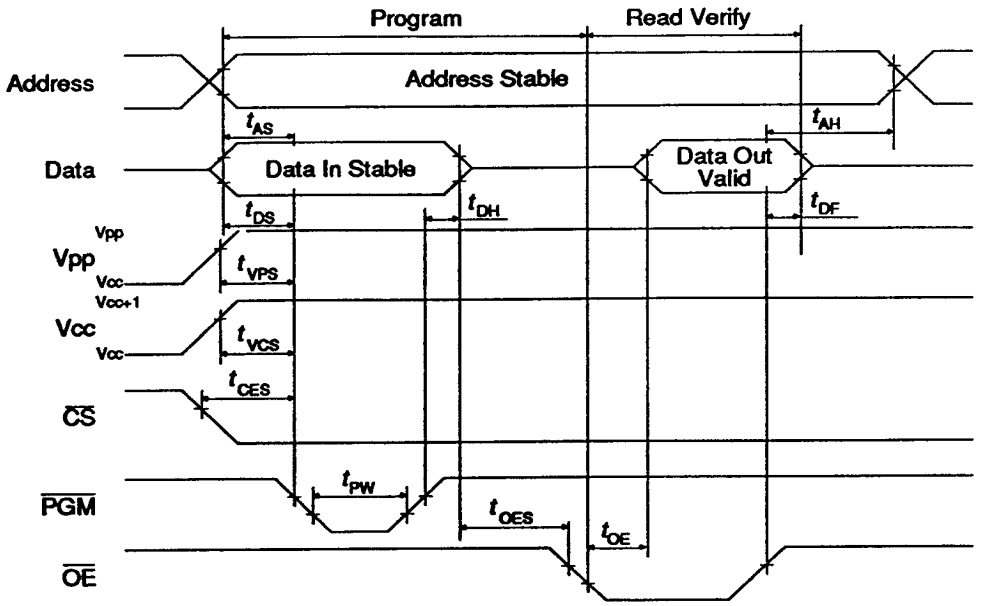
Parameter		*Symbol*	*min*	*typ*	*max*	*Unit*
Address Setup Time		t_{AS}	2	-	-	µs
OE Setup Time		t_{OES}	2	-	-	µs
OE Hold Time		t_{OEH}	2	-	-	µs
Data Setup Time		t_{DS}	2	-	-	µs
Address Hold Time		t_{AH}	0	-	-	µs
		t_{AHL}	2	-	-	µs
Data Hold Time		t_{DH}	2	-	-	µs
OE High to Output Float Delay	(1)	t_{DF}	0	-	130	ns
Vpp Setup Time		t_{VPS}	2	-	-	µs
Vcc Setup Time		t_{VCS}	2	-	-	µs
PGM Initial Program Pulse Width	(2)	t_{PW}	0.19	0.2	0.21	ms
PGM Overprogram Pulse Width	(3)	t_{OPW}	0.19	-	5.25	ms
Data Valid from OE		t_{OE}	0	-	150	ns
OE Pulse Rise Time During Programming		t_{PRT}	50	-	-	ns
PGM Setup Time		t_{PGMS}	2	-	-	µs
CS Setup Time		t_{CES}	2	-	-	µs
CS Hold Time		t_{CSH}	2	-	-	µs
OE Pulse Width during Data Latch		t_{LW}	1	-	-	µs

Notes (1) Defines the time at which the output achieves the open circuit condition and is no longer driven.
(2) Initial program pulse width tolerance is 0.2 ms± 5%.
(3) Length of this pulse may vary as a function of the iteration counter value n.

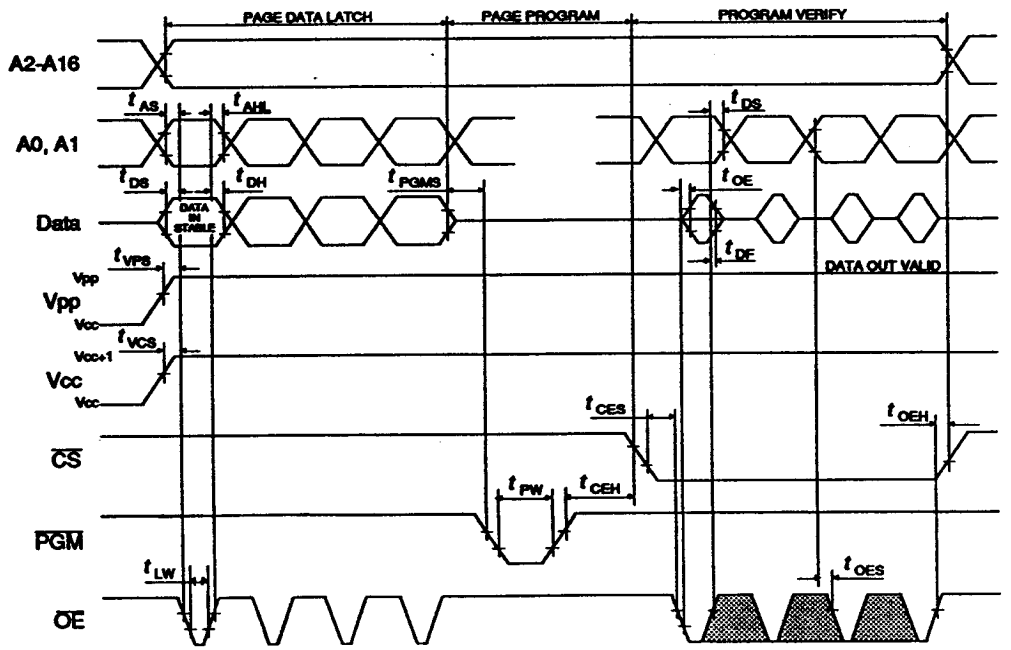
AC Test Conditions

* Input pulse levels: 0.45V to 2.4V
* Input rise and fall times: ≤ 20ns
* Input and Output timing reference levels: 0.8V and 2.0V

Single Byte Programming



Page Mode Programming

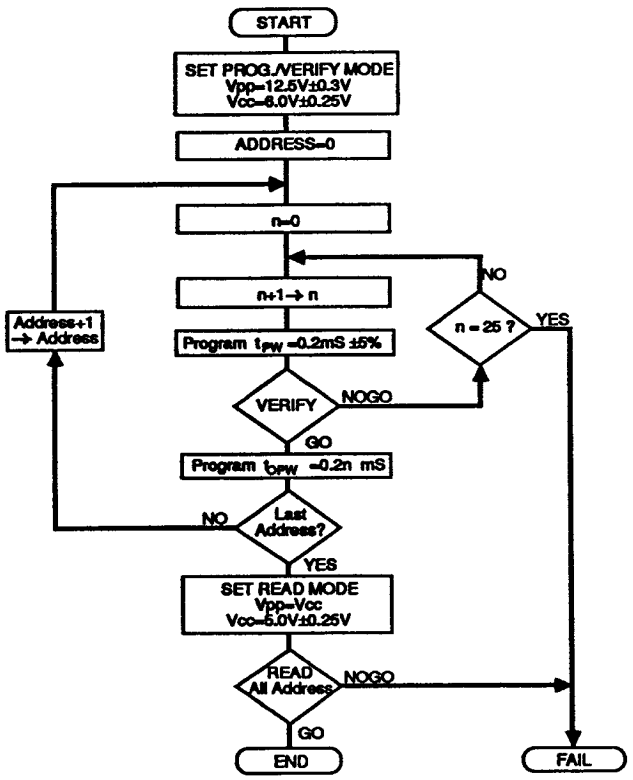


HIGH PERFORMANCE PROGRAMMING ALGORITHMS

The MUM8128W can be programmed using either of the alogorithms shown below. These allow faster programming times without stressing the device or causing deterioration in Data Retention Time. Two methods are described below, Single Byte and Page Mode, the selection of which are shown in the Truth Table on page 2.

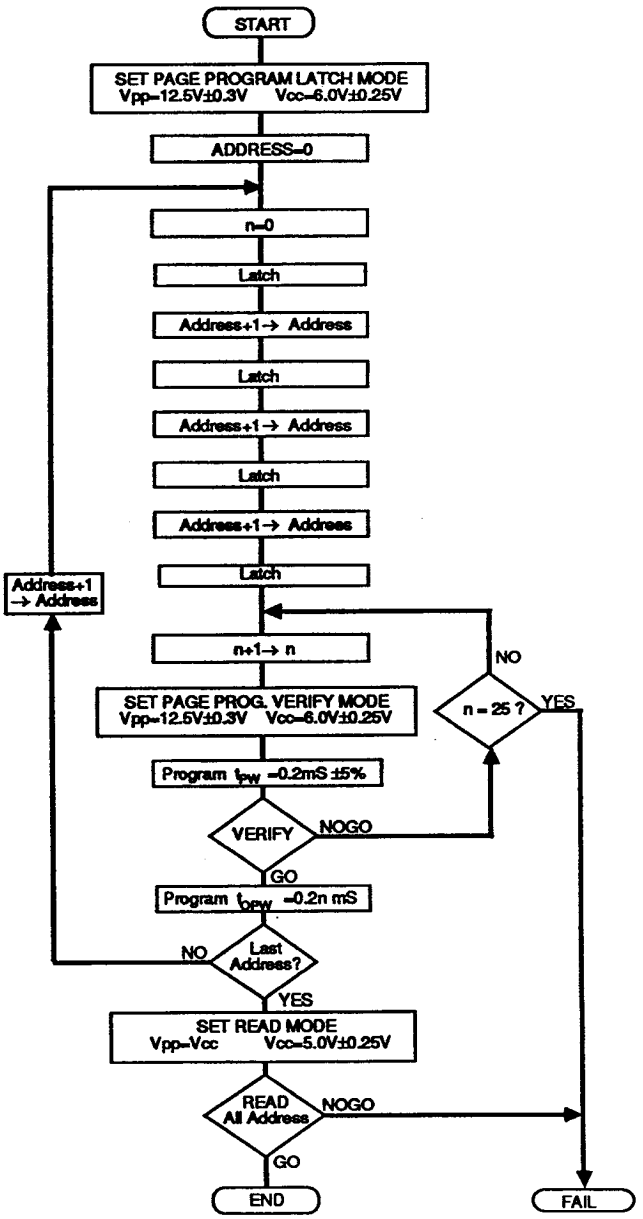
Single Byte

When the Program logic conditions are satisfied, the location is designated by A0 - A16, and the data to be programmed is applied 8 bits in parallel on D0 - D7. In this state, Byte programming is completed when $\overline{PGM}$ is at a low level.



Page Mode

Page Mode allows 4 bytes of data to be simultaneously programmed. The destination address for a Page Programming operation must reside on the same page i.e. A2 - A16 must not change. When the logic conditions in the Truth Table are satisfied, Page Mode Programming is activated. The four locations in the same page are designated by A0 - A1, and the data is applied in parallel on D0 - D7. In this state the data latch (4 bytes) is completed, and the data is programmed when $\overline{OE}$ is high. Programming is completed when $\overline{PGM}$ is low.

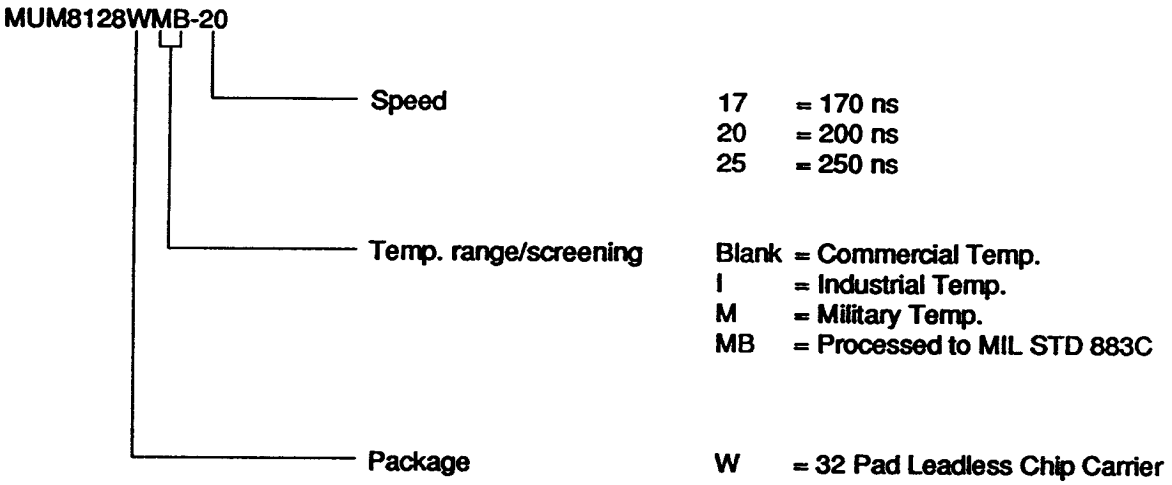


ERASE

Erasure of the MUM8128 is performed by exposure to ultraviolet light of 2537 Å at a minimum intensity of 15WS/cm², for approximately 15 - 20 minutes.

Note that sunlight and flourescent light may contain sufficient ultraviolet light to erase the programmed information. For this reason, and anyway for any operation in the READ mode, the transparent lid of this device should be covered with an opaque label.

Ordering Information



Military Screening Procedure

Component Screening Flow for high reliability product is in accordance with Mil-883C method 5004 and is detailed below:

MB COMPONENT SCREENING FLOW

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
High-temperature storage	1008 Condition C (24hrs @ +150°C)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at Ta=+25°C	100%
Burn-in	Method 1015,Condition D,Ta=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at Ta=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

mosaic
Mosaic Semiconductor Inc.

7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
FAX: (619) 271 6058