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OKI semiconductor

OKI SEMICONDUCTOR GROUP

MSM6368

T-52-13-07

DOT MATRIX 80 DOT COMMON DRIVER

GENERAL DESCRIPTION

The OKI MSM6368GS is a dot matrix LCD's common driver LSI, which is fabricated by low power CMOS silicon gate technology. This LSI consists of an 80-bit bidirectional shift register, 80-bit level shifter and an 80-bit 4-level driver. This LSI has 80 output pads to be connected to the LCD. By connecting more than two MSM6368GS in series, this LSI is applicable to a wide LCD panel.

This LSI can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from an external source.

FEATURES

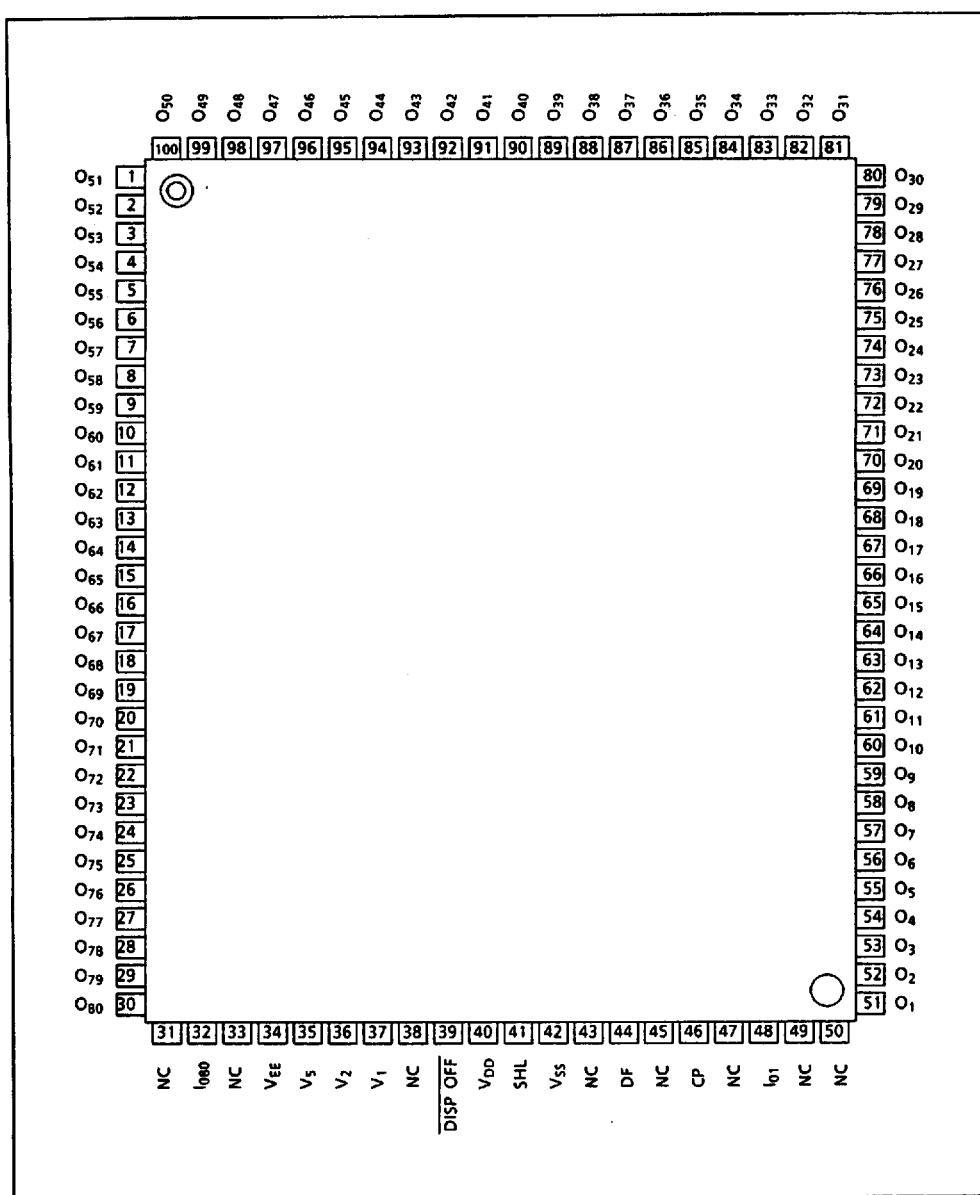
- Supply voltage : 4.5~5.5V
- LCD driving voltage : 20~40V
- Applicable LCD duty : 1/200~1/480
- LCD output : 80
- Bias voltage can be supplied externally.
- 100 pin Plastic QFP (QFP100-P-1420-K)

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PIN CONFIGURATION

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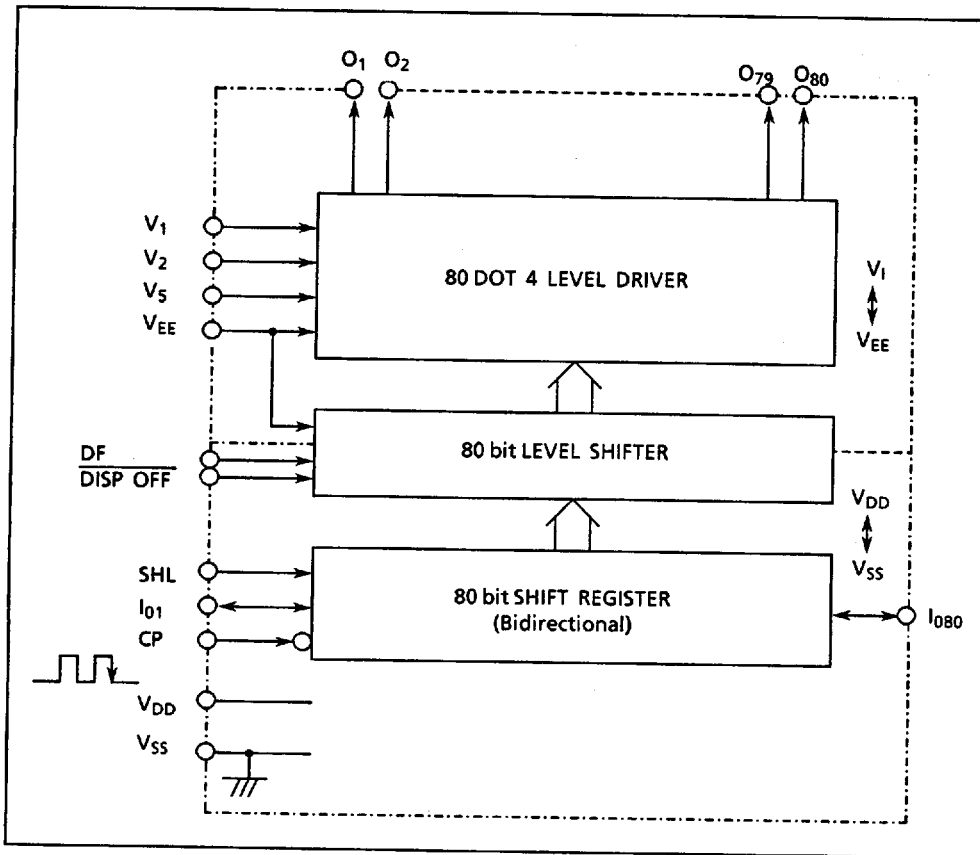


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FUNCTIONAL BLOCK DIAGRAM

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TRUTH TABLE

DF	LATCH DATA	DISP OFF	DRIVER OUT (O ₁ ~O ₈₀)
L	L	H	V ₂
L	H	H	V _{EE}
H	L	H	V ₅
H	H	H	V ₁
X	X	L	V ₁

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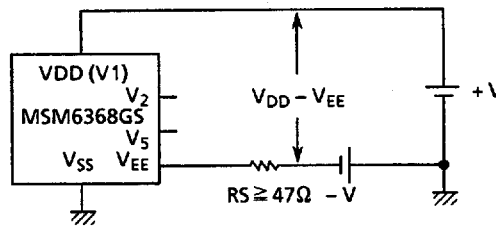
ABSOLUTE MAXIMUM RATINGS

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Parameter	Symbol	Condition	Ratings	Unit
Supply Voltage (1)	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3~	V
Supply Voltage (2)	$V_{DD} - V_{EE} *1$	$T_a = 25^\circ\text{C}$	0~40	V
	$V_{DD} - V_{EE} *2$	$T_a = 25^\circ\text{C}$	0~42	
Input Voltage	V_I	$T_a = 25^\circ\text{C}$	-0.3~ $V_{DD} + 0.3$	V
Storage Temperature	T_{stg}	-	-55~+150	$^\circ\text{C}$

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leq V_{DD}$

*2 In case of connecting Resistor ($R_S \geq 47\Omega$) at V_{EE} PIN

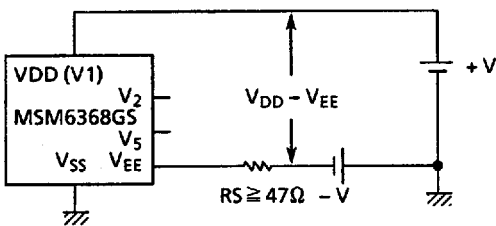


OPERATING RANGE

Parameter	Symbol	Condition	Ratings	Unit
Supply Voltage (1)	V_{DD}	-	4.5~5.5	V
Supply Voltage (2)	$V_{DD} - V_{EE} *1$	-	20~38	V
	$V_{DD} - V_{EE} *2$	-	20~40	
Operating Temperature	T_{op}	-	-20~+75	$^\circ\text{C}$

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leq V_{DD}$

*2 In case of connecting Resistor ($R_S \geq 47\Omega$) at V_{EE} PIN



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DC CHARACTERISTICS

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($V_{DD} = 5V \pm 10\%$ $T_a = -20 \sim +75^\circ C$)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input Voltage	$V_{IH} *1$	-	$0.8V_{DD}$	-	-	V
"L" Input Voltage	$V_{IL} *1$	-	-	-	$0.2V_{DD}$	V
"H" Input Current	$I_{IH} *1$	$V_{IH} = V_{DD}$ $V_{DD} = 5.5V$	-	-	1	μA
"L" Input Current	$I_{IL} *1$	$V_{IL} = 0V$ $V_{DD} = 5.5V$	-	-	-1	μA
"H" Output	$V_{OH} *2$	$I_O = -0.4 mA$ $V_{DD} = 4.5V$	$V_{DD} - 0.4$	-	-	V
"L" Output Voltage	$V_{OL} *2$	$I_O = 0.4 mA$ $V_{DD} = 4.5V$	-	-	0.4	V
ON Resistance	$R_{ON} *4$	$V_{DD} - V_{EE} = 35V$ $ V_N - V_{O1} = 0.25V$ $V_{DD} = 4.5V$ $*3$	-	-	0.5	$k\Omega$
Power Consumption Current	I_{DD}	CP = 28KHz $V_{DD} - V_{EE} = 35V$ No Load	-	-	100	μA
Input Capacitance	C_i	f = 1MHz	-	5	-	pF

*1 Applicable to CP, I_{01} , I_{080} , SHL, DF, DISP OFF terminals.

*2 Applicable to I_{01} , I_{080} terminals.

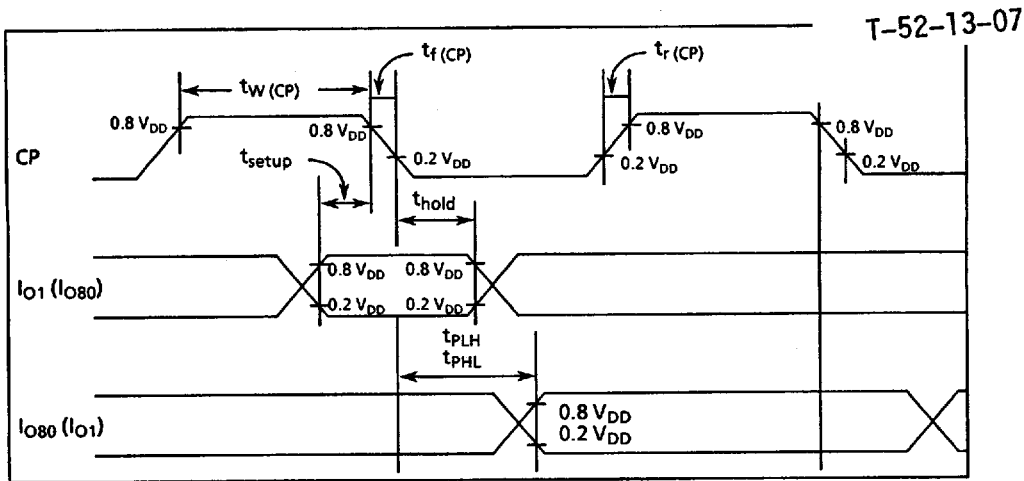
*3 $V_N = V_{DD} \sim V_{EE}$, $V_2 = \frac{1}{21} (V_{DD} - V_{EE})$, $V_5 = \frac{20}{21} (V_{DD} - V_{EE})$, $V_{DD} = V_1$

*4 Applicable to $O_1 \sim O_{80}$ terminals.

AC CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$ $T_a = -20 \sim +75^\circ C$ $C_L = 15pF$)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H", "L" propagation delay time	t_{PLH} t_{PHL}	-	-	-	250	ns
Maximum clock frequency	f_{CP}	-	1	-	-	MHz
CP pulse width	$t_W (CP)$	-	63	-	-	ns
Data set up time $I_{01} (I_{080}) \rightarrow CP$	t_{setup}	-	100	-	-	ns
Data hold time $I_{01} (I_{080}) \rightarrow CP$	t_{hold}	-	100	-	-	ns
CP rising/falling time	$t_r (CP)$ $t_f (CP)$	-	-	-	50	ns



PIN DESCRIPTION

- **IO1, IO80, SHL**

These are I/O pins of the 80-bit bidirectional shift register. The shift direction can be selected by the SHL pin. Table 1 gives functions of IO1, IO80, and SHL.

Table 1

SHLa	Shift direction	IO1/IO80	Input, output	Function
L	O ₁ →O ₈₀	IO1	Input	This is a scan data input pin of the shift register, I which inputs data in synchronization with a clock pulse. See Note 1.
		IO80	Output	This is an output pin of the shift register, which outputs data in synchronization with a clock pulse behind the number of bits (80) of the scan data, which is input from the IO1 pin. For cascade connection, see the application note.
H	O ₈₀ →O ₁	IO80	Input	This is a scan data input pin of the shift register, I which inputs data in synchronization with a clock pulse. See Note 1.
		IO1	Output	This is an output pin of the shift register, which outputs data in synchronization with a clock pulse behind the number of bits (80) of the scan data, which is input from the IO81 pin. For cascade connection, see the application note.

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Note 1: Table 2 gives the relation between scan data (I_{O1} , I_{O80}) and liquid crystal drive output (O_1 to O_{80}).

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Table 2

I_{O1} , I_{O80}	Liquid crystal drive output
"H"	Selection level (V_1 , V_{EE})
"L"	Non-Selection level (V_2 , V_5)

DESCRIPTION OF PINS

- **CP**

Scan data is shifted at the trailing edge of a clock pulse of the 80-bit bidirectional shift register.

- **DF**

This is an input pin for a liquid crystal drive waveform AC synchronization signal, which generally inputs a frame inversion signal.

- **V_{DD} , V_{SS}**

These are power pins of this IC. The V_{DD} pin is generally set to 4.5 to 5.5V. V_{SS} is a grounding pin, which is generally set to 0V.

- **$\overline{\text{DISP OFF}}$**

These are input pins to control the output pins O_1 to O_{80} . During low signal input, signals on the V1 level are output from the output pins O_1 to O_{80} . See the truth table.

- **V_1 , V_2 , V_5 , V_{EE}**

These are liquid crystal drive bias voltage pins. Bias voltages by resistance division are generally used. Fig. 1 shows an example of supply of liquid crystal drive bias voltages by resistance division. The V_1 pin may be separated from the V_{DD} pin.

Note when turning power on and off

The liquid crystal drive on this IC chip requires a high voltage. When a high voltage is applied to it with the logic power supply floated, an overcurrent flows. This may damage the IC chip. Be sure to carry out the following power-on and power-off sequences:

When turning power on:

First V_{DD} ON, next V_{EE} , V_5 , V_2 , V_1 ON. Or both at the same time.

When turning power off:

First V_{EE} , V_5 , V_2 , V_1 OFF, next V_{DD} OFF. Or both at the same time.

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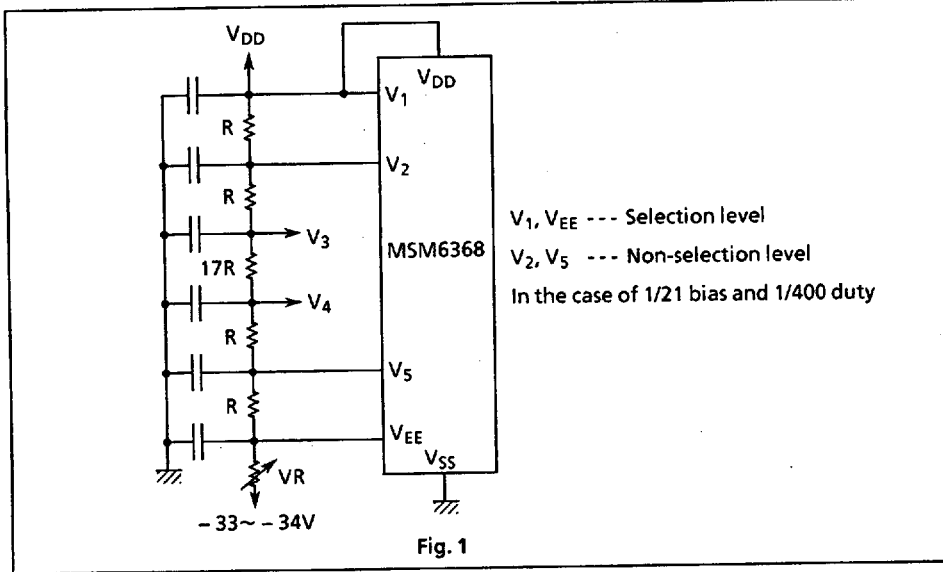
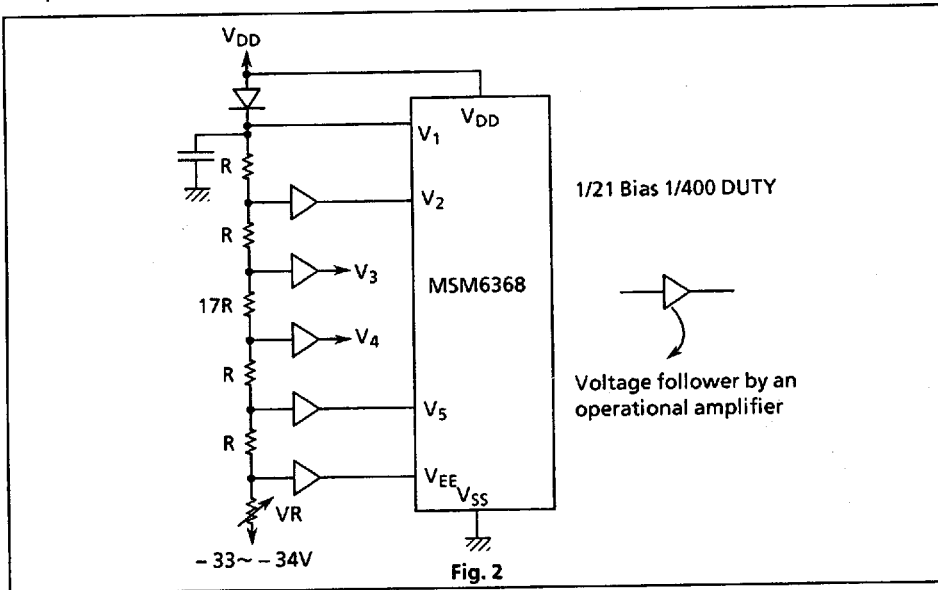


Fig. 2 shows an example of supply of bias voltages using an operational amplifier. the use of an operational amplifier reduces the bias impedance and the supply current.



● O_1 to O_{80}

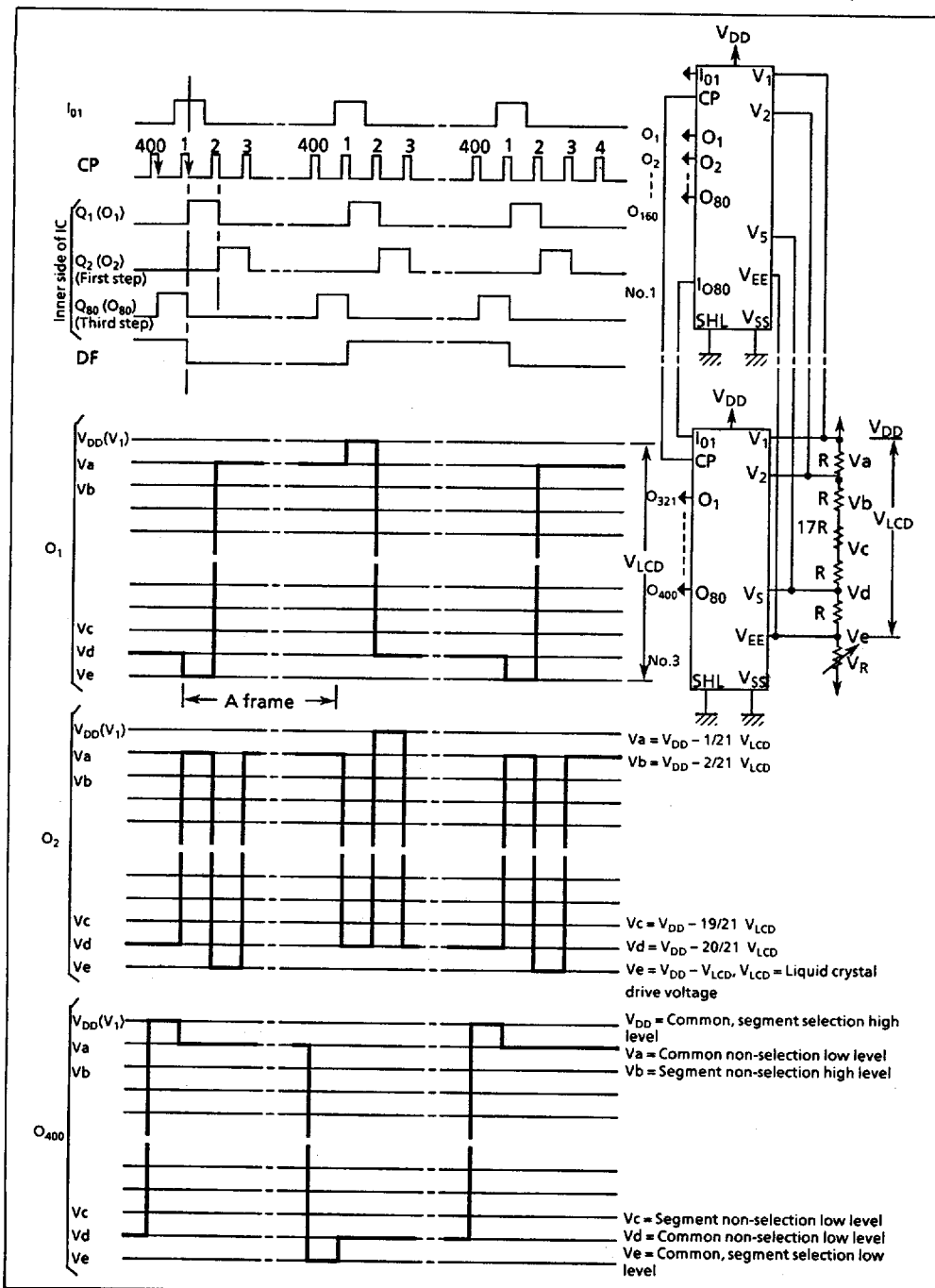
These are output pins of the 4-level driver of this IC, which correspond directly to the bits of the shift register. One of the four levels $V_1, V_3, V_5,$ and V_{EE} is selected and output by a combination of the data in shift register and a DF signal. See the truth table. Connect the output pins to the liquid crystal panel on the common side.

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TIMING CHART (1/400 duty, 1/21 bias)

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APPLICATION NOTE

