

### General Description

The LDS105P is a low cost secondary control circuit for low power applications needing constant voltage and constant current control. It implements a simple single-loop control by modifying the internal reference level as a function of current above the current limit threshold. The current loop reduces the reference by 40 mV per mV change at the current sense input. The error amp provides high gain and bandwidth under low voltage operation.

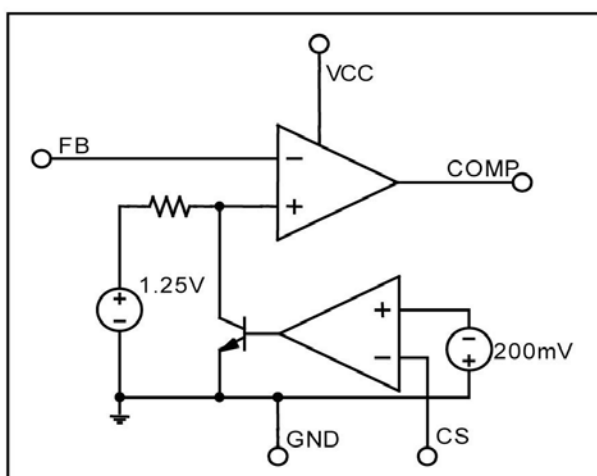
### Applications

- Offline Battery Chargers
- Constant V/ Constant I supplies

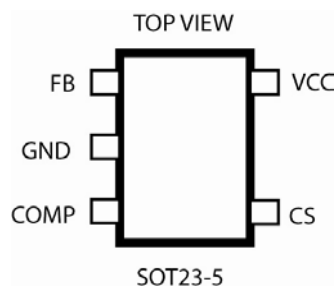
### Features

- 1.25V reference
- 200mV current limit threshold
- Error amp output swings near ground for low voltage operation
- High PSRR and line regulation
- Low current consumption
- Open collector output
- Low voltage operation 2.2V
- 10mA current sink
- 50 ppm/°C typical temperature deviation
- **RoHS compliant** available

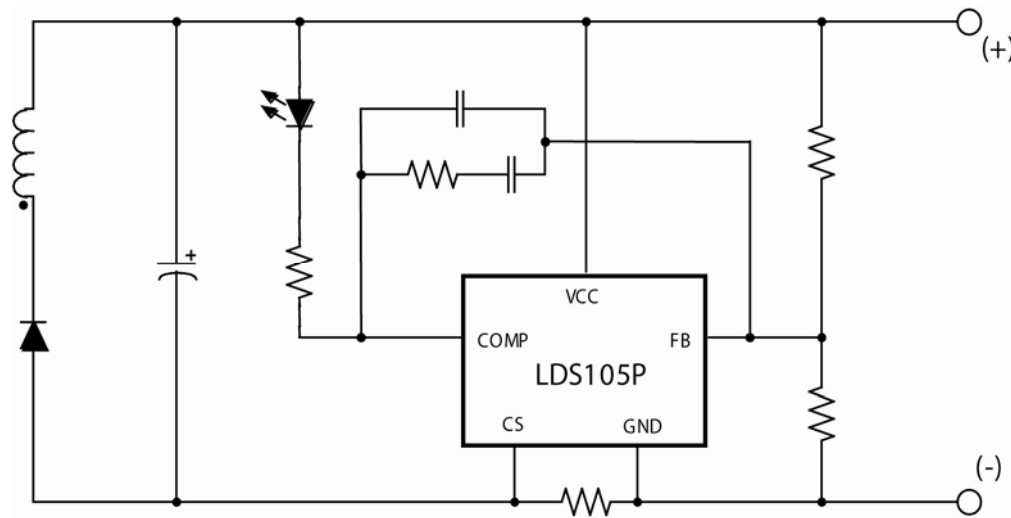
### Block Diagram



### Pin Configuration



## Typical Application



## Pin Descriptions

Pin	Pin Name	Function
1	VCC	Positive supply
2	GND	Ground
3	COMP	Output of error amplifier; 10 mA source/sink capability
4	FB	Inverting input to error amplifier; will have threshold of 1.25V.
5	CS	Current sense input

## Absolute Maximum Ratings

Parameter	Value	Units
V <sub>CC</sub> Voltage	20	V
COMP Voltage	20	V
REF Voltage	20	V
CS Voltage (Self limiting diodes)	±1	V
VCC, COMP, REF, CS Current	50	mA
Operating Junction Temperature	150	°C
Lead Temperature (soldering 10 seconds)	260	°C
Storage Temperature Range	-65 to +150	°C
ESD Rating (HBM)	2	KV

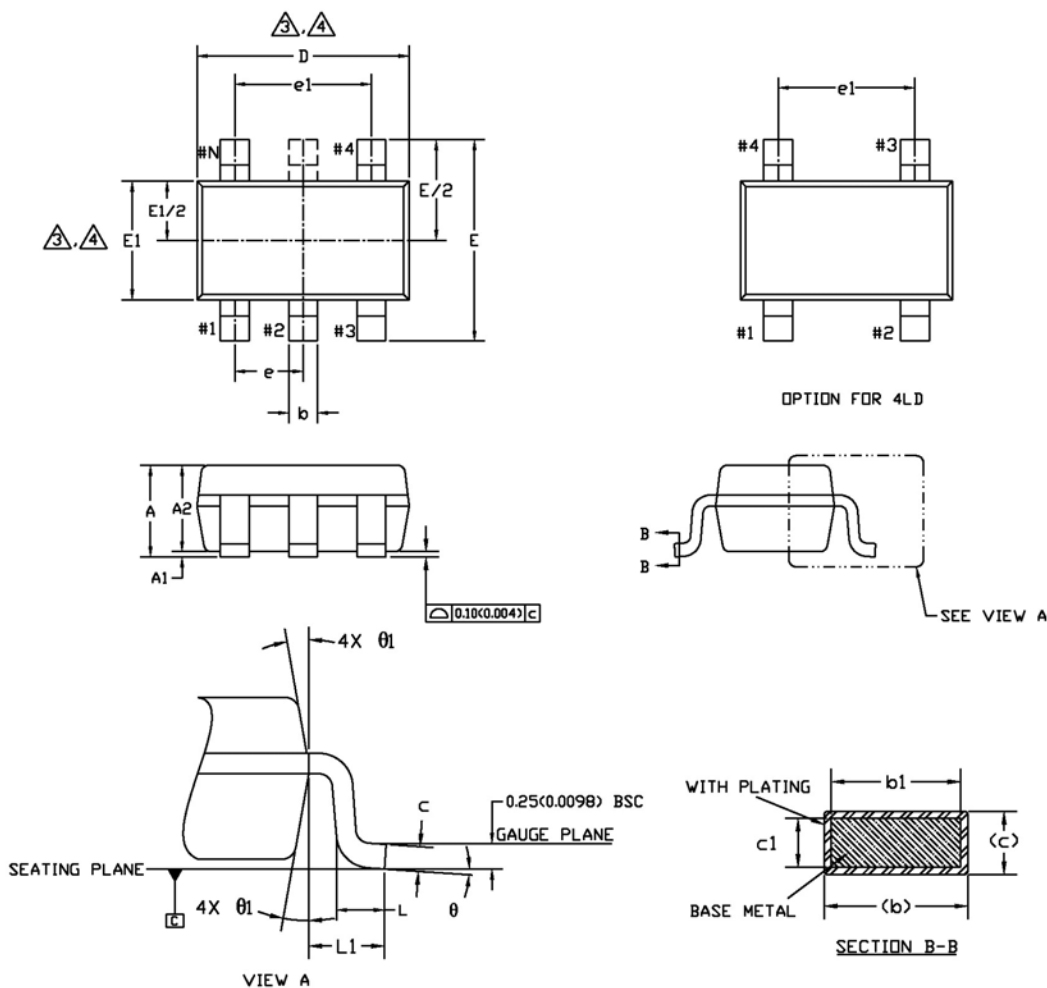
## Electrical Specifications

Electrical characteristics are guaranteed over the full temperature range  $-20^{\circ}\text{C} < T_j < 105^{\circ}\text{C}$ . Ambient temperature must be de-rated based upon power dissipation and package thermal characteristics. Unless otherwise stated, test conditions are  $V_{CC} = 3\text{V}$ ,  $V_{COMP} = V_{FB}$ ,  $I_{COMP} = 1\text{mA}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vcc	Supply Voltage		2.2		18	V
Icc	Quiescent Supply Current	$V_{COMP}=1\text{V}$ $V_{CC}=15\text{V}$		0.2	0.5	mA
Vref	Reference Voltage	$T_a=25^{\circ}\text{C}$	1.238	1.250	1.263	V
DVcc	Line regulation	$V_{CC}=2.5\text{V}$ to $V_{CC}=18\text{V}$		0.2	1	mV
DVload	Load Regulation	$I_{COMP}=1\text{mA}$ to $5\text{mA}$		1	2	mV
Tcref	Reference Temperature Deviation	$-20^{\circ}\text{C} < T_j < 105^{\circ}\text{C}$		0.5	1	%
IFB	REF input current		-500		500	nA
PSRR	Power Supply Rejection	Freq.=300KHz		40		dB
Av	Error Amplifier Open Loop Gain	$I_{COMP}=2\text{mA}$ , $COMP=1\text{V}$		80		dB
BW	Unity Gain Frequency	$I_{COMP}=2\text{mA}$ , $COMP=1\text{V}$		2.5		MHz
VCOMP	Output Saturation Voltage	$I_{COMP}=10\text{mA}$ , $V_{FB}=HIGH$		200	250	mV
TRANSC	Output Transconductance	$I_{COMP}=1\text{mA}$ to $20\text{mA}$		2.5		mA/mV
Ileak	Output Leakage Current	$V_{COMP}=16$ $V_{FB}=0$		200	400	nA
Vcs	Current sense threshold voltage	$T_j=25^{\circ}\text{C}$	197		203	mV
		$-20 < T_j < 105^{\circ}\text{C}$	195		205	
Gain	Current sense gain to reference	$-20 < T_j < 105^{\circ}\text{C}$	36	40	44	mV/mV
Ics	Bias current	$V_{cs}=-200\text{ mV}$		150		$\mu\text{A}$
		$V_{cs}=-250\text{ mV}$		220		

## Package Dimensions

## SOT23-3, SOT23-4, SOT23-5, SOT23-6



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.20	1.30	1.40	0.047	0.051	0.055
A1	0.05	-	0.15	0.002	-	0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.35	-	0.50	0.013	-	0.020
b1	0.35	0.40	0.45	0.013	0.015	0.017
c	0.08	-	0.22	0.003	-	0.008
c1	0.08	0.13	0.20	0.003	0.005	0.007
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.062 BSC		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.074 BSC		
L	0.35	0.45	0.55	0.013	0.017	0.021
L1	0.60 REF.			0.023 REF.		
θ	0°	4°	8°	0°	4°	8°
θ1	10° TYP			10° TYP		

## NOTE :

1. Dimensioning and tolerancing per ASME Y 14.5 M - 1994.
2. Dimensions are in millimeters. Converted inch dimension are not necessarily exact.
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.15 mm per side. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
4. Top package may be smaller than the bottom package. Dimension D and E1 are determine at the outermost extremes of the plastic body exclusive of mold flash gate burrs and interlead flash.
5. Terminal numbers are shown for reference only. Die is facing up for molding. Die is facing down for trim/form.

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## Ordering Information

Device	Operating Tj	%Tol	Pkg Type	VOUT	Wrap	Ordering Number
LDS105P	-20C° ≤ 105C°	1.0	SOT-23-5	1.25V	T&R	LDS105DY-M5-12-TL

Note: Lead Free and RoHS compliant.

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