2M × 36-Bit Dynamic RAM Module — HYM 362120GS-60/-70/-80

Advanced Information

- 2 097 152 words by 36-bit organization (alternative 4 194 304 words by 18-bit)
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
  80 ns access time
  150 ns cycle time (-80 version)
- Fast page mode capability with
  45 ns cycle time (-60/-70 version)
  50 ns cycle time (-80 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 6952 mW active (-60 version)
  max. 6292 mW active (-70 version)
  max. 5632 mW active (-80 version)
  CMOS – 132 mW standby
  TTL – 264 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  $\overline{\text{RAS}}$-only-refresh
  Hidden-refresh
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72-1250)
- Utilizes eight 1M × 1-DRAMs and sixteen 1M × 4 DRAMs in 300 mil SOJ packages
- 1024 refresh cycles / 16 ms
- Gold plated contact pads

The HYM 362120GS-60/-70/-80 is a 72 Mbyte RAM module organized as 2 097 152 words by 36-bit in a 72-pin single-in-line package comprising eight HYB 511000BJ 1M × 1 DRAMs and sixteen HYB 514400AJ 1M × 4 DRAMs in 300 mil wide SOJ-packages mounted together with twelve 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 362120GS-60/-70/-80 can also be used as a 4 194 304 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively.

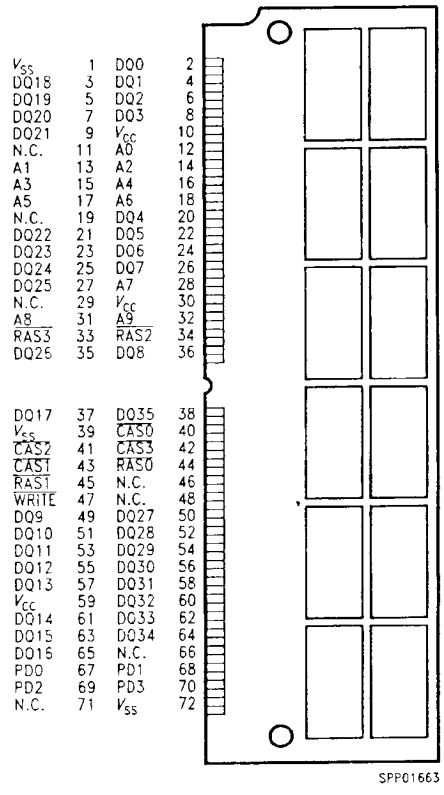
Each HYB 511000BJ and HYB 514400AJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 362120GS-60/-70/-80 dictates the use of early write cycles to prevent contention on D and Q.

Ordering Information

Type	Ordering Code	Package	Description
HYM 362120GS-60	on request	L-SIM-72-1250	DRAM Module (access time 60 ns)
HYM 362120GS-70	Q67100-Q645	L-SIM-72-1250	DRAM Module (access time 70 ns)
HYM 362120GS-80	Q67100-Q646	L-SIM-72-1250	DRAM Module (access time 80 ns)



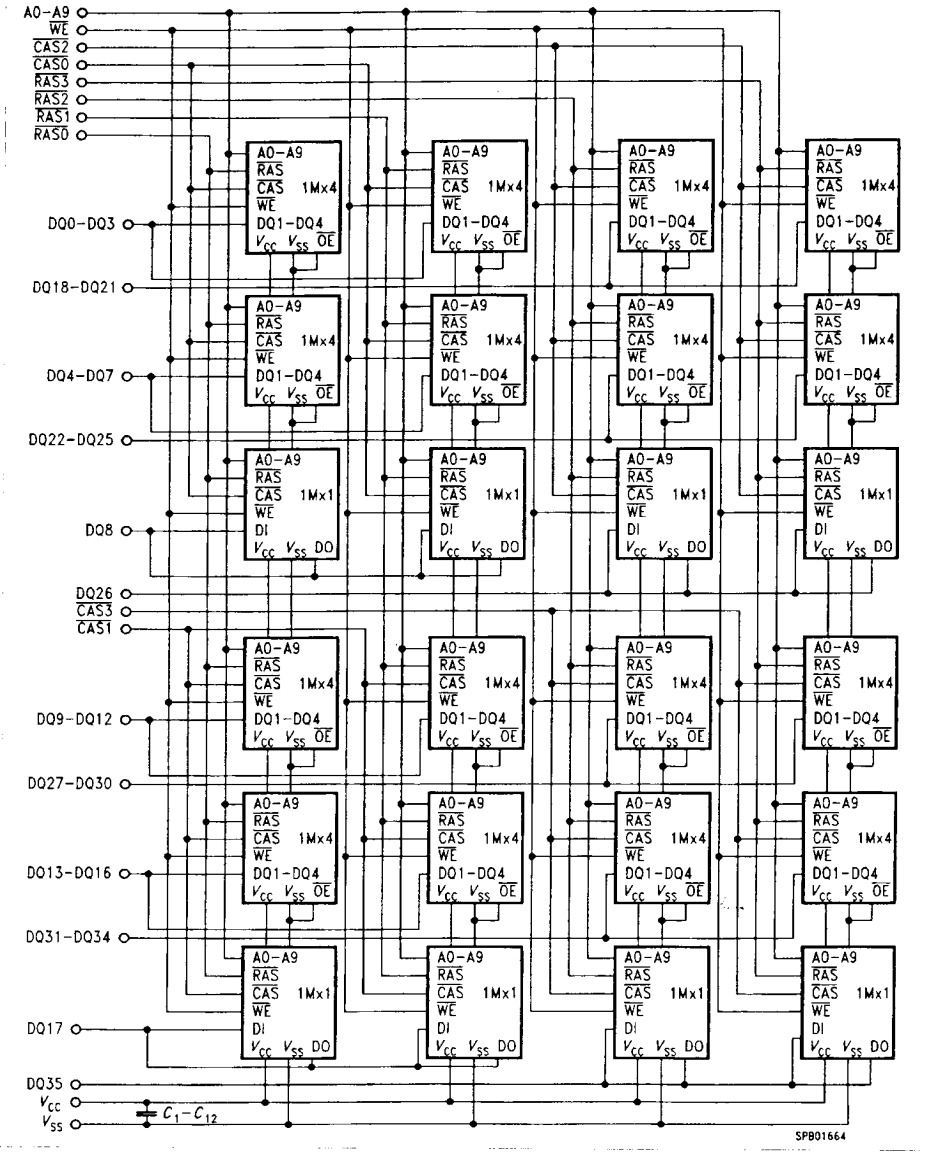
Pin Configuration

Pin Names

A0-A9	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60	-70	-80
PD0	N.C.	N.C.	N.C.
PD1	N.C.	N.C.	N.C.
PD2	N.C.	V_{SS}	N.C.
PD3	N.C.	N.C.	V_{SS}



Block Diagram

Absolute Maximum Ratings

Operation temperature range	0 to + 70 °C
Storage temperature range	– 55 to 125 °C
Soldering temperature	260 °C
Soldering time	10 s
Input/output voltage	– 1 to + 7 V
Power supply voltage	– 1 to + 7 V
Power dissipation	8.9 W
Data out current (short circuit)	50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics[1)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	5.5	V	
Input low voltage	V_{IL}	– 1.0	0.8	V	
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 20	20	µA	
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min)	I_{CC1}				
HYM 362120GS-60		–	1264	mA	2),
HYM 362120GS-70		–	1144	mA	3)
HYM 362120GS-80		–	1024	mA	
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	48	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	I_{CC3}				
HYM 362120GS-60		–	1264	mA	2)
HYM 362120GS-70		–	1144	mA	
HYM 362120GS-80		–	1024	mA	

Notes see page 201.

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, address cycling, $t_{PC} = t_{PC}$ min)	I_{CC4}				
HYM 362120GS-60		–	864	mA	[2], [3]
HYM 362120GS-70		–	744	mA	
HYM 362120GS-80		–	624	mA	
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V)	I_{CC5}	–	24	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min)	I_{CC6}				
HYM 362120GS-60		–	1264	mA	[2]
HYM 362120GS-70		–	1144	mA	
HYM 362120GS-80		–	1024	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9, $\overline{WE}$)	C_{I1}	–	160	pF
Input capacitance ($\overline{RAS0}$-$\overline{RAS2}$, $\overline{CAS0}$-$\overline{CAS3}$)	C_{I2}	–	42	pF
I/O capacitance (DQ0-DQ7, DQ9-DQ16, DQ18-DQ25, DQ27-DQ34)	C_{IO1}	–	29	pF
I/O capacitance (DQ8, DQ17, DQ26, DQ35)	C_{IO2}	–	39	pF

Notes see page 201.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		HYM 362120GS-60		HYM 362120GS-70		HYM 362120GS-80		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	150	–	ns
Fast page mode cycle time	t_{PC}	45	–	45	–	50	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	–	80	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	20	–	20	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	–	40	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	40	–	40	–	45	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	60	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	80	200000	ns
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	80	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	40	20	50	20	60	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	15	40	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address hold time ref. to $\overline{RAS}$	t_{AR}	50	–	55	–	60	–	ns

Notes see page 201.

AC Characteristics[4) 5)] (cont'd)
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter		Symbol	Limit Values						Unit
			HYM 362120GS-60		HYM 362120GS-70		HYM 362120GS-80		
			min.	max.	min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time		t_{RAL}	30	–	35	–	40	–	ns
Read command setup time		t_{RCS}	0	–	0	–	0	–	ns
Read command hold time	8)	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$	8)	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time		t_{WCH}	10	–	15	–	15	–	ns
Write command hold time ref. to $\overline{RAS}$		t_{WCR}	45	–	55	–	60	–	ns
Write command pulse width		t_{WP}	10	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time		t_{RWL}	20	–	20	–	20	–	ns
Write command to $\overline{CAS}$ lead time		t_{CWL}	20	–	20	–	20	–	ns
Data setup time	9)	t_{DS}	0	–	0	–	0	–	ns
Data hold time	9)	t_{DH}	15	–	15	–	15	–	ns
Data hold time ref. to $\overline{RAS}$		t_{DHR}	50	–	55	–	60	–	ns
Refresh period		t_{REF}	–	16	–	16	–	16	ms
Write command setup time	10)	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ setup time	13)	t_{CSR}	5	–	5	–	5	–	ns
$\overline{CAS}$ hold time	13)	t_{CHR}	15	–	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time		t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time	13)	t_{CPN}	10	–	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time	13)	t_{WRP}	10	–	10	–	10	–	ns
Write hold time ref. to $\overline{RAS}$	13)	t_{WRH}	10	–	10	–	10	–	ns

Notes see page 201.

Notes for pages 197 to 200:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading.
Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (max) and V_{IL} (max) are reference levels for measuring timing of input signals.
Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

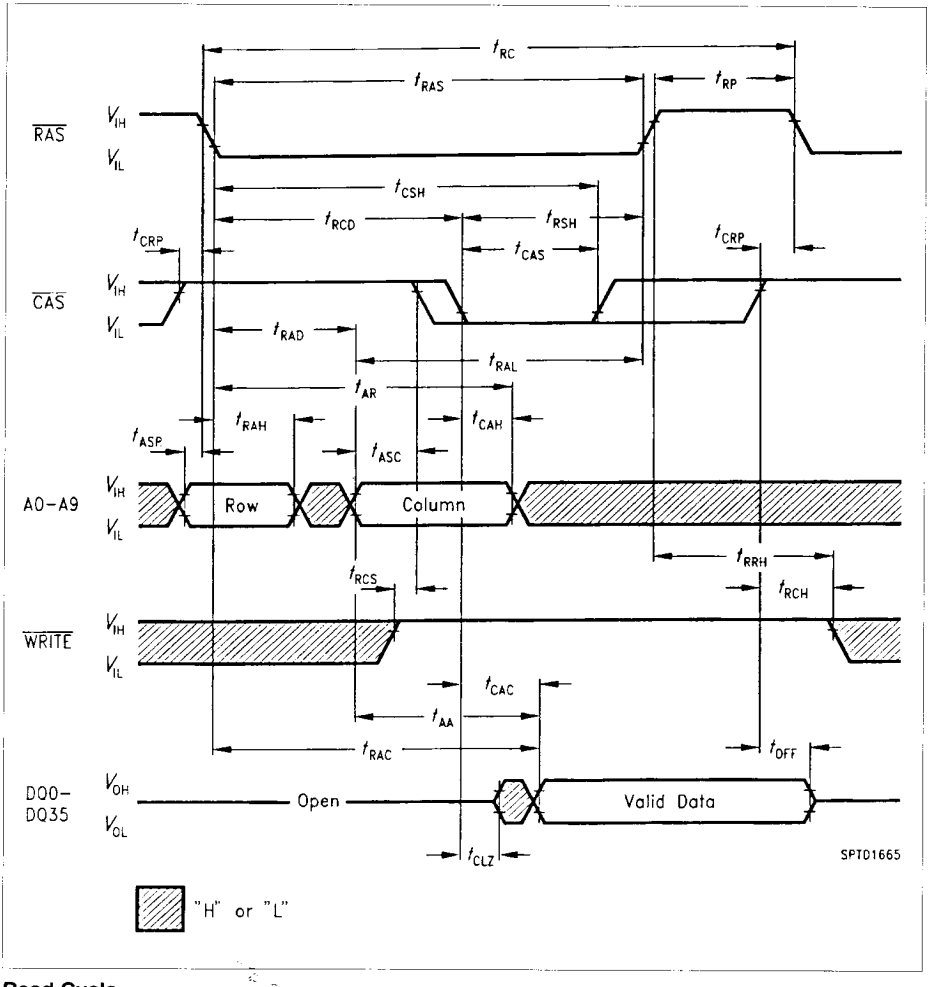
10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and data out pin will remain open (high impedance).

11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAS}.

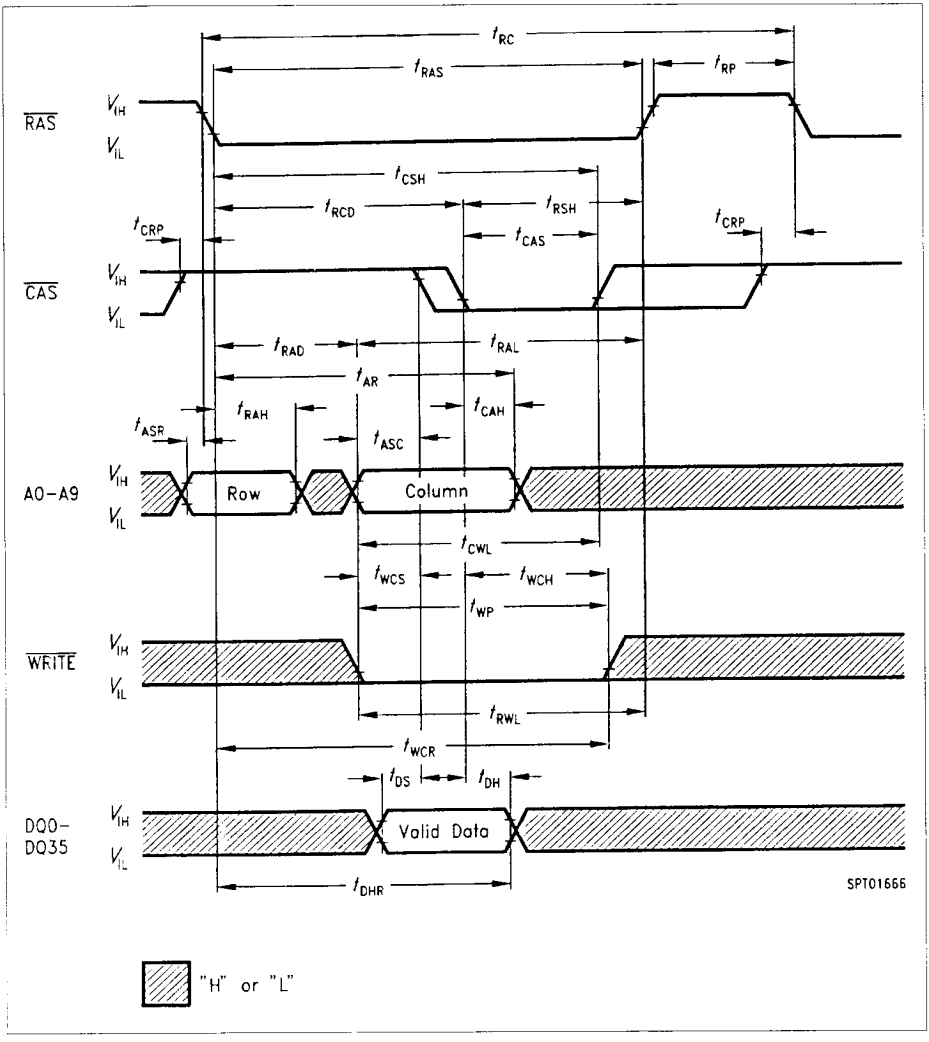
12) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

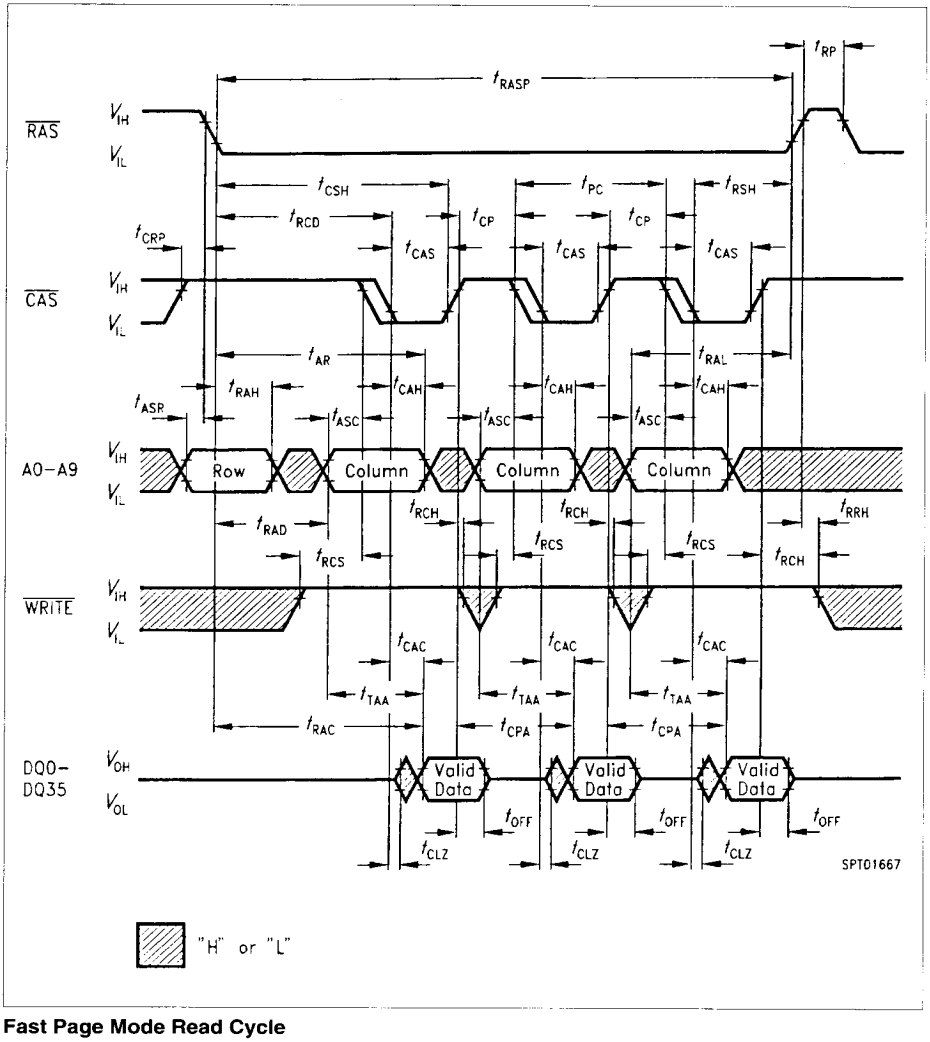
Waveforms



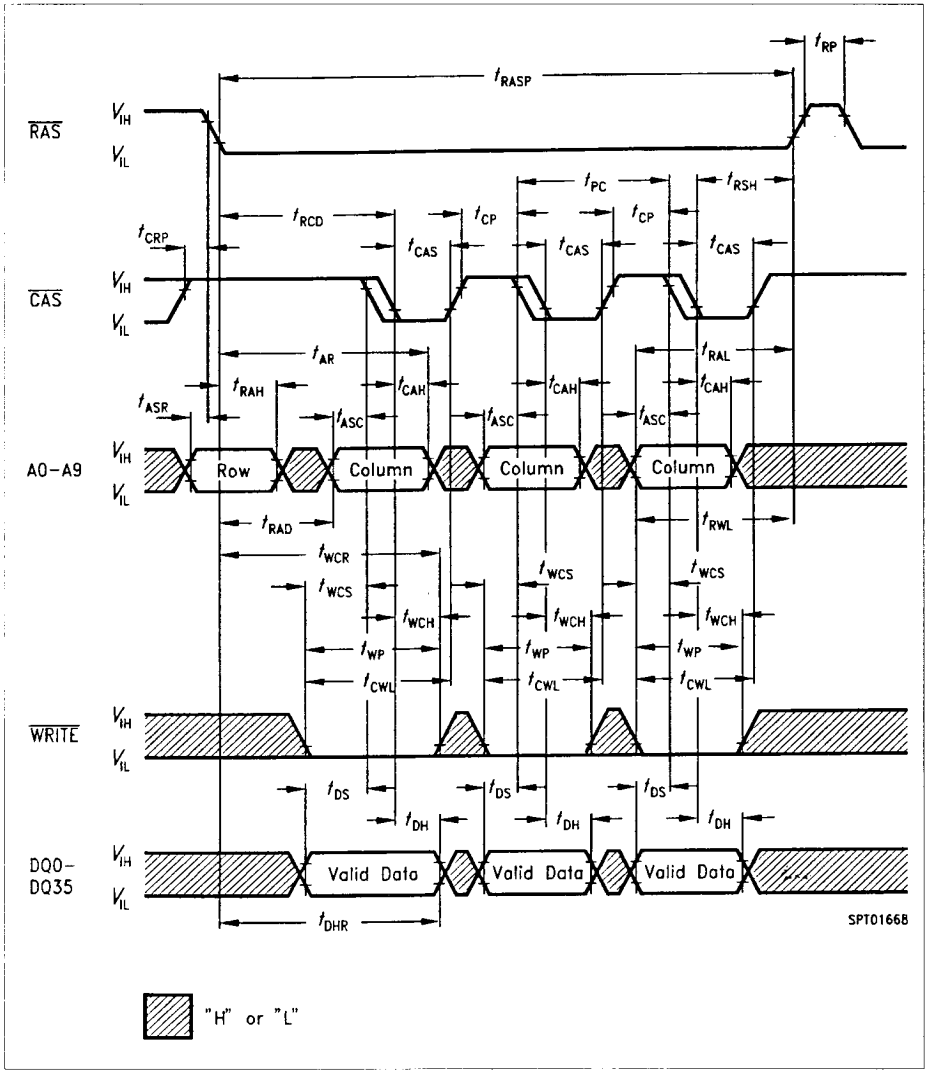
Read Cycle



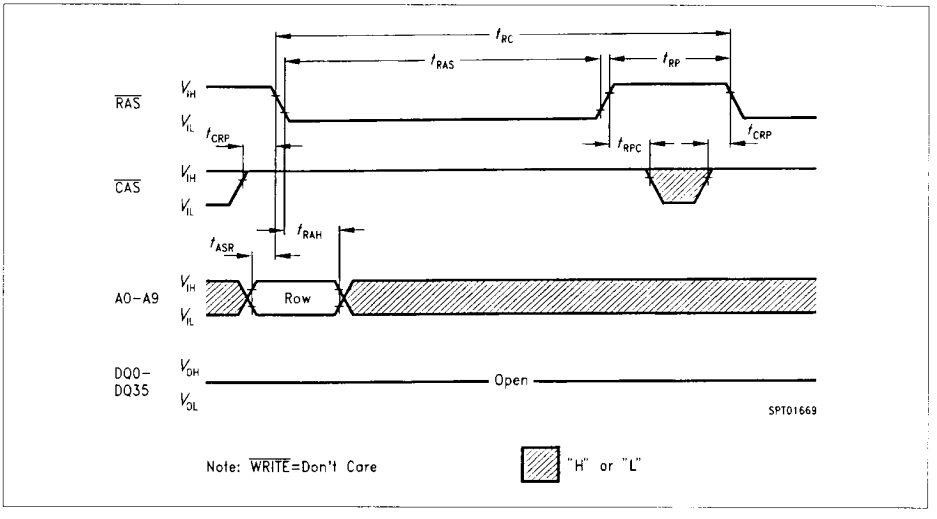
Write Cycle (early write)



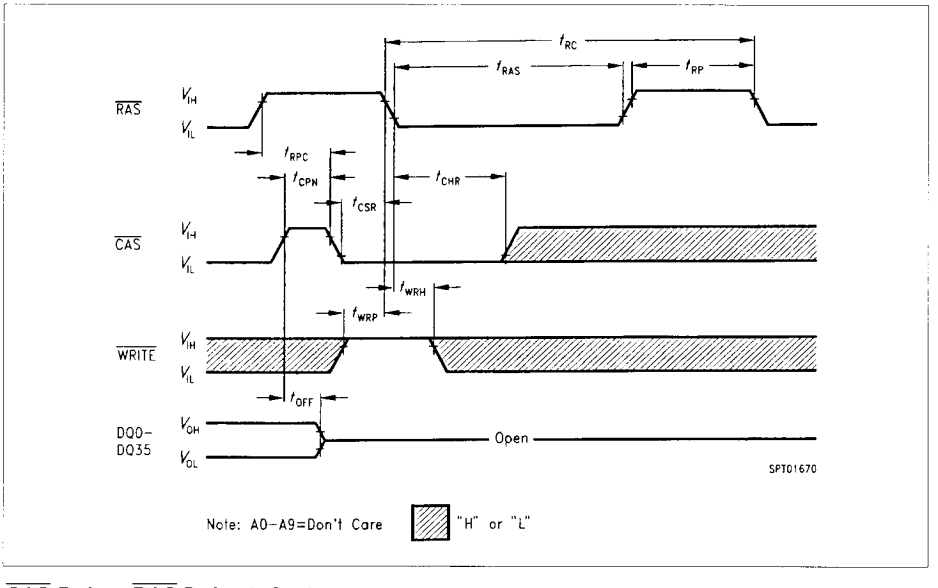
Fast Page Mode Read Cycle



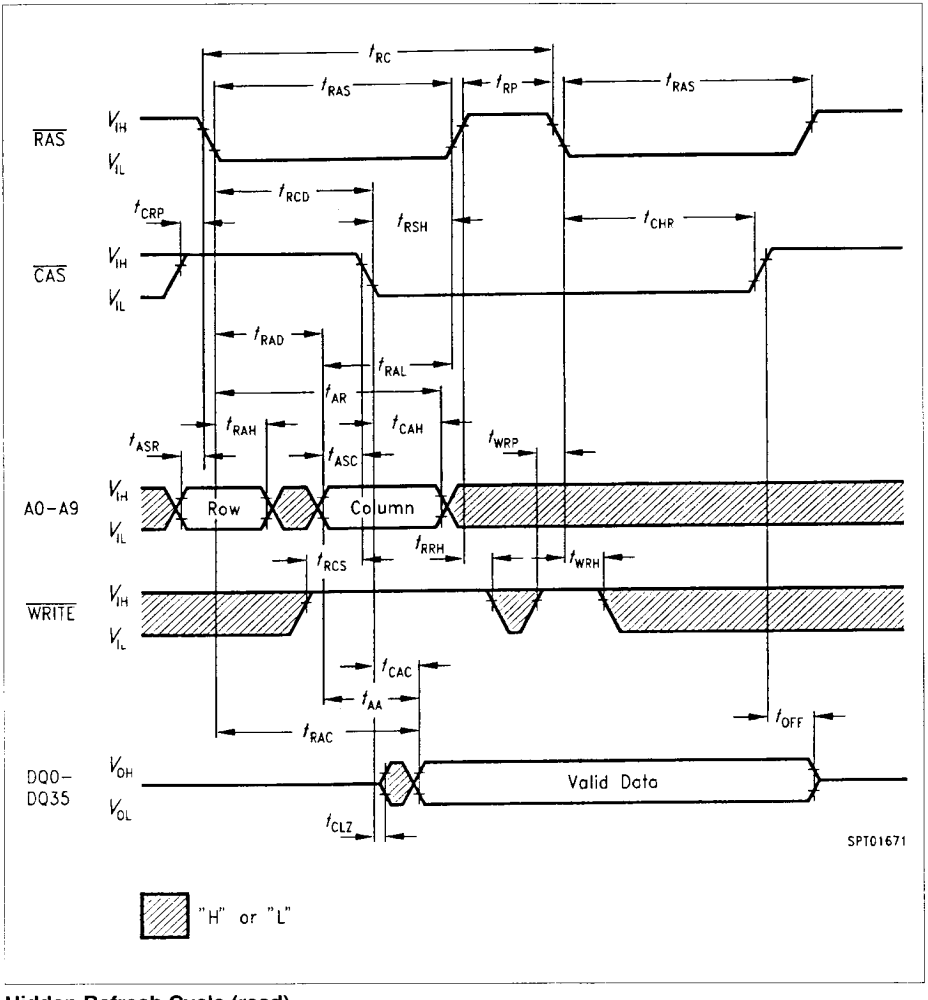
Fast Page Mode Write Cycle (early write)



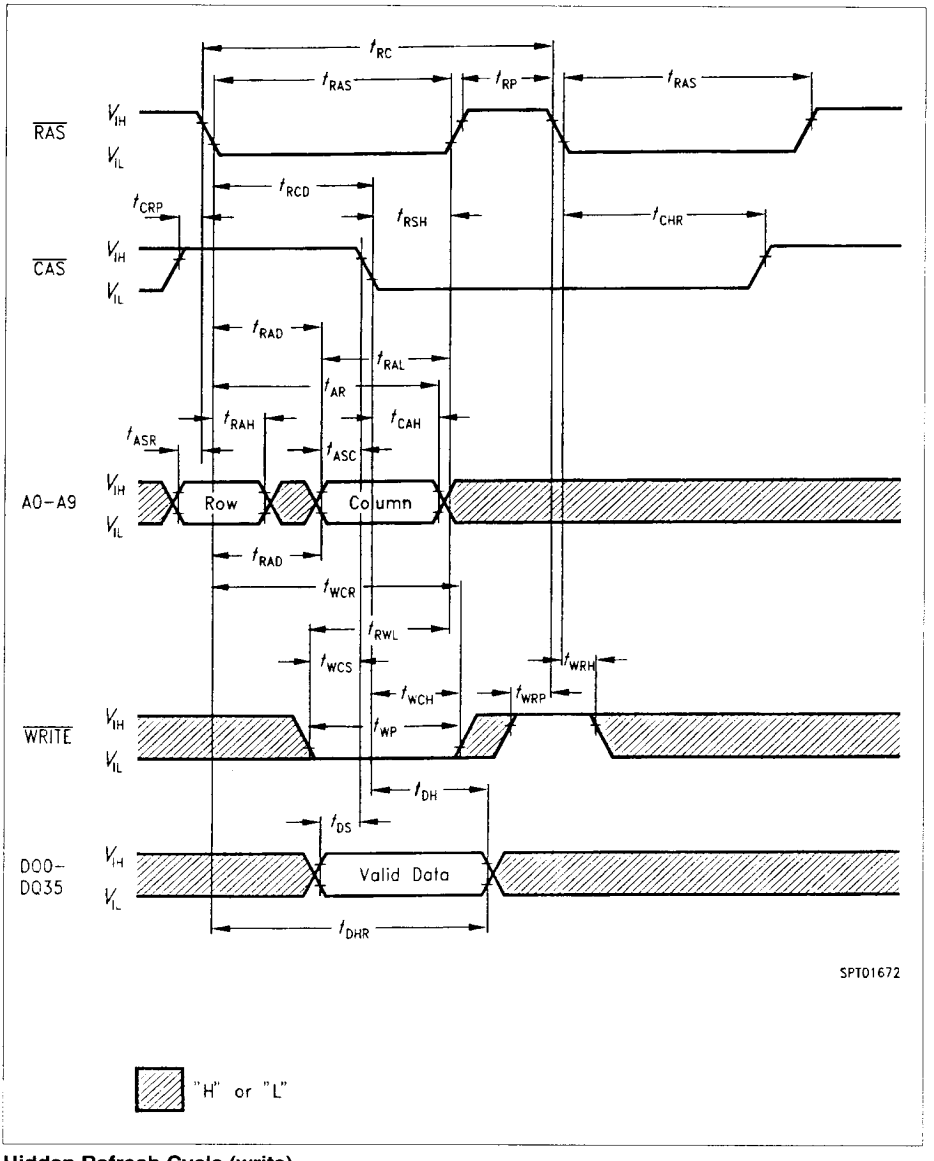
RAS-Only Refresh Cycle



CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle (read)



Hidden Refresh Cycle (write)