U-Series Channelless Architecture Gate Arrays

HUGHES AIRCRAFT COMPANY
MICROELECTRONICS CENTER

DESCRIPTION

Hughes U-Series VHSIC endorsed channelless gate arrays are a family of advanced technology logic structures. The family consists of configurable arrays that range in complexity from 1K to 40K equivalent 2-input gates. The Series is based on Hughes high performance HCMOS II 2-micron ($l_{eff} = 1.2\mu$) double metal CMOS process. The channelless structures combine the most desirable features of both conventional gate arrays and standard cells, to yield a semicustom solution that is tightly packed, high-performing and readily implemented. These features are attainable because the U-Series arrays do not include dedicated routing paths, and because they are easily implemented with the automated Hughes design tool.

The tools provide a fully integrated and automated approach to implementing U-Series designs. Mentor workstations are used to complete the front-end operations of schematic capture, logic simulation, timing estimation and test vector generation. Placement and routing is done with Hughes proprietary and highly efficient layout software. Results from layout are then used with workstation routines to back annotate to further evaluate timing performance prior to mask making and fabrication. The tools automate all design steps from schematic capture to generation of mask tapes.

FEATURES

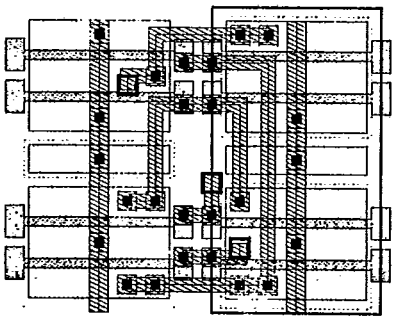
- Channelless Array Structures
- Fully Automated Implementation
- Array Complexity from 1K to 40K gates
- Output Drive of 6 TTL Loads
- 2-micron Technology, HCMOS-II
- Effective Channel Length of 1.2-micron
- Gate Propagation Delays of 0.4ns
- Operating Power of 8μW/gate/MHz

U-SERIES CHANNELLESS ARRAY FAMILY*

Array	2-Input Equivalents	I/O Pins	Total Pins
HU1140	40672	248	256
HU1132	32120	220	228
HU1120	19608	172	180
HU1115	14504	148	156
HU1109	8816	116	124
HU1107	6600	100	108
HU1105	4704	84	92
HU1103	2992	68	76
HU1102	2016	56	64
HU1101	1040	40	48

*Available packages are described in Section X. Consult factory for custom package requirements.

TYPICAL 8-TRANSISTOR CELL



Hughes Aircraft Company has licensed from LSI Logic Corporation, the right to utilize their products and software tools for resale of VLSI devices to the military and government agencies. Two primary methods to alternate sourcing LSI Logic products are:

1. The customer shall provide Hughes the same data packet that is normally provided to LSI Logic. Hughes shall perform the back-end services of placement, routing, design validation, mask making, and fabrication of prototypes.

2. With customer prior written release, Hughes shall purchase LSI Logic tooling databases (mask, assembly, and test). This method of alternate sourcing is reserved for production requirements after the devices have been originally prototyped by LSI Logic.

L7000 SERIES ARRAY FAMILY – Double Metal 2.0 micron CMOS technology

ARRAY	GATE COUNT	I/O PINS	TOTAL PINS
LL7080	880	44	52
LL7140	1443	58	66
LL7220	2224	70	78
LL7320	3192	80	96
LL7420	4242	98	114
LL7600	6072	122	138
LL7840	8370	150	166
LL71000	10013	158	174

L9000 SERIES ARRAY FAMILY – Double Metal 1.5 micron CMOS technology

ARRAY	GATE COUNT	I/O PINS	TOTAL PINS
LL9080	880	44	52
LL9140	1443	58	66
LL9220	2224	70	78
LL9320	3192	80	96
LL9420	4242	98	114
LL9600	6072	122	138
LL9840	8370	150	166
LL91000	10013	158	174

L10000 SERIES ARRAY FAMILY – Channelless HCMOS III Array Family with 1.5 micron design rules

ARRAY	GATE COUNT	I/O PADS	TOTAL PADS
LCA10026	25740	158	168
LCA10038	37932	184	204
LCA10051	50904	214	234
LCA10075	74970	256*	282
LCA10100	100182	256*	326
LCA10129	129042	256*	368

*I/O pins limited by test head.

MACRO LIBRARY

Hughes supports the U-Series channelless gate array family with comprehensive Macro Library that includes a wide variety of SSI and MSI logic functions. Each macro has been fully tested and simulated. New macros are being created on a regular basis, and custom macros may be constructed for specific design requirements.

The Macro Library is well documented with datasheets on characteristics of each macro. In each datasheet, information is included on general operation and truth tables, functional and schematic diagrams, propagation delay over various capacitive loads, and performance derating curves for both temperature and voltage.

DESIGN AUTOMATION

Hughes employs an integrated set of design software tools to fully automate the implementation of U-Series designs, which include a number of proprietary programs to facilitate all stages of the design cycle.

Full simulation tools are available for MENTOR workstations. Both logic and timing routines are based on the macro library characterization and use worst case parameters during simulation. Macros are placed and then interconnected using powerful layout algorithms that yield a very high probability of first routing success. The number of gates that may be utilized depend on circuit complexity. Actual interconnect capacitances are back annotated with the workstation software to verify performance. These integrated tools result in circuit success with first fabrication.

DEVELOPMENT CYCLE

Hughes is flexible in the manner of design interface. The customer may enter the development cycle at a number of different points. The most common flow has the customer conducting the workstation operations, while Hughes completes the physical design. Design reviews are held prior to design capture, layout, fabrication and production.

PRODUCT FLOW

Military product flows generally follow a build-to-suit format. Source control drawings determine the specific screens required. Generic high reliability and industrial screens are also offered by Hughes and are detailed in the CMOS databook.

PACKAGING

To accommodate the many available I/O of the U-Series arrays, Hughes has sized each array in a number of different package types. Side brazed DIPs, leadless carriers, pin grid arrays and flat packs are among the more usual selections. Custom package tooling is also an option. (See Section X)

HUGHES U-SERIES CHANNELLESS ARCHITECTURE GATE ARRAYS

ABSOLUTE MAXIMUM RATINGS

(Referenced to Ground)

DC Supply-Voltage Range (V_{DD}) ..... −0.3 to +7.0 Volts
Input Voltage (V_I) ..... −0.3 Volts to (V_{DD} +0.3) Volts
Maximum Junction Temp (T_J) ..... 150°C 10mA

Storage Temperature Range (T_{STG})
Ceramic ..... −65 to +150°C
Plastic ..... −40 to +125°C

RECOMMENDED OPERATING CONDITIONS

Military ..... −55 to +125°C
Industrial ..... −40 to + 85°C
Commercial ..... 0 to + 70°C
DC Supply voltage (V_{DD}) ..... +2 to +5.5 Volts

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC PARAMETERS

PARAMETERS	SYMBOL	CONDITIONS −55 < TA < +125°C	LIMITS min.	LIMITS max.	Unit
Output High Voltage 1 TTL 3 TTL 5 TTL	V_{OH}	V_{DD} = 4.6V I_{OH} = −1mA I_{OH} = −3mA I_{OH} = −5mA	4.1 4.1 4.1		V V V
Output Low Voltage 1 TTL 3 TTL 5 TTL	V_{OL}	V_{DD} = 4.6V I_{OL} = 1.6mA I_{OL} = 4.8mA I_{OL} = 8.0mA		0.4 0.4 0.4	V V V
Input High Voltage CMOS TTL SCHMITT	V_{IH}	V_{DD} = 4.6V, 5.5V	3.5 2.0 4.0		V V V
Input Low Voltage CMOS TTL SCHMITT	V_{IL}	V_{DD} = 4.6V, 5.5V		1.5 0.8 0.8	V V V
Input High Current 1) 2) No pull up/down Pull up Pull down	I_{IH}	V_{DD} = 5.5V, Vin = 5.5V	 10	10 10 250	µA µA µA
Input Low Current 1) 2) No pull up/down Pull up Pull down	I_{IL}	V_{DD} = 5.5V, Vin = 0V	−10 −250 −10	 −10 	µA µA µA
Device Static Curr. 2)	I_Q	V_{DD} = 5.5V No input drawing current		5	mA
Capacitance In 4) Out	Cin Cout	Includes 2.0 pf package capacitance		5 5	pF pF
Electro static damage protection 4)	V_{ESD}		4		KV
Schmitt trigger input hysterais 4)	V_{HYS}		1		V

NOTES:
1) Input currents listed also apply to 3-state buffers in high Z state.
2) I_{IH} and I_{IL} are not measured at −55°C.
3) Add 250µA for each input resistor sinking or sourcing current.
4) Guaranteed but not tested.
Speed power factor: P_Q = 8uW/SWITCHING GATE/MHZ, typical plus I/O power dissipation.

SEMI-CUSTOM DESIGN FLOW

The customer will perform design capture using the MENTOR design workstation and the Hughes U-Series macro library. (See Development Flow diagram)

The Pre-Layout Design Review is a major milestone, whereby HMC and the customer meet and review documents required to transfer the design to HMC for layout. All specification issues are completed at this time.

Timing verification of a circuit will be performed at HMC, as part of the normal quality assurance process, before the design is released for layout and fabrication.

All designs accepted for layout shall have three sets of test vectors included: Functional, DC parametrics, and AC parametrics. The AC tests may include up to six timing paths which characterize the speed of the circuit. After layout is complete, the speed of the device is tested against these vectors, with back annotated actual route delays and input transition data, using an advanced timing analysis tool called DANA. The post-route DANA simulation is the final assurance test (before mask making) by which HMC determines whether the circuit will meet the specification, because its accuracy approaches that of Spice.

A new Computer Aided Design tool called the DESIGN VERIFIER (developed by HMC's Design Automation), is used to achieve a one week turn-around time for the physical implementation of a U-Series Configurable Gate Array on a MENTOR workstation. One of the key features of the DESIGN VERIFIER, is checking the customer created test patterns, to be translated for use on the automatic test equipment, for testing the actual integrated circuit. The DESIGN VERIFIER "shell", complemented with the three sets of test vectors, produce a first-time working test program in about four hours.

HMC performs the following:

1. Rerun logic simulation using the test pattern to verify the netlist.
2. Auto placement and routing of the design.
3. Back annotation.
4. Perform post route timing verification.

A Critical Design Review is held whereby the customer approves the layouts and timing verification of the critical paths. With customer approval, HMC will then proceed to:

1. Make the PG tape.
2. Make masks.
3. Order DUT boards, Burn-In boards, and packages.
4. Produce wafers.
5. Install test programs.
6. Assemble and test initial prototypes.

HMC will deliver ten commercial prototypes, fully tested at 25C and 5v as part of normal NRE costs.

DEVELOPMENT CYCLE

Hughes offers several levels of design interface. Your engineers may do the entire design or Hughes' engineers can do the design work. The chart below details the levels of interface.