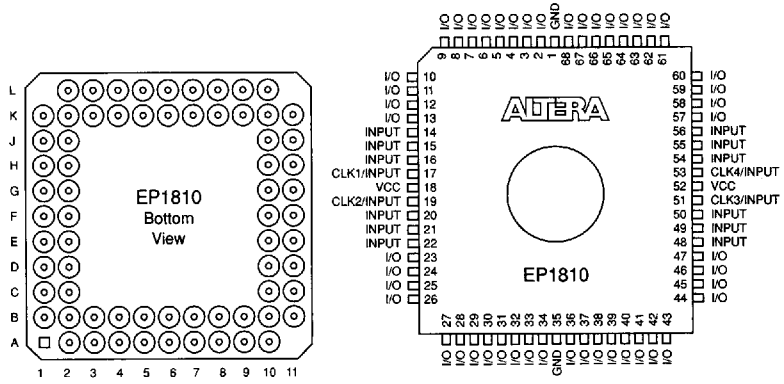
EP1810 EPLD

Features

- High-performance, 48-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 20, 25, 35, and 45 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Programmable I/O architecture with up to 64 inputs or 48 outputs
- Pin-, function-, and programming file-compatible with Altera's EP1810T and EP1810 MIL-STD-883-compliant devices
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in 68-pin windowed ceramic and one-time-programmable plastic packages (see Figure 28):
  - Pin-grid array package (ceramic PGA only)
  - J-lead chip carrier (JLCC and PLCC)

Figure 28. EP1810 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 2 in this data sheet for PGA package pin-out information. Windows in ceramic packages only.



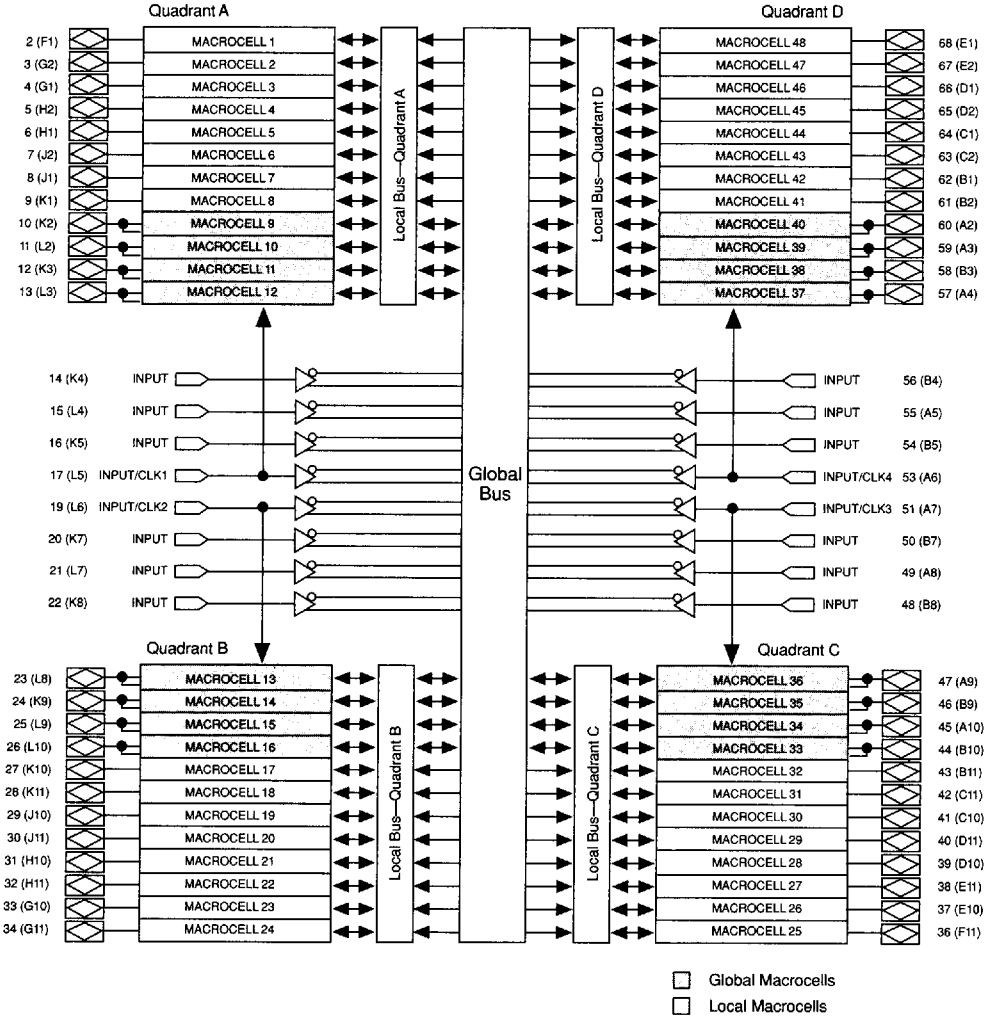
68-Pin PGA 68-Pin J-Lead

General Description

The Altera EP1810 EPLD offers LSI density, TTL-equivalent speed, and low power consumption. The EP1810 has 48 macrocells, 16 dedicated input pins, and 48 I/O pins (see Figure 29). The EP1810 is divided into four quadrants, each containing 12 macrocells. Of the twelve macrocells in each quadrant, 8 have quadrant feedback and are "local" macrocells. (See "Feedback Selection" earlier in this data sheet for more information.) The remaining 4 macrocells in the quadrant are "global" macrocells. Both local and global macrocells can access signals from the global bus, which consists

Figure 29. EP1810 Block Diagram

Numbers in parentheses are for J-lead packages. Numbers without parentheses are for PGA packages.



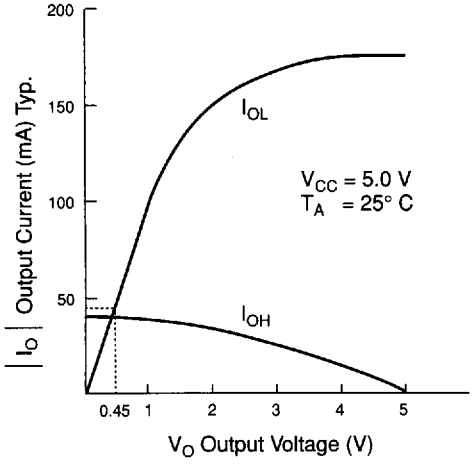
of the true and complement forms of the dedicated inputs and the true and complement forms of the feedbacks from the global macrocells.

The EP1810 also has four dedicated inputs (one in each quadrant) that can be used as quadrant Clock inputs. If the dedicated input is used as a Clock pin, the input feeds the Clock input of all registers in that particular quadrant.

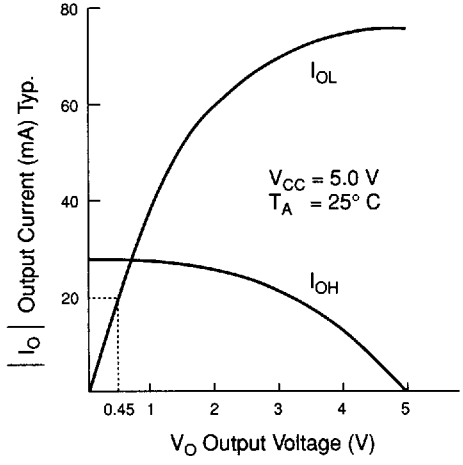
Figure 30 shows the output drive characteristics of EP1810 I/O pins and typical supply current (I_{CC}) versus frequency for the EP1810 EPLDs.

Figure 30. EP1810 Maximum Output Drive Characteristics & I_{CC} vs. Frequency

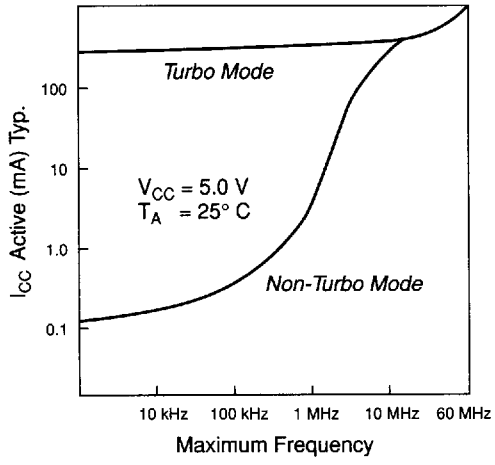
Output Drive Characteristics of EP1810-20 and EP1810-25 EPLDs



Output Drive Characteristics of EP1810-35 & EP1810-45 EPLDs



I_{CC} vs. Frequency of EP1810 EPLDs



Absolute Maximum Rating See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300	300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*Note (3)*		50	ns
t_F	Input fall time			50	ns

DC Operating Conditions *Note (2), (4), (5)*

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC		3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC				0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND		–10		10	µA
I_{CC1}	V_{CC} supply current	V_I = V_{CC} or GND, I_O = 0,	-20, -25		50	150	µA
	(non-turbo, standby)	*Notes (6), (7)*	-35, -45		35	150	µA
I_{CC2}	V_{CC} supply current	V_I = V_{CC} or GND, No load,	-20, -25		20	40	mA
	(non-turbo, active)	f = 1.0 MHz, *Note (7)*	-35, -45		10	30 (40)	mA
I_{CC3}	V_{CC} supply current	V_I = V_{CC} or GND, No load,	-20, -25		180	225 (250)	mA
	(turbo, active)	f = 1.0 MHz, *Note (7)*	-35, -45		100	180 (240)	mA

Capacitance *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

AC Operating Conditions: EP1810-20, EP1810-25 *Note (5)*

External Timing Parameters			EP1810-20		EP1810-25		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	25	ns
t_{PD2}	I/O input to non-registered output			22		28	25	ns
t_{SU}	Global clock setup time		13		17		25	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15		18	0	ns
t_{CH}	Global clock high time		8		10		0	ns
t_{CL}	Global clock low time		8		10		0	ns
t_{ASU}	Array clock setup time		8		10		25	ns
t_{AH}	Array clock hold time		8		10		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	25	ns
t_{CNT}	Minimum global clock period			20		25	0	ns
f_{CNT}	Maximum internal frequency	*Note (7)*	50		40		0	MHz
f_{MAX}	Maximum clock frequency	*Note (10)*	62.5		50		0	MHz

Internal Timing Parameters			EP1810-20		EP1810-25		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{IN}	Input pad and buffer delay			5		7	0	ns
t_{IO}	I/O input pad and buffer delay			2		3	0	ns
t_{LAD}	Logic array delay			9		12	25	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		6	0	ns
t_{ZX}	Output buffer enable delay			6		6	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (11)*		6		6	0	ns
t_{SU}	Register setup time		8		10		0	ns
t_{H}	Register hold time		8		10		0	ns
t_{IC}	Array clock delay			9		12	25	ns
t_{ICS}	Global clock delay			4		5	0	ns
t_{FD}	Feedback delay			3		3	–25	ns
t_{CLR}	Register clear time			9		12	25	ns

AC Operating Conditions: EP1810-35, EP1810-45 *Note (5)*

External Timing Parameters			EP1810-35		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		35		45	30	ns
t_{PD2}	I/O input to non-registered output			40		50	30	ns
t_{SU}	Global clock setup time		25		30		30	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		20		25	0	ns
t_{CH}	Global clock high time		12		15		0	ns
t_{CL}	Global clock low time		12		15		0	ns
t_{ASU}	Array clock setup time		10		11		30	ns
t_{AH}	Array clock hold time		15		18		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		35		45	30	ns
t_{CNT}	Minimum global clock period			35		45	0	ns
f_{CNT}	Maximum internal frequency	*Note (7)*	28.6		22.2		0	MHz
f_{MAX}	Maximum clock frequency	*Note (10)*	40		33.3		0	MHz

Internal Timing Parameters			EP1810-35		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{IN}	Input pad and buffer delay			7		6	0	ns
t_{IO}	I/O input pad and buffer delay			5		5	0	ns
t_{LAD}	Logic array delay			19		28	30	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		9		11	0	ns
t_{ZX}	Output buffer enable delay			9		11	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (11)*		9		11	0	ns
t_{SU}	Register setup time		10		10		0	ns
t_{H}	Register hold time		15		18		0	ns
t_{IC}	Array clock delay			19		28	30	ns
t_{ICS}	Global clock delay			4		8	0	ns
t_{FD}	Feedback delay			6		7	–30	ns
t_{CLR}	Register clear time			24		32	30	ns

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For all Clocks: t_R and t_F = 100 ns (50 ns for military and industrial temperature versions).
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When the Turbo Bit is not set (non-turbo mode), an EP910 EPLD enters standby mode if no logic transitions occur for 100 ns (after the last transition).
(7) Measured with a device programmed as four 12-bit counters. I_{CC} measured at 0° C.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. Pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP1810-20, EP1810-25, EP1810-35, EP1810-45
Industrial Temp.	(–40° C to 85° C)	EP1810-25, EP1810-45
Military Temp.	(–55° C to 125° C)	EP1810-45, *Note (1)*

Note:

(1) Only military-temperature-range devices are listed. MIL-STD-883-compliant product specifications are provided in "EP1810 MIL-STD-883-Compliant EPLD" in this data sheet and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

Pin-Out Information

Table 2 provides pin-out information for EP1810 devices in the PGA package.

Table 2. EP1810 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	GND	K4	INPUT
A3	I/O	B10	I/O	F11	I/O	K5	INPUT
A4	I/O	B11	I/O	G1	I/O	K6	VCC
A5	INPUT	C1	I/O	G2	I/O	K7	INPUT
A6	CLK4/INPUT	C2	I/O	G10	I/O	K8	INPUT
A7	CLK3/INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	CLK1/INPUT
B4	INPUT	E2	I/O	J10	I/O	L6	CLK2/INPUT
B5	INPUT	E10	I/O	J11	I/O	L7	INPUT
B6	VCC	E11	I/O	K1	I/O	L8	I/O
B7	INPUT	F1	I/O	K2	I/O	L9	I/O
B8	INPUT	F2	GND	K3	I/O	L10	I/O