



E128VH, E500H

Ultra High Performance ECL ASICs

DESCRIPTION

The Fujitsu Ultra High Performance E128VH and E500H ASICs offer the highest speed performance available from any Fujitsu ASIC with signal frequencies up to 5 GB/s. Gate delays of 40 ps are specified for the E128VH. The performance of the I/O buffers is equally impressive. Typical edge rates for the E128VH are specified at 55 ps for the rising edge and 45 ps for the falling edge.

Developed to meet the need for a high-speed small circuit device with simplified design procedure and speedy turnaround, the Ultra High Performance Series ASICs are Fujitsu turnkey designs that use customer-provided performance specifications and logic functions. Device level simulation can be performed using SPICE.

The Ultra High Performance ASICs consist of a range of up to 500 equivalent gates, each made up of basic cells which may be designed into functional logic blocks with single-ended or differential outputs.

Basic Cell	Equivalent Gate Count
AND or 2:1 multiplexer	3 gates
Flip-flop with Set and Reset	8 gates
Latch or EXOR	5 gates
OR/NOR	1 gate

The maximum equivalent gate count for any basic cell is eight gates. Eight basic cells form a major cell.

GENERAL FEATURES

- Simplified implementation of customer-specified functions
- Device-level circuit simulation with SPICE
- Internal gate propagation delay = 65 ps (typ. single ended output)
40 ps (typ. differential output)
- Fast rise/fall times
- Power/speed tradeoffs
- Minimum jitter
- High-speed signals (up to 5 GB/s)

E128VH FEATURES

- 128 equivalent gates
- 26 I/O pins (maximum 8 outputs)
- V_{CC} = 6 pins, V_{EE} = 2 pins
- Conductive cooling
- Up to 5 GB/s

E500H FEATURES

- 504 equivalent gates
- 40 I/O pins
- V_{CC} = 14 pins, V_{EE} = 8 pins
- Up to 3 GB/s

ELECTRICAL CHARACTERISTICS

FLEXIBLE OUTPUTS

I/O Buffer	Power Supply			I/O Buffer	Power Supply		
(Pseudo ECL supported upon request)	+5 V	0 V	-	ECL Level	-	0 V	-5.2 V

ELECTRICAL CHARACTERISTICS (Continued)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{EE}	-60 to 0	V
Input Voltage	V_{IN}	-3.0 to 0	V
Output Current	I_{OUT}	-50	mA
Operating Temperature	T_C	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Rating	Series	Symbol	Condition
Power Supply Voltage	10KH	V_{EE}	-5.2 V \pm -5%
	100K		-4.5 V \pm -0.3%
Terminal Voltage	10KH, 100K	V_T	-2.0 V \pm 5%
Output Terminating Resistance	10KH, 100K	R_T	50 Ω
Input Terminating Resistance	10KH, 100K	R_{TIN}	50 Ω
Operating Temperature	10KH, 100K	T_C	-40 to +85°C

ELECTRICAL CHARACTERISTICS (Continued)

DC CHARACTERISTICS (10 KH)

Recommended operating conditions unless otherwise specified

$V_{CC} = GND, V_{EE} = 5.2 V$

Parameter	Symbol	Condition	T_C (°C)	Value			Unit
				Minimum	Typical	Maximum	
Output High Voltage	V_{OH}	$V_{IN}: V_{IH} \text{ or } V_{IL}$	-40	-1.10	-	-0.89	V
			0	-1.04	-	-0.84	
			25	-1.00	-0.92	-0.81	
			75	-0.94	-	-0.735	
			85	-0.93	-	-0.72	
Output Low Voltage	V_{OL}	Output connected to -2.0 V thru 50 Ω	-40	-1.95	-	-1.63	V
			0	-1.95	-	-1.63	
			25	-1.95	-1.75	-1.63	
			75	-1.95	-	-1.60	
			85	-1.95	-	-1.595	
Input High Voltage	V_{IH}	$V_{IN}: V_{IH} \text{ or } V_{IL}$	-40	-1.21	-	-0.89	V
			0	-1.17	-	-0.84	
			25	-1.13	-	-0.81	
			75	-1.07	-	-0.735	
			85	-1.06	-	-0.72	
Input Low Voltage	V_{IL}		-40	-1.95	-	-1.52	
			0	-1.95	-	-1.48	
			25	-1.95	-	-1.48	
			75	-1.95	-	-1.45	
			85	-1.95	-	-1.445	

ELECTRICAL CHARACTERISTICS (Continued)

DC CHARACTERISTICS (100 K)

Recommended operating conditions unless otherwise specified

$V_{CC} = \text{GND}, V_{EE} = 4.5 \text{ V}$

Parameter	Symbol	Condition	T_C (°C)	Value			Unit
				Minimum	Typical	Maximum	
Output High Voltage	V_{OH}	$V_{IN}: V_{IH} \text{ or } V_{IL}$ Output connected to -2.0 V thru 50Ω	-40	-1.085	-	-0.88	V
			0	-1.025	-	-0.88	
			25	-1.025	-0.955	-0.88	
			75	-1.025	-	-0.88	
			85	-1.025	-	-0.88	
Output Low Voltage	V_{OL}		-40	-1.81	-	-1.555	V
			0	-1.81	-	-1.62	
			25	-1.81	-1.72	-1.62	
			75	-1.81	-	-1.62	
			85	-1.81	-	-1.62	
Input High Voltage	V_{IH}	-40	-1.165	-	-0.88	V	
		0	-1.165	-	-0.88		
		25	-1.165	-	-0.88		
		75	-1.165	-	-0.88		
		85	-1.165	-	-0.88		
Input Low Voltage	V_{IL}	-40	-1.81	-	-1.475	V	
		0	-1.81	-	-1.475		
		25	-1.81	-	-1.475		
		75	-1.81	-	-1.475		
		85	-1.81	-	-1.475		

ELECTRICAL CHARACTERISTICS

(Continued)

AC CHARACTERISTICS (E128VH)

Recommended operating conditions unless otherwise specified

Parameter	Symbol	Output Type	Value			Unit
			Minimum	Typical	Maximum	
Output Rise Time	t_r	Low Power	–	220	–	ps
		Medium Power	–	100	–	
		High Power	–	75	–	
		Ultra High Power	–	60	–	
Output Fall Time	t_f	Low Power	–	210	–	ps
		Medium Power	–	90	–	
		High Power	–	65	–	
		Ultra High Power	–	50	–	
Toggle Frequency	f_{tog}	–	5.0	7.0	–	GHz
Propagation Delay Time	t_{pd}	Single-ended		65	*	ps
		–	–	–		
		Differential		40		

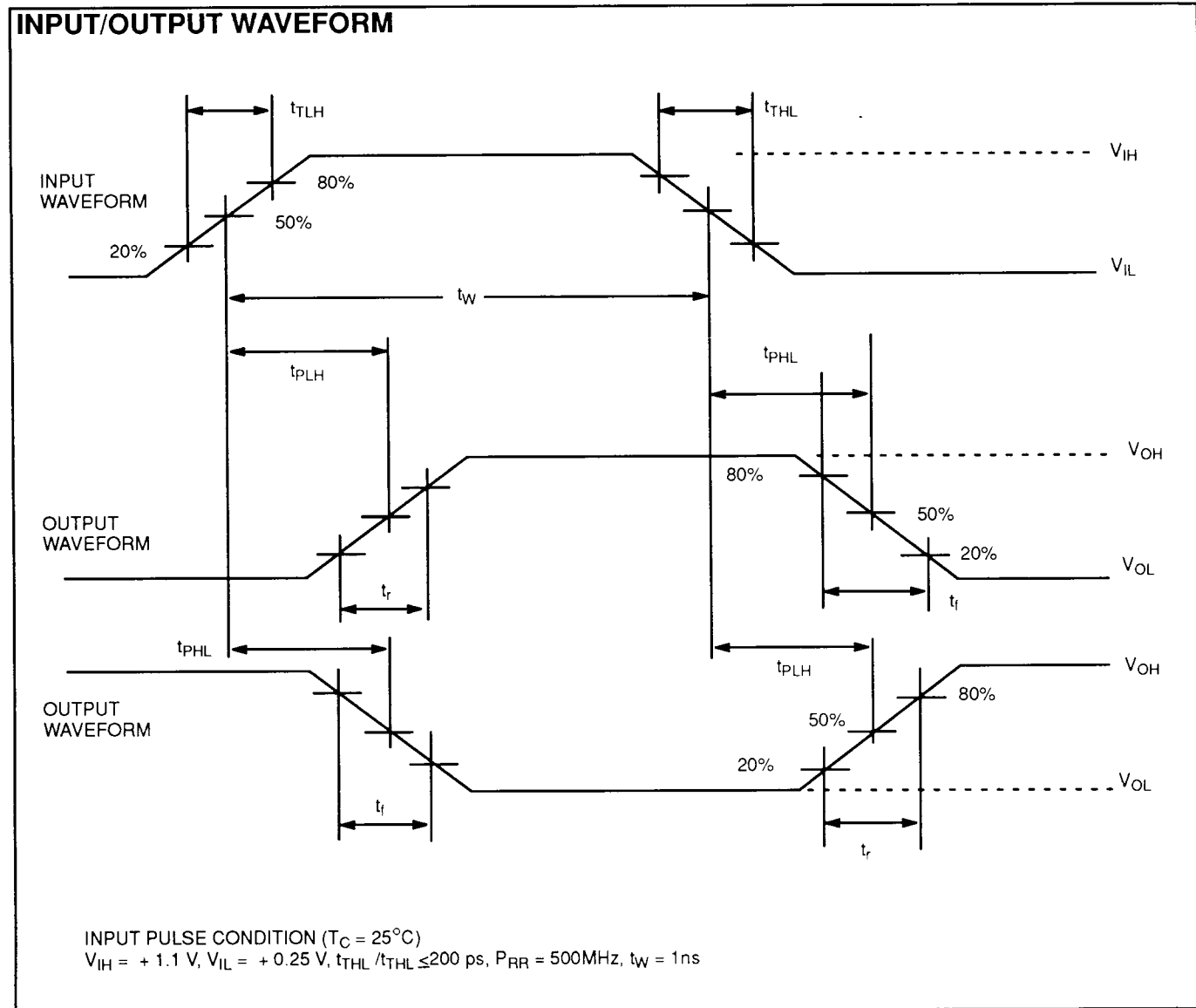
AC CHARACTERISTICS (E500H)

Recommended operating conditions unless otherwise specified

Parameter	Symbol	Output Type	Value			Unit
			Minimum	Typical	Maximum	
Output Rise Time	t_r	Low Power	–	370	–	ps
		Medium Power	–	190	–	
		High Power	–	105	–	
		Ultra High Power	–	80	–	
Output Fall Time	t_r	Low Power	–	370	–	ps
		Medium Power	–	190	–	
		High Power	–	90	–	
		Ultra High Power	–	70	–	
Toggle Frequency	f_{tog}	–	3.0	4.5	–	GHz
Propagation Delay Time	t_{pd}	Single-ended		80	*	ps
		–	–	–		
		Differential		60		

ELECTRICAL CHARACTERISTICS

(Continued)



E500H SERIES CHIP STRUCTURE

Internal Cells	Basic Cell	ECL Up to 2-level Series Gate -AND/2:1 Multiplexer = 3 cells -Flip-flop with Set and Reset = 8 cells -Latch/EXOR = 5 cells -OR/NOR = 1 cell with either Single-ended or Differential Outputs
	Cell Matrix	63 Basic Cells (7 x 9)
	Current Levels	Four options for I_{EF} : 0.18 (L)/0.35 (M)/0.65 (H)/1.3 (UH) Three Options for I_{CS} : 0.18 (L)/0.35 (M,H)/0.7 (UH)
Output Buffers	2 UH Power Output Macros 12 H Power Output Macros 24 M Power Output Macros 24 L Power Output Macros Four options for I_{CS} (3 mA/4 mA/8 mA/16 mA)	
Signal Pins	Total: 40 pins maximum Input: 39 pins maximum Output: 24 pins maximum	
Power Supply Pins	V_{CC} : 14 pins V_{EE} : 6 pins	V_{EE2} = 2 pins V_T = 6 pins

E128VH SERIES CHIP STRUCTURE

Internal Cells	Basic Cell	ECL Up to 2-level Series Gate -Flip-flop with Set and Reset = 4 cells -Two of AND/2:1 Multiplexer = 3 cells -Two of Latch/EXOR/AND/2:1 Multiplexer = 5 cells -Two of OR/NOR = 1 cell with either Single-ended or Differential Outputs
	Cell Matrix	16 Basic Cells (4 x 4)
	Current Levels	Three options for I_{EF} : (0.5 mA/1 mA/1.75 mA) One fixed I_{CS} : (1 mA)
Output Gates	2 UH Power Output Macros 4 H Power Output Macros 8 M Power Output Macros 8 L Power Output Macros Four options for I_{CS} (4 mA/8 mA/16 mA/24 mA)	
Signal Pins	Total: 20 pins maximum Input: 19 pins maximum Output: 8 pins maximum	
Power Supply Pins	V_{CC} : 6 pins V_{EE} : 2 pins	

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Circuit diagrams using Fujitsu products are included to illustrate typical semiconductor applications. Information sufficient for construction purposes may not be shown.

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