DPS512X16Cn3

Ceramic, 512Kx16 Very High Speed SRAM Stack Modules

DESCRIPTION:

The DPS512X16Cn3 High Speed SRAM "STACK" modules are a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC). Available in straight leaded, "J" leaded or gullwing leaded packages, or mounted on a 50-pin PGA co-fired ceramic substrate. The module packs 8-Megabits of low-power CMOS static RAM in an area as small as 0.463 in^2, while maintaining a total height as low as 0.705 inches.

The DPS512X16Cn3 STACK modules contain eight individual 128K x 8 SRAMs, each packaged in a hermetically sealed SLCC, making the modules suitable for commercial, industrial and military applications.

By using SLCCs, the "Stack" family of modules offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

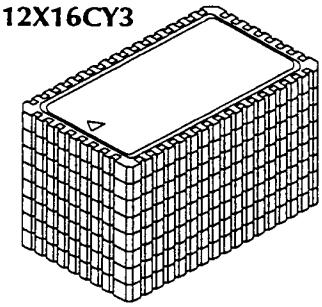
FEATURES:

- Organizations Available: 512Kx16 or 1024Kx8
- Access Times: 20*, 25, 30, 35, 45ns
- Fully Static Operation - No clock or refresh required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- Packages Available:

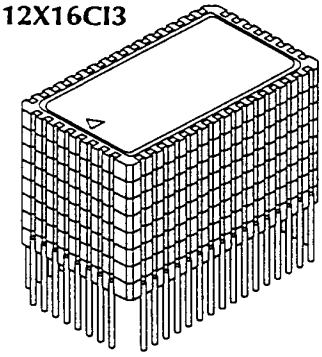
DPS512X16CY3	48 - Pin SLCC Stack
DPS512X16CI3	48 - Pin Straight Leaded Stack
DPS512X16CH3	48 - Pin Gullwing Leaded Stack
DPS512X16CJ3	48 - Pin "J" Leaded Stack
DPS512X16CA3	50 - Pin PGA Dense-Stack

* Commercial only.

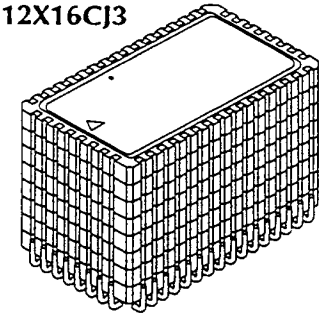
DPS512X16CY3



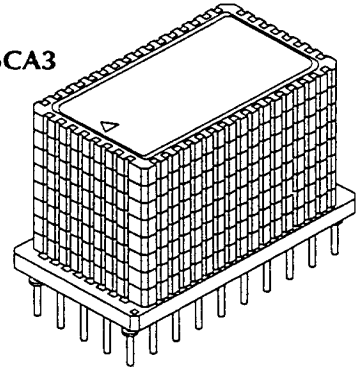
DPS512X16CI3



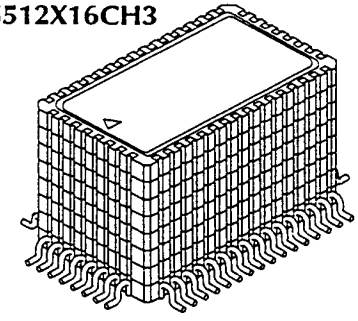
DPS512X16CJ3



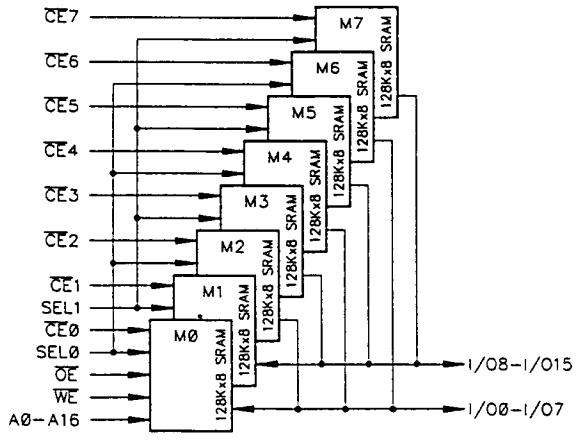
DPS512X16CA3



DPS512X16CH3



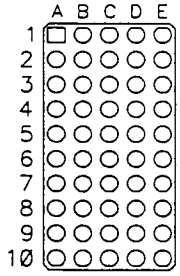
FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O15	Data Input/Output
$\overline{CE0}$ - $\overline{CE7}$	Low Chip Enables
SEL0, SEL1	High Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

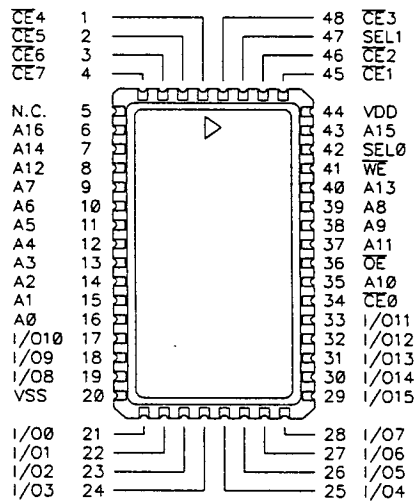
(TOP VIEW)



50 - PIN PGA
DENSE-STACK

	A	B	C	D	E
1	$\overline{CE7}$	$\overline{CE5}$	$\overline{CE3}$	$\overline{CE2}$	$\overline{CE1}$
2	VSS	$\overline{CE6}$	$\overline{CE4}$	SEL1	VDD
3	N.C.	A16	$\overline{WE}$	SEL0	A15
4	A14	A12	A7	A8	A13
5	A6	A5	$\overline{OE}$	A11	A9
6	A4	A3	A2	$\overline{CE0}$	A10
7	A1	A0	I/O13	I/O12	I/O11
8	I/O10	I/O9	I/O8	I/O15	I/O14
9	VSS	I/O1	I/O3	I/O5	VDD
10	I/O0	I/O2	I/O4	I/O6	I/O7

48 - PIN LEADLESS STACK
48 - PIN STRAIGHT LEADED STACK
48 - PIN "J" LEADED STACK
48 - PIN GULLWING LEADED STACK



RECOMMENDED OPERATING RANGE[3]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Operating Temp.	-55	+25	+125	°C

TRUTH TABLE						
Mode	SEL	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	L	X	X	X	HIGH-Z	Standby
Not Selected	X	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	H	L	H	H	HIGH-Z	Active
Read	H	L	H	L	D_{OUT}	Active
Write	H	L	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}= -4.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL}=8.0mA	-	0.4	V

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	100	pF	V_{IN}[2] = 0V
C_{CE}	Chip Enable	40		
C_{SEL}	Active High Chip Select	50		
C_{WE}	Write Enable	100		
C_{OE}	Output Enable	100		
$C_{I/O}$	Data Input/Output	90		

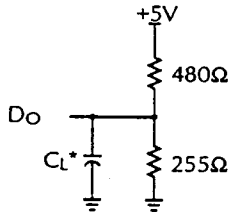
DC OPERATING CHARACTERISTICS: Over operating ranges											
Symbol	Characteristics	Test Conditions		TYP. (†)	C		I		M		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-	-5	+5	-5	+5	-5	+5	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-	-10	+10	-10	+10	-10	+10	µA
I_{CC}	Operating Supply Current	Cycle = min., Duty = 100%	X8	205		280		280		300	mA
		I_{OUT} = 0mA	X16	290		400		400		440	
I_{SB1}	Full Standby Supply Current	V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ V_{SS} 0.2V		3.2		40		40		40	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		120		160		160		160	mA
I_{DR3}	Data Retention Supply Current (3V)	V_{DR} = 3V, $\overline{CE}$ ≥ V_{DR} -0.2V, or SEL ≤ 0.2V		0.56		3.20		4.80		16.00	mA
I_{DR2}	Data Retention Supply Current (2V)	V_{DR} = 2V, $\overline{CE}$ ≥ V_{DR} -0.2V, or SEL ≤ 0.2V		0.28		2.00		3.20		14.40	mA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA		-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA		-	2.4		2.4		2.4		V

† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

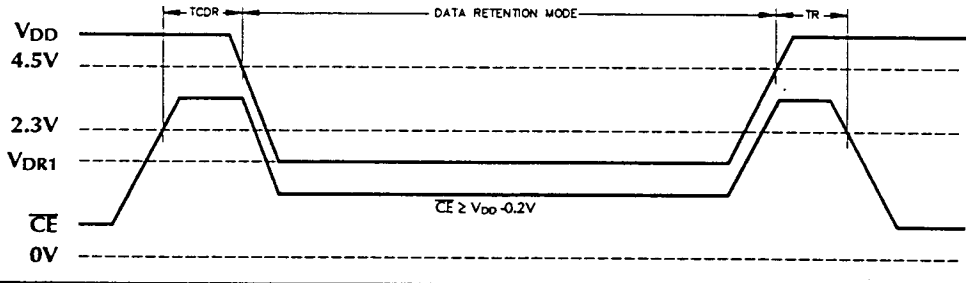
OUTPUT LOAD		
Load	C_L	Parameters Measured
1	30 pF	except t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}
2	5 pF	t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}

Figure 1. Output Load
* Including Probe and Jig Capacitance.

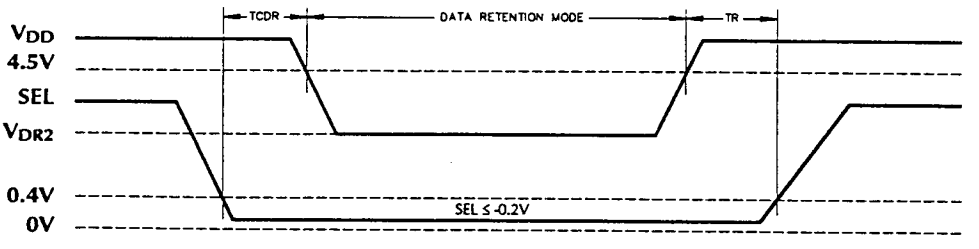


Data Retention AC Characteristics [8]						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{CE} \geq V_{DR}$ -0.2V, SEL $\leq V_{DR}$ 0.2V, $V_{IN} \geq V_{DR}$ -0.2V, or $V_{IN} \leq$ 0.2V	2.0	-	-	V
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled.



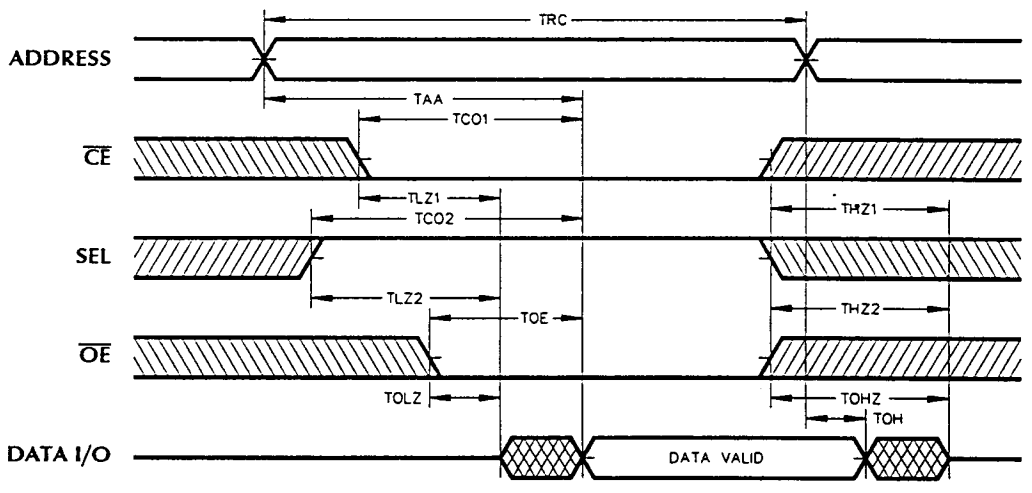
DATA RETENTION WAVEFORM: [8] SEL Controlled.



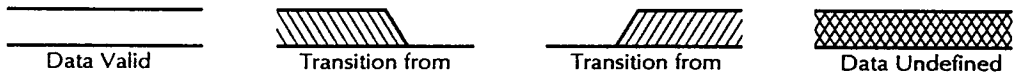
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	-20†		-25		-30		-35		-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	20		25		30		35		45		ns
2	t_{AA}	Address Access Time		20		25		30		35		45	ns
3	t_{CO1}	Chip Enable ($\overline{CE}$) to Output Valid		20		25		30		35		45	ns
4	t_{CO2}	Chip Enable (SEL) to Output Valid		20		25		30		35		45	ns
5	t_{OE}	Output Enable to Output Valid		8		10		15		20		25	ns
6	t_{LZ1}	Chip Enable ($\overline{CE}$) to Output in LOW-Z [4, 5]	3		3		3		3		3		ns
7	t_{LZ2}	Chip Enable (SEL) to Output in LOW-Z [4, 5]	3		3		3		3		3		ns
8	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	0		0		0		0		0		ns
9	t_{HZ1}	Chip Enable ($\overline{CE}$) to Output in HIGH-Z [4, 5]		10		12		15		20		25	ns
10	t_{HZ2}	Chip Enable (SEL) to Output in HIGH-Z [4, 5]		10		12		15		20		25	ns
11	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		8		10		15		20		25	ns
12	t_{OH}	Output Hold from Address Change	3		3		3		3		3		ns

† Commercial only.

READ CYCLE



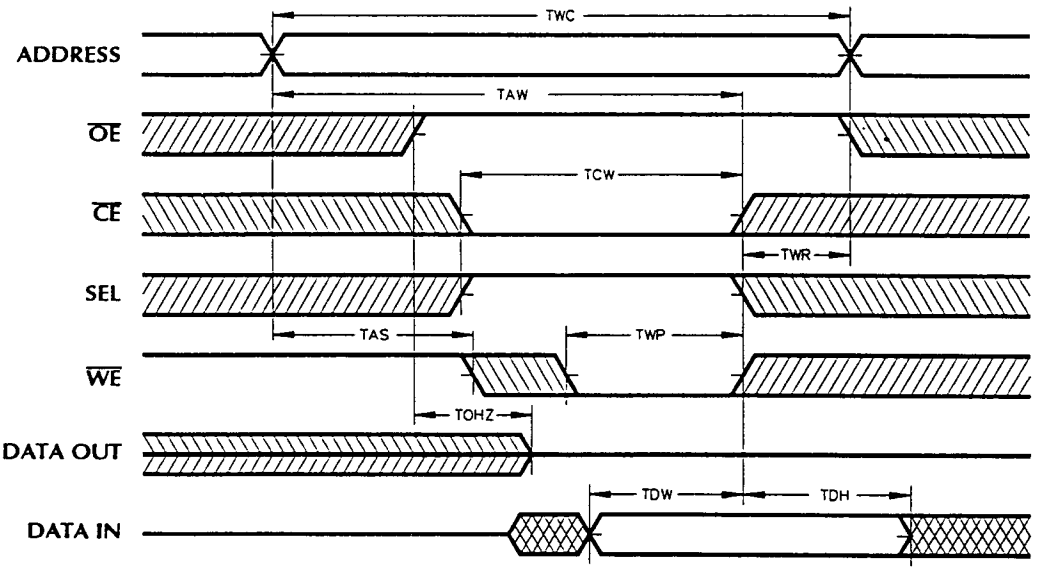
WAVEFORM KEY



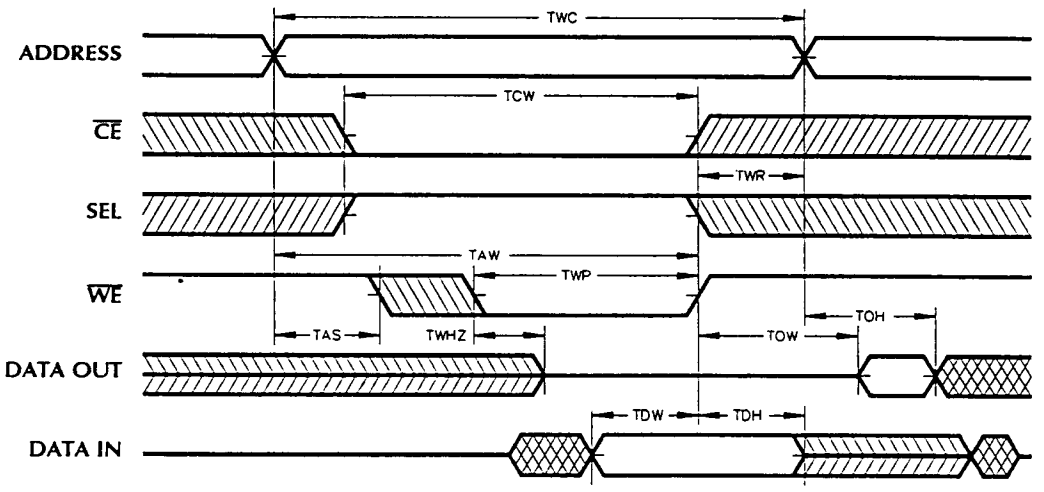
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6,7]: Over operating ranges													
No.	Symbol	Parameter	-20†		-25		-30		-35		-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	20		25		30		35		45		ns
14	t_{AW}	Address Valid to End of Write	15		20		25		30		40		ns
15	t_{CW}	Chip Enable to End of Write	15		20		25		30		40		ns
16	t_{AS}	Address Set-up Time*	0		0		0		0		0		ns
17	t_{WP}	Write Pulse Width	15		20		25		30		35		ns
18	t_{WR}	Write Recovery Time	0		0		0		0		0		ns
19	t_{WHZ}	Write Enable to Output in HIGH-Z [4,5]		8		10		12		15		20	ns
20	t_{DW}	Data to Write Time Overlap	12		15		15		20		25		ns
21	t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns
22	t_{OW}	Output Active from End of Write	3		3		3		3		3		ns

* Valid for both Read and Write Cycles.
† Commercial only.

WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ Clocked.



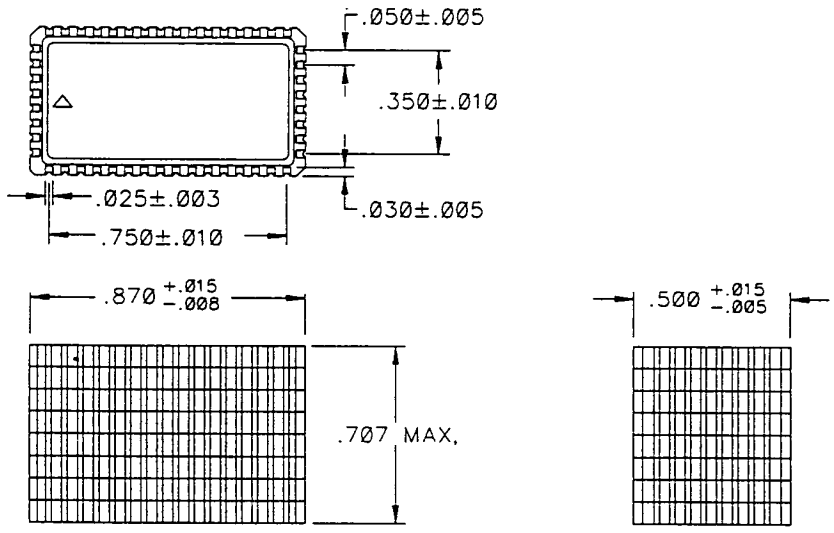
WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is LOW.



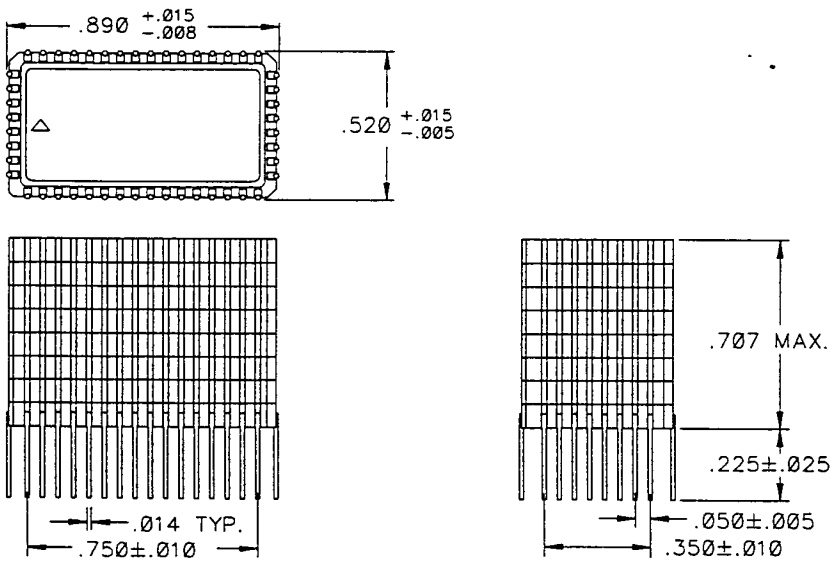
NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. SEL controls address buffer, $\overline{WE}$ buffer, $\overline{CE}$ buffer and $\overline{OE}$ buffer and D_{IN} buffer. If SEL controls Data Retention Mode, V_{IN} levels (Address, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, I/O) can be in the high impedance state. If $\overline{CE}$ controls Data Retention Mode, SEL must be SEL≥V_{DD} -0.2V or SEL ≤0.2V. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the High Impedance State.

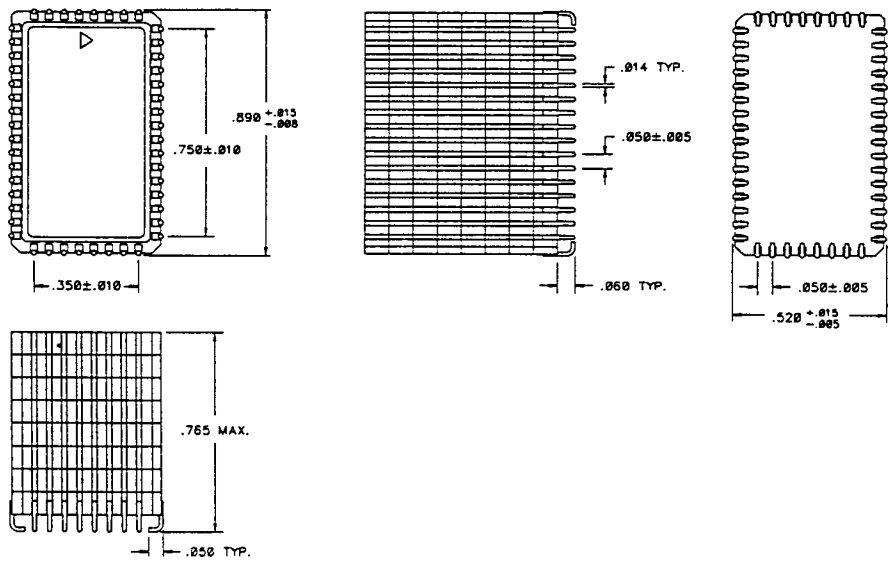
DPS512X16CY3 (48 - PIN LEADLESS STACK) MECHANICAL DRAWING



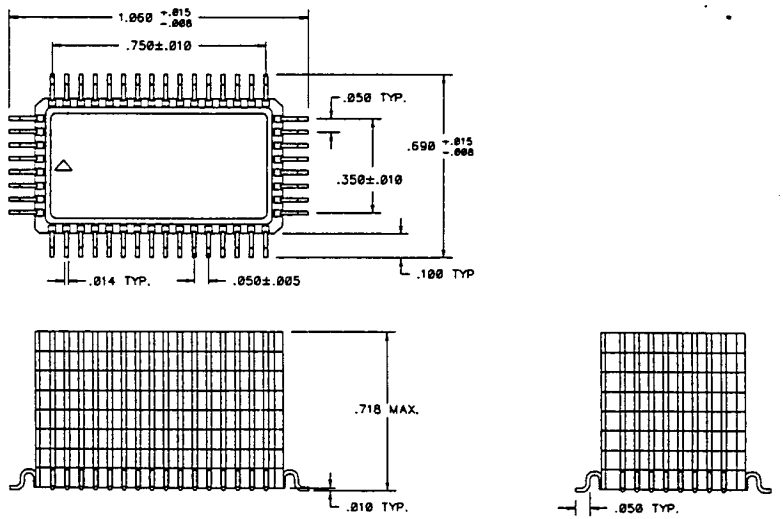
DPS512X16CI3 (48– PIN STRAIGHT LEADED STACK) MECHANICAL DRAWING



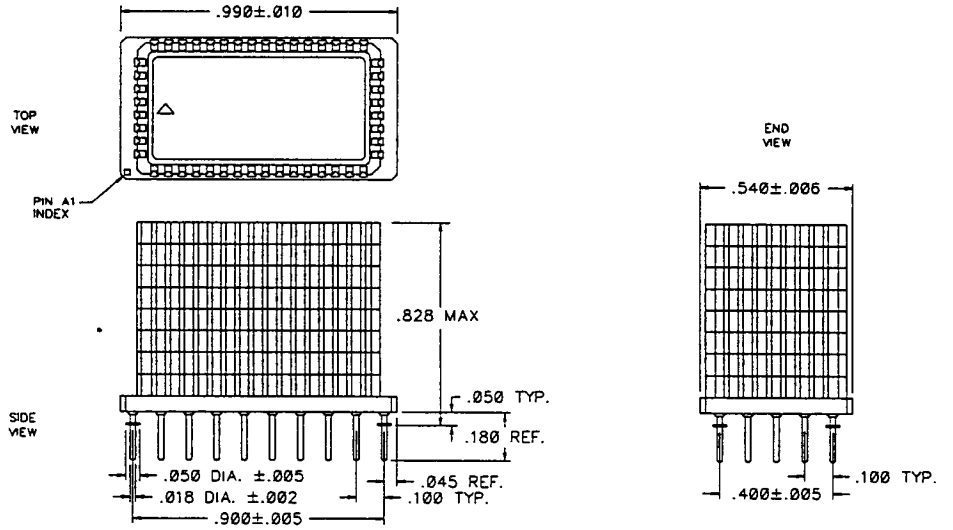
DPS512X16CJ3 (48 - PIN "J" LEADED STACK) MECHANICAL DRAWING



DPS512X16CH3 (48 - PIN GULLWING LEADED STACK) MECHANICAL DRAWING



DPS512X16CA3 (50 - PIN PGA) MECHANICAL DRAWING



ORDERING INFORMATION

DP S 512 X 16 C X3 – XX X

PREFIX | TYPE | MEMORY DEPTH | DESIG | MEMORY WIDTH | DESIG. | PACKAGE | SPEED | GRADE

C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	−40°C to +85°C
M	MILITARY	−55°C to +125°C
B	MIL−PROCESSED	−55°C to +125°C

20	20ns (COMMERCIAL ONLY)
25	25ns
30	30ns
35	35ns
45	45ns

A3	DENSE−STACK PGA (PIN GRID ARRAY)
H3	GULLWING LEADED SLCC STACK
I3	THRU−HOLE LEADED SLCC STACK
J3	"J" LEADED SLCC STACK
Y3	LEADLESS SLCC STACK

VERY HIGH SPEED / DUAL CHIP ENABLE

MODULE WITHOUT SUPPORT LOGIC

CMOS SRAM DEVICES

Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove, California 92641-1428
(714) 898-0007 ◆ (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772