

**DESCRIPTION:**

The DPS256X16Cn3/DPS256X16Bn3 High Speed SRAM "STACK" modules are a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC). Available in straight leaded, "J" leaded or gullwing leaded packages, or mounted on a 50-pin PGA co-fired ceramic substrate. The module packs 4-Megabits of low-power CMOS static RAM in an area as small as 0.463 in<sup>2</sup>, while maintaining a total height as low as 0.349 inches.

The DPS256X16Cn3/DPS256X16Bn3 STACK modules contain four individual 128K x 8 SRAMs, each packaged in a hermetically sealed SLCC, making the modules suitable for commercial, industrial and military applications.

The DPS256X16Bn3 has one active low Chip Enable ( $\overline{CE}$ ) and while the DPS256X16Cn3 an active low Chip Enable ( $\overline{CE}$ ) and an active high Select Line (SEL).

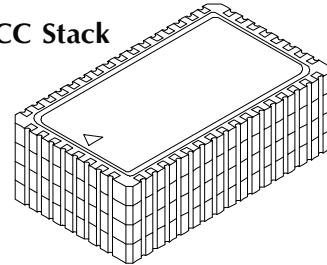
By using SLCCs, the "Stack" family of modules offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

**FEATURES:**

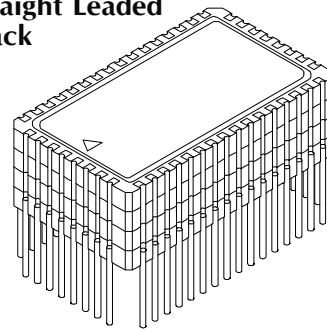
- Organizations Available: 256Kx16 or 512Kx8
- Access Times: 20\*, 25, 30, 35, 45ns
- Fully Static Operation - No clock or refresh required
- Single +5V Power Supply,  $\pm 10\%$  Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- Packages Available:
  - 48 - Pin SLCC Stack
  - 48 - Pin Straight Leaded Stack
  - 48 - Pin "J" Leaded Stack
  - 48 - Pin Gullwing Leaded Stack
  - 50 - Pin PGA Dense-Stack

\* Commercial only.

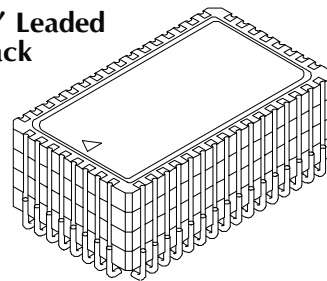
**SLCC Stack**



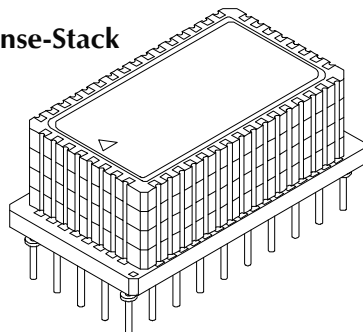
**Straight Leaded Stack**



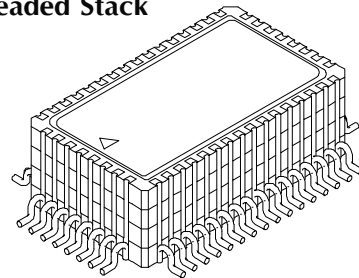
**"J" Leaded Stack**



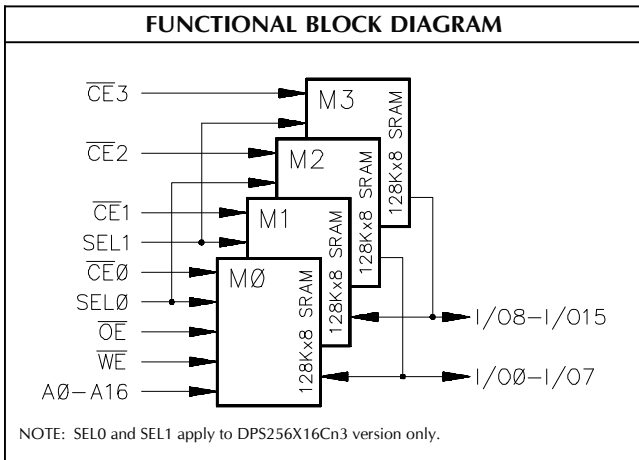
**Dense-Stack**



**Gullwing Leaded Stack**



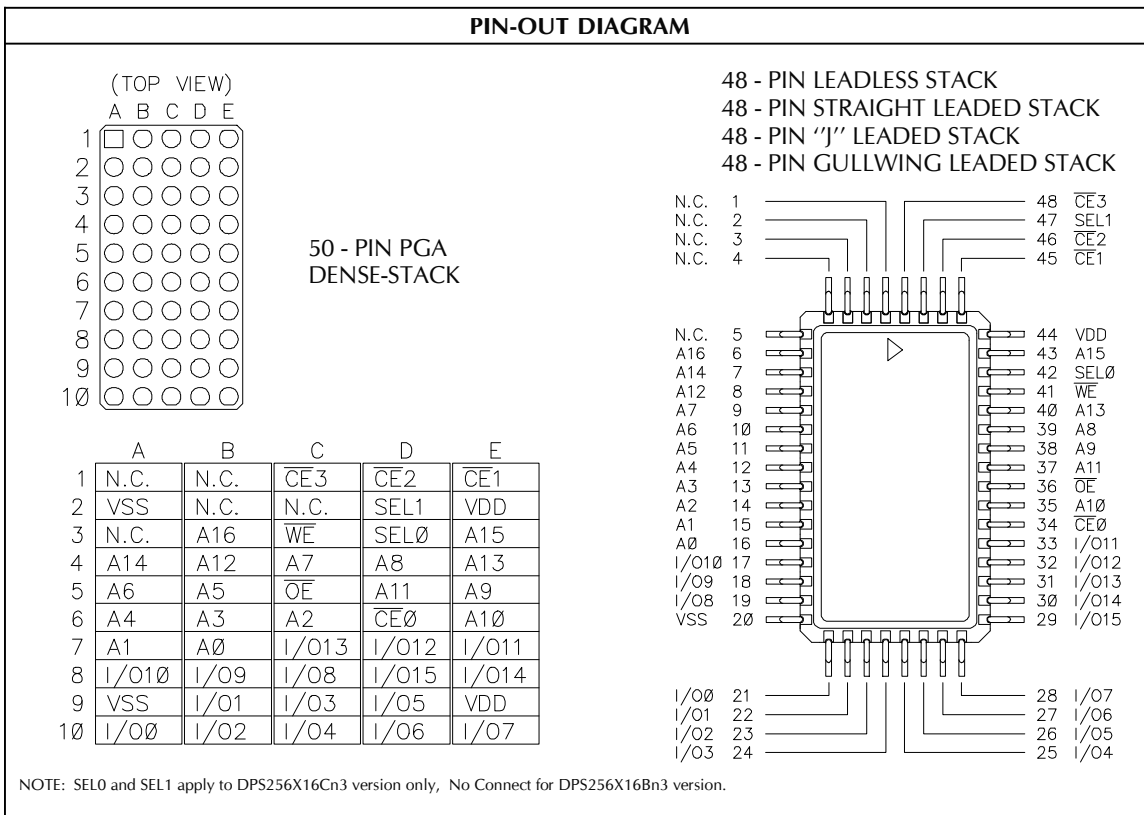
**FUNCTIONAL BLOCK DIAGRAM**



**PIN NAMES**

A0 - A16	Address Inputs
I/O0 - I/O15	Data Input/Output
$\overline{CE0} - \overline{CE3}$	Low Chip Enables
SEL0, SEL1	High Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VDD	Power (+5V)
VSS	Ground
N.C.	No Connect

**PIN-OUT DIAGRAM**



RECOMMENDED OPERATING RANGE <sup>3</sup>						
Symbol	Characteristic	Min.	Typ.	Max.	Unit	
V <sub>DD</sub>	Supply Voltage	4.5	5.0	5.5	V	
V <sub>IH</sub>	Input HIGH Voltage	2.2		V <sub>DD</sub> +0.3	V	
V <sub>IL</sub>	Input LOW Voltage	-0.5 <sup>2</sup>		0.8	V	
T <sub>A</sub>	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

TRUTH TABLE						
Mode	SEL	CE	WE	OE	I/O Pin	Supply Current
Not Selected	L	X	X	X	High-Z	Standby
Not Selected	X	H	X	X	High-Z	Standby
D <sub>OUT</sub> Disable	H	L	H	H	High-Z	Active
Read	H	L	H	L	D <sub>OUT</sub>	Active
Write	H	L	L	X	D <sub>IN</sub>	Active

H = HIGH                                      L = LOW                                      X = Don't Care  
NOTE: SEL applies to DPS256X16Cn3 version only.

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>OH</sub>	HIGH Voltage	I <sub>OH</sub> = -4.0mA	2.4		V
V <sub>OL</sub>	LOW Voltage	I <sub>OL</sub> = 8.0mA		0.4	V

ABSOLUTE MAXIMUM RATINGS <sup>3</sup>			
Symbol	Parameter	Value	Unit
T <sub>STC</sub>	Storage Temperature	-65 to +150	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
V <sub>DD</sub>	Supply Voltage <sup>1</sup>	-0.5 to +7.0	°C
V <sub>I/O</sub>	Input/Output Voltage <sup>1</sup>	-0.5 to V <sub>DD</sub> +0.5	V

CAPACITANCE <sup>4</sup> : T <sub>A</sub> = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C <sub>ADR</sub>	Address Input	40	pF	V <sub>IN</sub> <sup>2</sup> = 0V
C <sub>CE</sub>	Chip Enable	15		
C <sub>SEL</sub>	Active High Chip Select	25		
C <sub>WE</sub>	Write Enable	40		
C <sub>OE</sub>	Output Enable	40		
C <sub>I/O</sub>	Data Input/Output	25		

NOTE: C<sub>SEL</sub> applies to DPS256X16Cn3 version only.

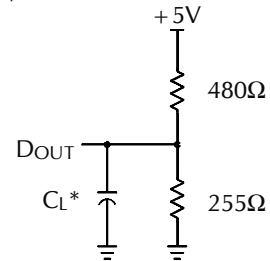
DC OPERATING CHARACTERISTICS: Over operating ranges											
Symbol	Characteristics	Test Conditions	Typ. (†)	C		I		M/B		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>DD</sub>	-	-20	+20	-20	+20	-20	+20	µA	
I <sub>OUT</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to V <sub>DD</sub> , CE or OE = V <sub>IH</sub> , or WE = V <sub>IL</sub>	-	-20	+20	-20	+20	-20	+20	µA	
I <sub>CC</sub>	Operating Supply Current	Cycle = min., Duty = 100% I <sub>OUT</sub> = 0mA	X8	175		230		245		265	mA
			X16	250		340		350		390	
I <sub>SB1</sub>	Full Standby Supply Current	V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤ V <sub>SS</sub> +0.2V	1.6		20		20		40	mA	
I <sub>SB2</sub>	Standby Current (TTL)	CE = V <sub>IH</sub>	100		120		140		140	mA	
I <sub>DR3</sub>	Data Retention Supply Current (3.0V)	V <sub>DR</sub> = 3.0V, CE ≥ V <sub>DR</sub> -0.2V, (or SEL ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤ +0.2V)	0.28		1.6		2.4		8.0	mA	
I <sub>DR2</sub>	Data Retention Supply Current (2.0V)	V <sub>DR</sub> = 2.0V, CE ≥ V <sub>DR</sub> -0.2V, (or SEL ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤ +0.2V)	0.14		1.0		1.6		7.2	mA	
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> = 8.0mA	-		0.4		0.4		0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = -4.0mA	-		2.4		2.4		2.4	V	

† Typical measurements made at +25°C, Cycle = min., V<sub>DD</sub> = 5.0V.  
NOTE: Test Conditions in parenthesis apply to DPS256X16Cn3 version only.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

Figure 1. Output Load

\* Including Probe and Jig Capacitance.

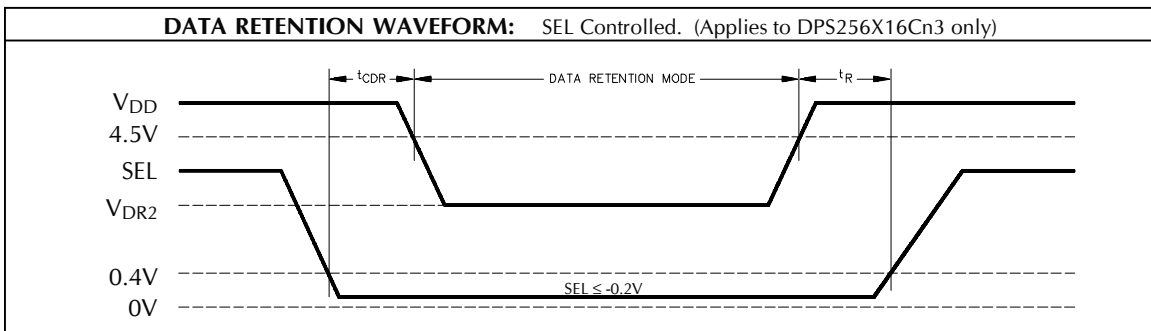
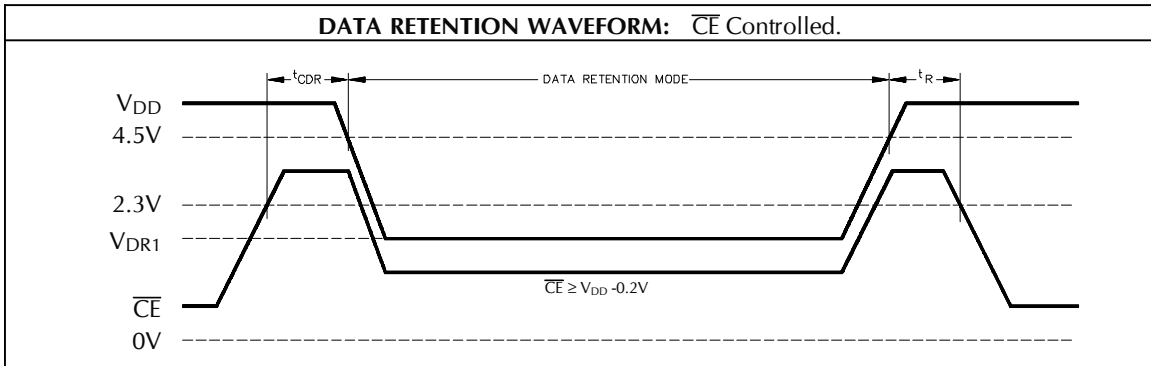


OUTPUT LOAD		
Load	CL	Parameters Measured
1	100pF	except tLZ1, tLZ2, tHZ1, tHZ2, tOHZ, tOLZ, and tWHZ
2	5pF	tLZ1, tLZ2, tHZ1, tHZ2, tOHZ, tOLZ, and tWHZ

NOTE: tLZ2 and tHZ2 apply to DPS256X16Cn3 version only.

Data Retention AC Characteristics <sup>8</sup>						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDR	VDD for Data Retention	$\overline{CE} \geq V_{DR} - 0.2V$ , ( $SEL \geq V_{DR} - 0.2V$ , or $V_{IN} \leq V_{DR} - 0.2V$ or $V_{IN} \leq 0.2V$ )	2.0	-	-	V
VCDR	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
tR	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

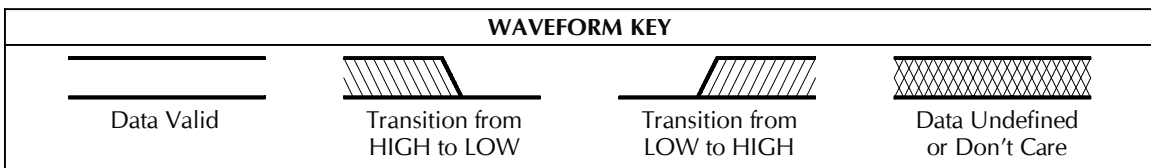
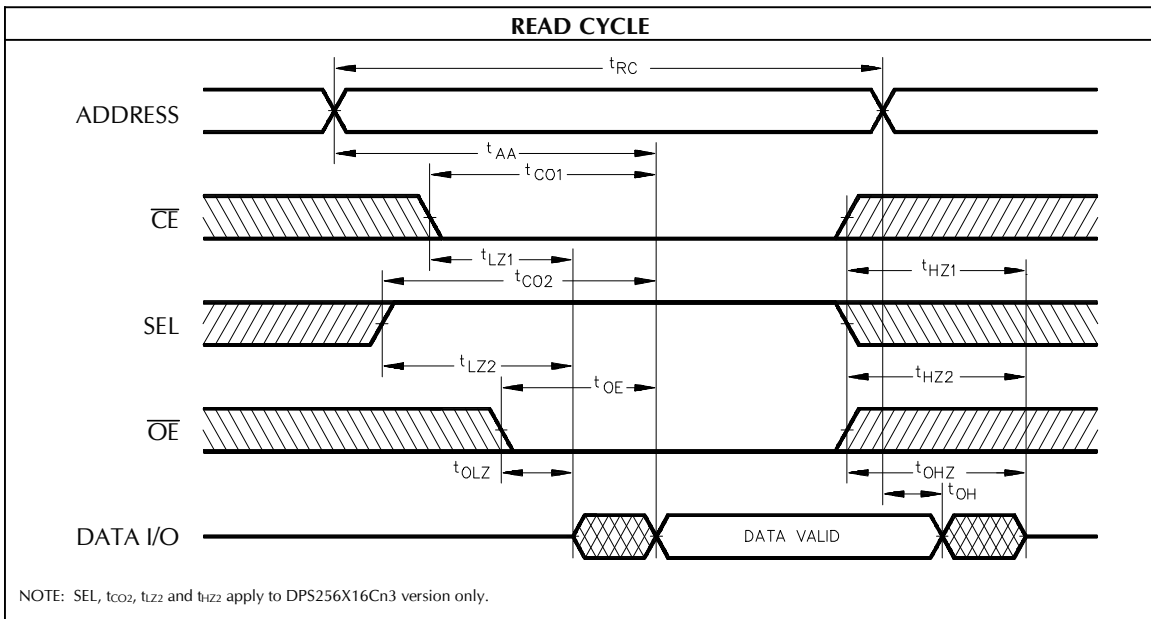
NOTE: Test Conditions in parenthesis apply to DPS256X16Cn3 version only.



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t <sub>RC</sub>	Read Cycle Time	20		25		30		35		45		ns
2	t <sub>AA</sub>	Address Access Time		20		25		30		35		45	ns
3	t <sub>CO1</sub>	$\overline{CE}$ to Output Valid		20		25		30		35		45	ns
4	t <sub>CO2</sub>	SEL to Output Valid		20		25		30		35		45	ns
5	t <sub>OE</sub>	Output Enable to Output Valid		8		10		15		20		25	ns
6	t <sub>LZ1</sub>	$\overline{CE}$ to Output in LOW-Z <sup>4,5</sup>	3		3		3		3		3		ns
7	t <sub>LZ2</sub>	SEL to Output in LOW-Z <sup>4,5</sup>	3		3		3		3		3		ns
8	t <sub>OLZ</sub>	Output Enable to Output in LOW-Z <sup>4,5</sup>	0		0		0		0		0		ns
9	t <sub>HZ1</sub>	$\overline{CE}$ to Output in HIGH-Z <sup>4,5</sup>		10		12		15		20		25	ns
10	t <sub>HZ2</sub>	SEL to Output in HIGH-Z <sup>4,5</sup>		10		12		15		20		25	ns
11	t <sub>OHZ</sub>	Output Enable to Output in HIGH-Z <sup>4,5</sup>		8		10		15		20		25	ns
12	t <sub>OH</sub>	Output Hold from Address Change	3		3		3		3		3		ns

\* Available in Commercial Only.

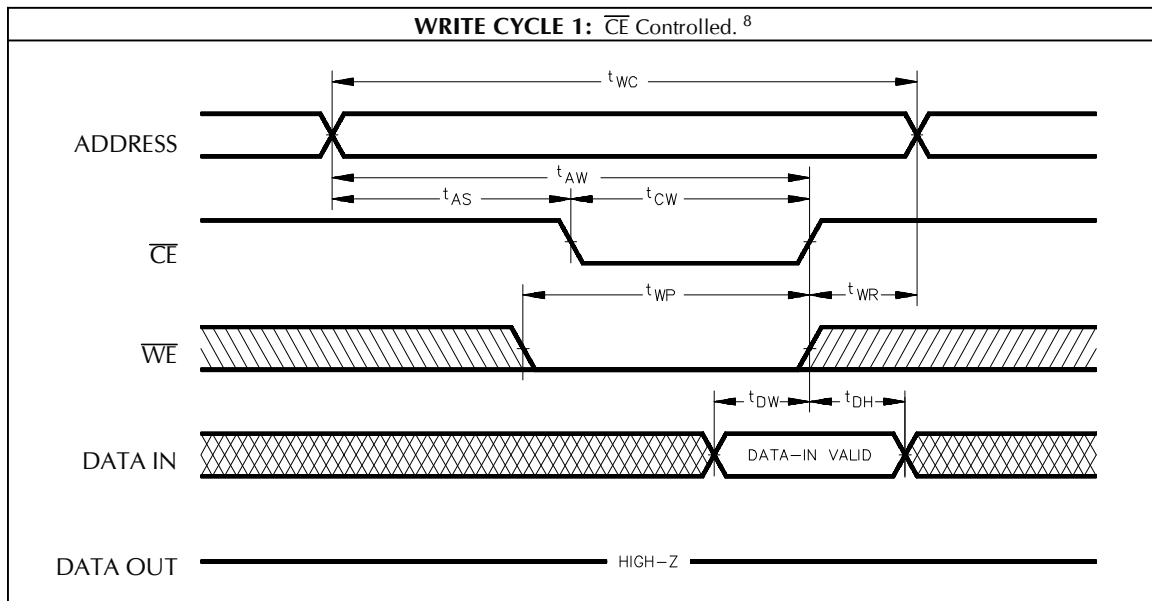
NOTE: t<sub>CO2</sub>, t<sub>LZ2</sub> and t<sub>HZ2</sub> apply to DPS256X16Cn3 version only.



AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE <sup>6,7</sup> : Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t <sub>WC</sub>	Write Cycle Time	20		25		30		35		45		ns
14	t <sub>AW</sub>	Address Valid to End of Write	15		20		25		30		40		ns
15	t <sub>CW</sub>	Chip Enable to End of Write	15		20		25		30		40		ns
16	t <sub>AS</sub>	Address Set-Up Time **	0		0		0		0		0		ns
17	t <sub>WP</sub>	Write Pulse Width	15		20		25		30		35		ns
18	t <sub>WR</sub>	Write Recovery Time	0		0		0		0		0		ns
19	t <sub>WHZ</sub>	Write Enable to Output in HIGH-Z <sup>4,5</sup>		8		10		12		15		20	ns
20	t <sub>DW</sub>	Data to Write Time Overlap	12		15		15		20		25		ns
21	t <sub>DH</sub>	Data Hold from Write Time	0		0		0		0		0		ns
22	t <sub>OW</sub>	Output Active from End of Write	3		3		3		3		3		ns

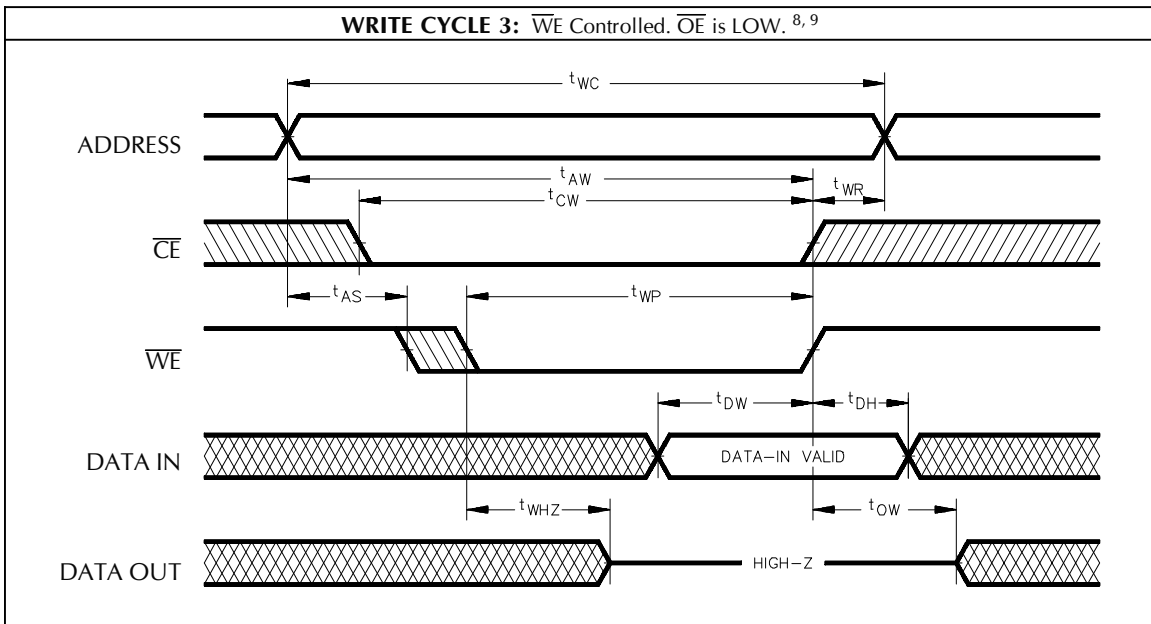
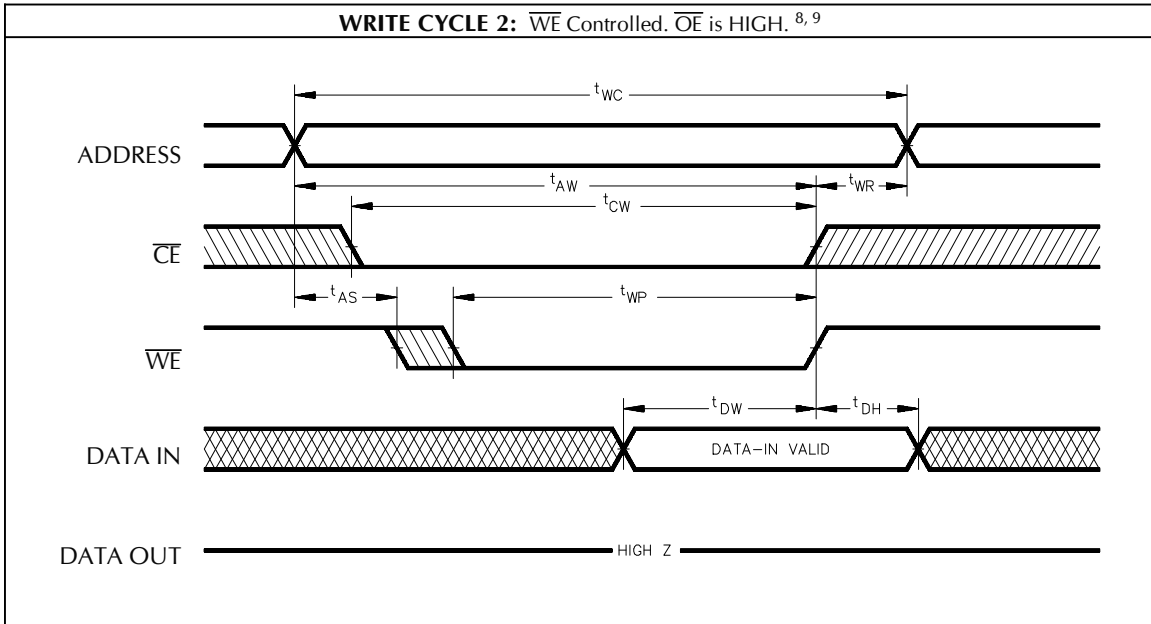
\* Available in Commercial Only.

\*\* Valid for both Read and Write Cycles.

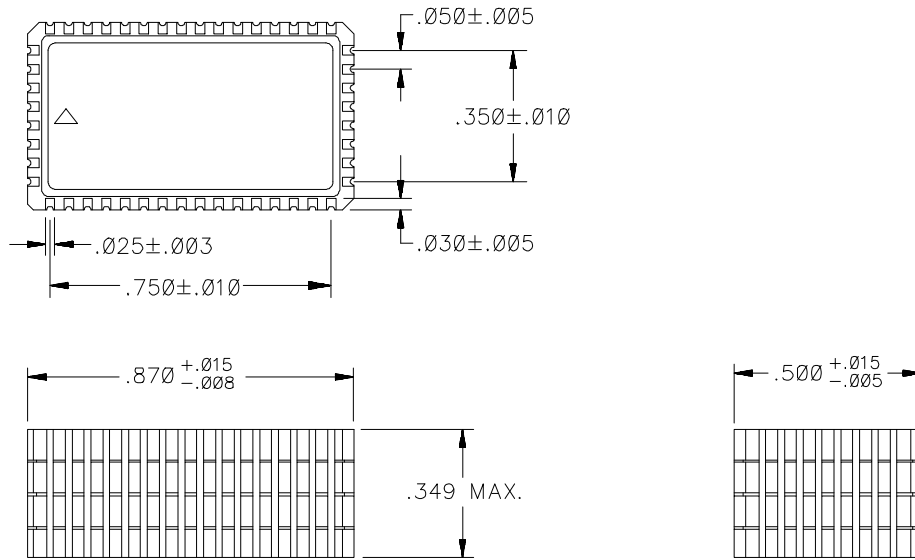


**NOTES:**

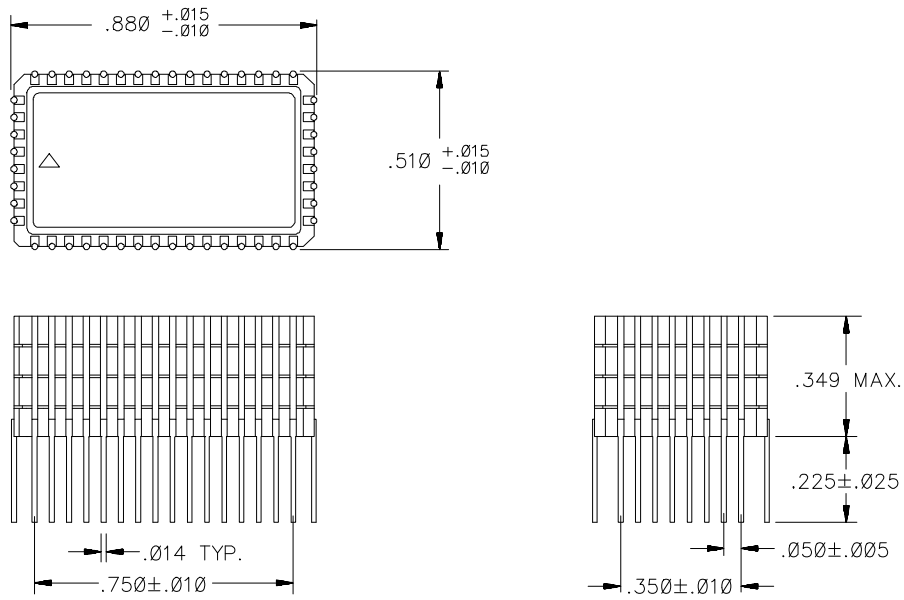
- All voltages are with respect to V<sub>SS</sub>.
- 2.0V min. for pulse width less than 20ns (V<sub>IL</sub> min. = -0.5V at DC level).
- Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- This parameter is guaranteed and not 100% tested.
- Transition is measured at the point of ±500mV from steady state voltage.
- When  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
- The outputs are in a high impedance state when  $\overline{WE}$  is LOW.
- SEL timing is the same as  $\overline{CE}$  timing (Valid for DPS256X16Cn3 only). The Waveform is inverted.
- Chip Enable and Write Enable can initiate and terminate WRITE Cycle.



(48 - PIN LEADLESS STACK) MECHANICAL DRAWING

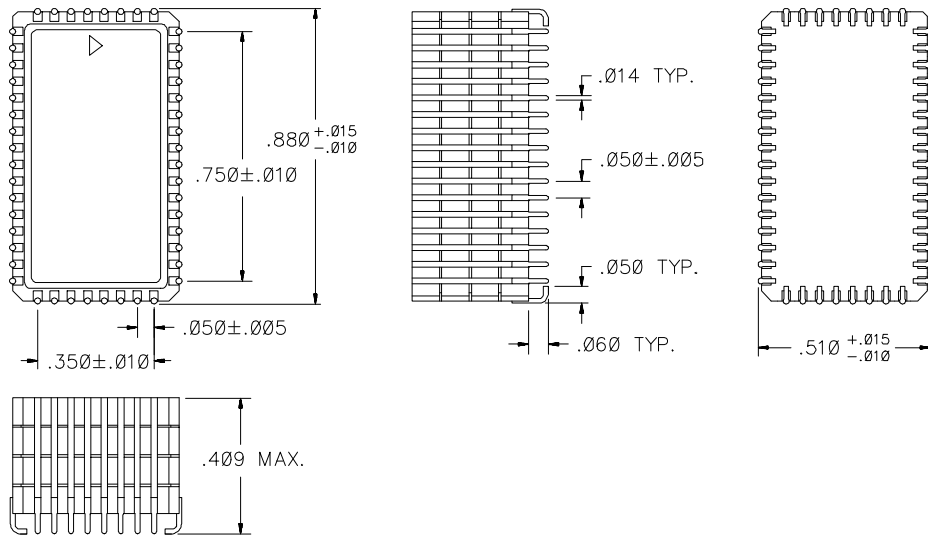


(48 - PIN STRAIGHT LEADED STACK) MECHANICAL DRAWING

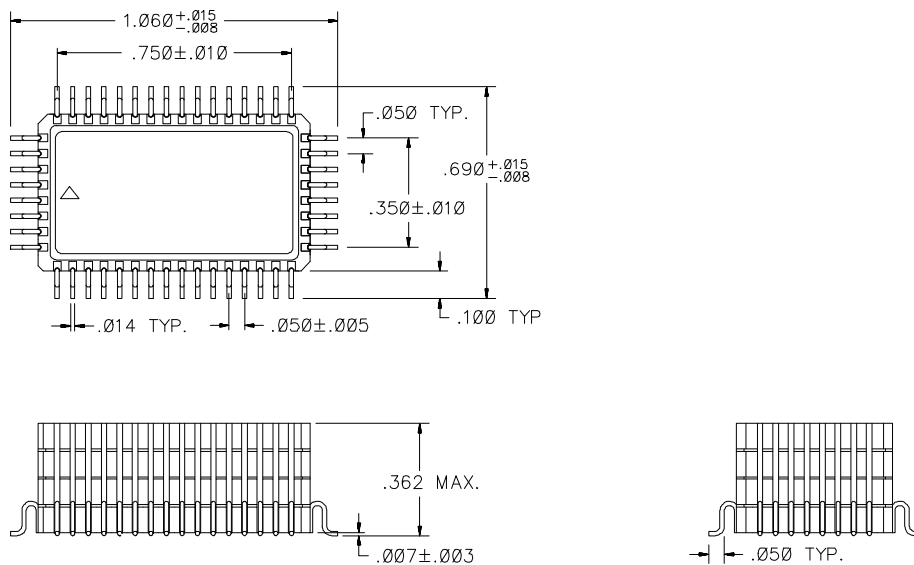


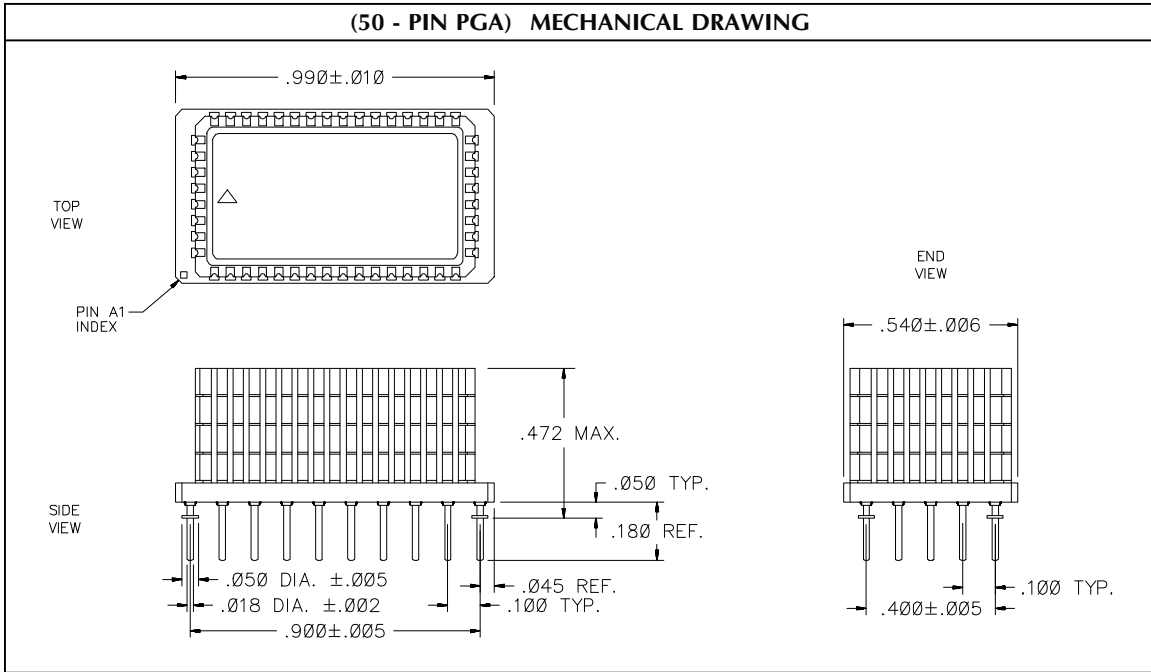


(48 - PIN "J" LEADED STACK) MECHANICAL DRAWING



(48 - PIN GULLWING LEADED STACK) MECHANICAL DRAWING





**ORDERING INFORMATION**

DP	S	256	X	16	X	X3	-XX	X		
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG.	PACKAGE	SPEED	GRADE		
									C	COMMERCIAL
									I	INDUSTRIAL
									M	MILITARY
									B	MIL-PROCESSED
									20	20ns (COMMERCIAL ONLY)
									25	25ns
									30	30ns
									35	35ns
									45	45ns
									A3	DENSE-STACK PGA (PIN GRID ARRAY)
									H3	GULLWING LEADED SLCC STACK
									I3	THRU-HOLE LEADED SLCC STACK
									J3	"J" LEADED SLCC STACK
									Y3	LEADLESS SLCC STACK
									B	HIGH SPEED / SINGLE CHIP ENABLE
									C	HIGH SPEED / DUAL CHIP ENABLE
										MODULE WITHOUT SUPPORT LOGIC
										CMOS SRAM DEVICES

**Dense-Pac Microsystems, Inc.**

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 (714) 898-0007 ♦ (800) 642-4477 (Outside CA) ♦ FAX: (714) 897-1772 ♦ <http://www.dense-pac.com>