This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

T-52-33-19

CY7C618

CYPRESS SEMICONDUCTOR

SBus DMA Controller

Features

- Supports two independent peripheral channels
- Supports packing and unpacking from 32-bit SBus to 16- or 8-bit data paths
- Byte, halfword, and word transfers on the SBus are supported as both master and slave
- Rerun acknowledgments are supported as both master and slave
- Support for access of SBus Fcode PROM is included

Introduction

The SBus DMA controller provides an SBus interface for peripheral controllers of subsystems such as the Ethernet and disk I/O. It provides two independent channels, one with a 16-bit data path and one with an 8-bit data path. (Refer to the Logic Block Diagram. The blocks contained within the dotted lines correspond to the logic described here.) Each channel can operate as either an SBus master or a slave.

The status of the DMA transfers in progress can be monitored and the progress of the transfer can be controlled by means of accessing status and control information on the DMA controller and the peripheral controllers, which is available at any time for SBus access by the CPU.

The two channels differ in their operation as SBus masters. The 16-bit channel, called the E channel, supports peripheral controllers that generate their own memory addresses for DMA, keep track of the state of the transfer in terms of bytes transferred, and so on. In other words, the Ethernet channel supports peripheral controllers that have their own memory bus master functionality. The E channel essentially acts as a sort of "lever arm" into the SBus by which the peripheral controllers' memory access cycles are converted into the protocol of the SBus. Addresses are extended from 24 to 32 bits and data is packed/unpacked from 16 to 32 bits.

In contrast, the 8-bit channel, called the D channel, supports the sort of peripheral controller that has no DMA circuitry itself but participates in the DMA transfer by means of a DMA request/DMA acknowledge signal handshake. Hence the D channel has full DMA master functionality, including address and byte counters. Eight- to 32-bit packing/unpacking is supported.

Logic Block Diagram