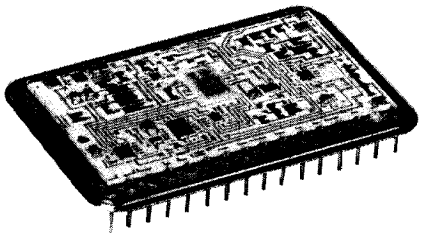
12 BIT HYBRID A/D CONVERTER
5μs Conversion Time; ±0.012% F.S. Range Linearity Error



FEATURES

- *PIN COMPATIBLE ADC-85 TYPE WITH WIDE TEMPERATURE RANGE AND LOWER POWER CONSUMPTION*
- *PIN SELECTABLE CODING:*
  Complementary Binary
  Complementary Offset Binary
  Complementary Two's Complement
- *VOLTAGE RANGES:*
  ±2.5V, ±5V, ±10V, 0 – 5V, 0 – 10V
- *BOTH SERIAL AND PARALLEL OUTPUT*
- *INTERNAL OR EXTERNAL CLOCK*
- *POWER CONSUMPTION 1.2W TYP*

DESCRIPTION

The ADH-8585 and ADH-8586 are complete in a 32 pin triple DIP hermetically sealed metal package and are pin compatible with other generic ADC-85 12 bit A/D converters. An advanced design using thin-film and MSI technologies results in conversion times of 10μsec for the ADH-8585 and 5μsec for the ADH-8586, corresponding to word rates of nearly 100 KHz and 200 KHz, respectively. Conversion times may be reduced to less than this by short cycling and increasing the internal clock rate if less resolution and accuracy are acceptable. Gain and offset errors can be trimmed to zero using two external potentiometers, making accuracy equal to the ±1/2 LSB linearity. The internal reference and internal clock are externally accessible, and an external clock may be used.

APPLICATIONS

Because of their high reliability, hermetically sealed metal cases, and wide operating temperature ranges, the ADH-8585 and ADH-8586 will meet the most demanding military and industrial requirements. Typical applications include data acquisition systems, automatic test equipment and electronic countermeasures systems. Standard processing at no added cost is based on MIL-STD-883, except for burn-in which is an option. These converters are excellent for remotely located and hard to access equipment where small size and high MTBF are critical.

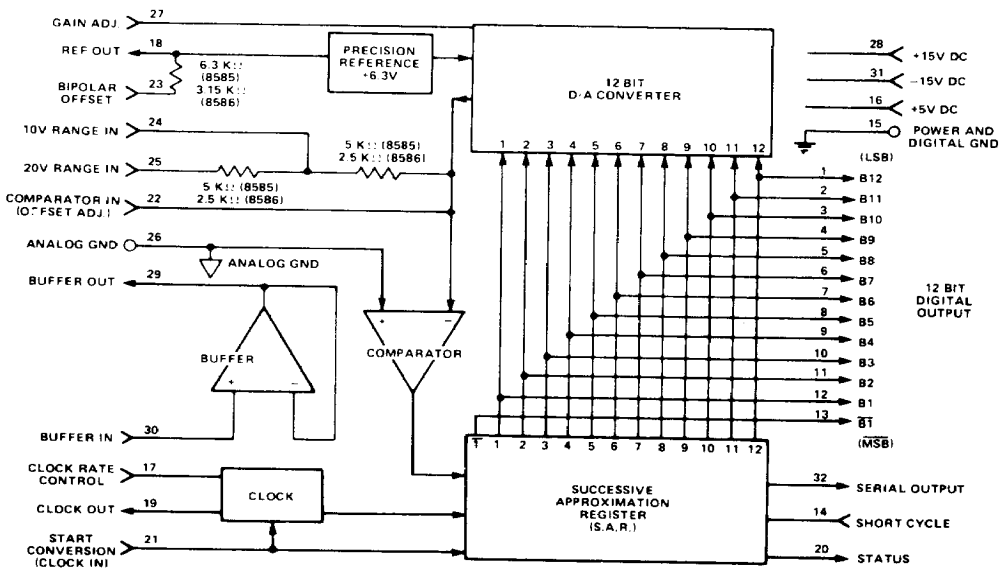


FIGURE 1. ADH-8585 AND ADH-8586 BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION AND BLOCK DIAGRAM

The main elements of the ADH-8585 and ADH-8586 as shown in the block diagram, Figure 1, are a voltage comparator, a 12 bit successive approximation register (S.A.R.), and a 12 bit digital to analog converter connected in a closed loop. The analog input and the D/A converter output are superimposed at the sum point of the comparator. Successive approximation is used to make the D/A output equal to the analog input. Conversions are initiated by an external START CONVERSION pulse, and a STATUS logic output indicates when a conversion has been completed and output data is available. A more detailed description of the closed loop operation can be found in the Background Information section for A/D converters in this catalog.

The 10V RANGE INPUT or 20V RANGE INPUT is connected to the analog input (depending on scaling) and the BIPOLAR OFFSET is used to select unipolar or bipolar operation. An input buffer amplifier is provided for higher input impedance, but its use has been made optional. The buffer amplifier must be allowed to settle before a conversion can be initiated.

The rate of the internal clock is determined by the voltage provided at the CLOCK RATE CONTROL input. When this input is connected to power ground, the internal clock rate is appropriate for the full accuracy 12 bit converter. However, it may be necessary to adjust the voltage to obtain the optimum clock rate.

The conversion rate can be increased by truncating the conversion at 10 or 8 bits using the SHORT CYCLE pin. Short cycling allows the clock to be speeded up. The internal clock rate can be increased by applying a more positive voltage to the CLOCK RATE CONTROL, thereby increasing the conversion time still further. It is also possible to use an external clock.

There are two grounds in the system. The analog ground for the analog input signal is designated by ⏚. The power supply ground, designated by ⏚, is also used as a ground for all logic signals. To minimize crosstalk, the analog and power grounds are not connected internally. They should be connected as directly as possible externally, preferably with a ground plane beneath the module.

INPUT SCALING AND OUTPUT CODING

There are five input voltage ranges, with pin connections as shown in Figure 2, Connections for Normal Operation. For unipolar input (ranges 0 – 5V or 0 – 10V) the output coding using bits 1 through 12 is complementary offset binary. For bipolar input (ranges ±2.5V, ±5V, or ±10V) the output coding is either complementary straight binary using bits 1 through 12, or complementary two's complement if bits 2 through 12 and bit 1 (the MSB complement) is used. The coding is described by the transition table in Figure 3. The analog input voltage levels shown in the left hand column should correspond to the transition points between the digital codes shown at the right.

SPECIFICATIONS

Typical values at +25°C case temperature and nominal power supply voltages

PARAMETER	UNITS	VALUE	
		10 BIT	12 BIT
RESOLUTION	Bits	10	12
ACCURACY AND DYNAMICS			
Linearity Error	% of F.S.R.	±0.048 max	±0.012 max
Linearity Error Tempco	ppm/°C	±5 max	±2 max
Gain Error (Trimmable to zero)	% of F.S.R.	±0.1 typ	±0.1 typ
Gain Error Tempco	ppm/°C	±25 max	±15 max
Offset (Trimmable to zero)			
Unipolar	% of F.S.R.	±0.05 typ	±0.05 typ
Bipolar	% of F.S.R.	±0.1 typ	±0.1 typ
Offset Tempco			
Unipolar	ppm/°C	±3 max	±3 max
Bipolar	ppm/°C	±10 max	±7 max
Diff. Linearity Error	LSB	±1	±1
		8585 / 8586	8585 / 8586
Conversion Time*	µs	6 max / 3 max	10 max / 5 max
Cycle Time*	µs	6.4 max / 3.2 max	10.5 max / 5.25 max
ANALOG INPUTS			
Input Ranges			
Unipolar	V	0 to +5, 0 to +10	
Bipolar	V	±2.5, ±5, ±10	
Max Voltage Without Damage	V	Two times full scale range	
Impedance (Direct Input)		8585 / 8586	
0 to +5V and ±2.5V	KΩ	2.5 typ / 1.25 typ	
0 to 10V and ±5V	KΩ	5 typ / 2.5 typ	
±10V	KΩ	10 typ / 5 typ	
Buffer Amplifier			
Impedance	MΩ	100 min	
Bias Current	nA	±100 typ, 250 max	
Setting Time (to .01% for 20V step)	µs	2 typ	
DIGITAL INPUT/OUTPUT (TTL COMPATIBLE)			
12 Bit Parallel Output		Positive logic, bits 1 through 12 plus MSB complement Drive capability 2 std TTL loads for 8585 5 std TTL loads for 8586 Unipolar coding: Complementary Binary Bipolar coding: Complementary Offset Binary or Complementary Two's Complement	
Serial Data Output		Non return to zero (NRZ), drive capability and coding same as for parallel output	
Start Conversion Input		Positive pulse, 50 ns min, trailing edge initiates conversion Loading is 1 std TTL load	
Status		Logic "1" during conversion, drops to "0" to indicate parallel data is available	
Drive Capability		2 TTL loads	
Internal Clock Output		Train of 13 positive pulses initiated by the Start Conversion trailing edge Drive capability is 2 std TTL loads Clock Frequency can be changed by pin programming or by external potentiometer adjustment	
INTERNAL REFERENCE OUTPUT			
Voltage Level	V	+6.3 ± 5%	
Current	mA	0.2 max for no degradation in specifications	
Voltage Tempco	ppm/°C	±20 max	

* The internal clock frequency is controlled by an externally applied voltage. The Conversion Time and Cycle Time values listed can be obtained by adjusting the clock voltage.

PARAMETER	UNITS	VALUE		
POWER SUPPLIES				
Supply Voltages	V	+15 ±5%	−15 ±5%	+5 ±5%
Max Voltage Without Damage	V	±18	±18	+7
Current				
8585	mA	35 typ 45 max	25 typ 35 max	50 typ 75 max
8586	mA	40 typ 50 max	30 typ 45 max	110 typ 150 max
Power Supply Sensitivity	%FSR/%PS	0.002	±0.002	±0.001
THERMAL CHARACTERISTICS				
Temperature Ranges (Case)				
Operating				
1 Option	C	−55 to +125		
3 Option	C	−25 to +85		
Storage	C	−55 to +135		
Thermal Impedances				
Case to Air	C/Watt	θ_{CA} = 15		
Junction to Case	C/Watt	θ_{JC} = 2		
PHYSICAL CHARACTERISTICS				
Type of Package		Metal case, hermetically sealed, 32 pin triple DIP		
Size	inches	1.75 x 1.05 x 0.22 (4.45 x 2.67 x 0.56 cm)		
Weight	oz	0.67 typ (19 g)		

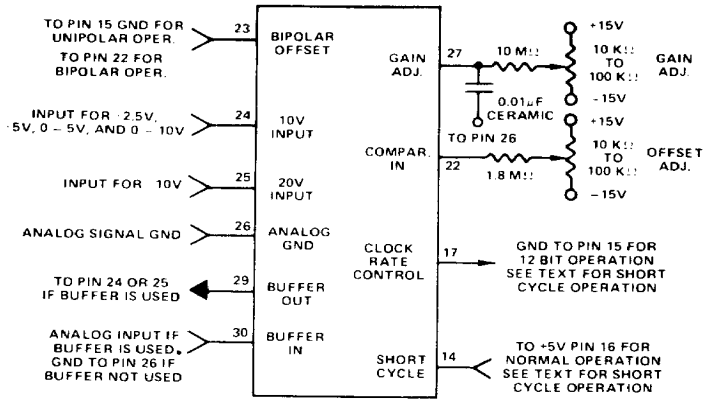


FIGURE 2. CONNECTIONS FOR NORMAL OPERATION

TIMING DIAGRAM AND EXTERNAL CLOCK

The timing for normal 12 bit operation of the ADH-8585 and ADH-8586 is shown in Figure 4. The trailing edge of the START CONVERSION pulse starts the conversion by initiating the first of the 13 equal positive pulses of the internal clock. The leading edge of the first clock pulse then causes the STATUS to go to logic "1" and also causes the first bit to be tried. The leading edge of the second clock pulse causes Bit 2 to be tried, and Bit 1 then becomes valid. The twelfth clock pulse causes Bit 12 to be tried. Bit 12 becomes valid after the leading edge of the clock pulse 13, and the STATUS then drops to logic "0" to indicate that the conversion has been completed.

The SERIAL DATA OUTPUT is a non return to zero type (NRZ). Data for each bit becomes valid at the same time as the corresponding parallel data for the same bit, and remains valid for one clock cycle. A recommended way to clock data from the SERIAL OUTPUT is to use the trailing edge of each clock pulse to shift the data into a twelve bit shift register.

An EXTERNAL CLOCK can also be used as indicated in Figure 4. If the START CONVERSION input is at logic "1" at a time when any internal clock would normally be initiated, the clock is turned off and neither that pulse nor subsequent pulses will exist. Because of this feature an external clock with negative pulses can be applied to the Start Conversion input , pin 21. The leading edge of the first negative external clock pulse turns on the internal clock and Bit 1 is tried. If the external clock pulse is shorter than 200 ns, the Start Conversion input will be at logic "1" at the time when the second internal clock would normally be initiated, so the internal clock will turn off. The external clock is then free to initiate the trial of Bit 2 at any time. The only limitation on the rate of the external clock is that it must be no faster than twice the rate of the internal clock. The clock rate control could be used to adjust the internal clock rate to meet this criterion.

SHORT CYCLING AND CLOCK RATE CONTROL

The minimum conversion time and minimum cycle time depend on the number of bits tried and on the clock period. The clock period must be long enough to allow the comparator to settle out. The ADH-8586 is twice as fast as the ADH-8585 because its comparator settles faster at the expense of lower input impedance.

The number of bits tried can be reduced for both units changing the SHORT CYCLE pin connection. Pin 14 is connected to the next higher bit than the number of bits to be tried. For instance, for 10 bits, connect pin 14 to pin 2 (bit 11). For 8 bits, connect pin 14 to pin 4 (bit 9).

When fewer bits are tried, it is possible to increase the clock rate because less accuracy is required. For full 12 bit operation when no particular or optimum conversion time is required, the Clock Rate Control, pin 17, is usually grounded as shown in Figure 2. In the same way, when rates are not critical, pin 17 can be connected to +5V for 10 bit operation and +15V for 8 bit operation. Optimum clock rates will generally require fine adjustment of the clock voltage. The approximate clock rates with the three standard voltage levels are:

Pin 17 Voltage	Approximate Clock Rate	
	ADH-8585	ADH-8586
0V	1.3 MHz	2.6 MHz
+5V	2 MHz	4 MHz
+15V	2.5 MHz	5 MHz

If both short cycling and pin-programmed clock rate control are used to increase the conversion rate, the following nominal conversion times are obtained for 10 and 8 bits:

Resolution	Pin 17 Voltage	Conversion Time	
		ADH-8585	ADH-8586
12 Bits	0V	10μs	5μs
10 Bits	+5V	6μs	3μs
8 Bits	+15V	4μs	2μs

TRANSITION VALUE		DIGITAL BIT OUTPUTS											
UNIPOLAR	BIPOLAR	MSB											LSB
COMPLEMENTARY BINARY	COMPLEMENTARY OFFSET BINARY	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12
+F.S. – 3/2 LSB	+F.S. – 3/2 LSB	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0
+3/4 F.S. – 1/2 LSB	+1/2 F.S. – 1/2 LSB	0	0	1	1	1	1	1	1	1	1	1	1
		0	1	0	0	0	0	0	0	0	0	0	0
+1/2 F.S. + 1/2 LSB	+1/2 LSB	0	1	1	1	1	1	1	1	1	1	1	0
		0	1	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. – 1/2 LSB	–1/2 LSB	0	1	1	1	1	1	1	1	1	1	1	1
		1	0	0	0	0	0	0	0	0	0	0	0
+1/4 F.S. + 1/2 LSB	–1/2 F.S. + 1/2 LSB	1	0	1	1	1	1	1	1	1	1	1	0
		1	0	1	1	1	1	1	1	1	1	1	1
+3/2 LSB	–F.S. + 3/2 LSB	1	1	1	1	1	1	1	1	1	1	0	1
		1	1	1	1	1	1	1	1	1	1	1	0
+1/2 LSB	–F.S. + 1/2 LSB	1	1	1	1	1	1	1	1	1	1	1	0
		1	1	1	1	1	1	1	1	1	1	1	1

3A. Theoretical transition values for Complementary Binary and Complementary Offset Binary coding. For Complementary Two's Complement coding, all values are the same as for Complementary Offset Binary, except that the MSB is reversed (MSB bits "0" become "1" and "1" become "0").

VOLTAGE RANGE	FULL SCALE (VOLTS)	1/2 LSB (VOLTS)
±2.5V	2.50000	0.00061
±5V	5.00000	0.00122
±10V	10.00000	0.00244
0 to +5V	5.00000	0.00061
0 to +10V	10.00000	0.00122

3B. Full Scale (F.S.) and 1/2 LSB for 12 bit accuracy.

FIGURE 3. THEORETICAL TRANSITION VALUES

Resolution	+V	R	Conversion Time 8585	Conversion Time 8586
12 Bits	+5V	2 KΩ	6.8 – 10μs	3.5 – 5μs
10 Bits	+15V	5 KΩ	4.0 – 6μs	2.0 – 3.0μs
8 Bits	+15V	5 KΩ	3.5 – 6μs	1.75 – 3.0μs

Note that if the clock rate is increased to a value greater than that specified for the number of bits required, the linearity error will be substantially increased.

The CLOCK RATE CONTROL can also be connected to negative voltage as large as –15V, and this will decrease the clock rate.

The clock rates and conversion times listed are nominal values. To adjust the clock rate accurately, pin 17 may be connected to a voltage divider as shown in figure 5. R is a multi-turn trim potentiometer with a tempco of ±100 ppm/°C or less. The range of adjustment of the clock rate will be nominally as follows:

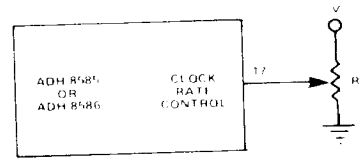


FIGURE 5. OPTIONAL CLOCK RATE FINE ADJUSTMENT

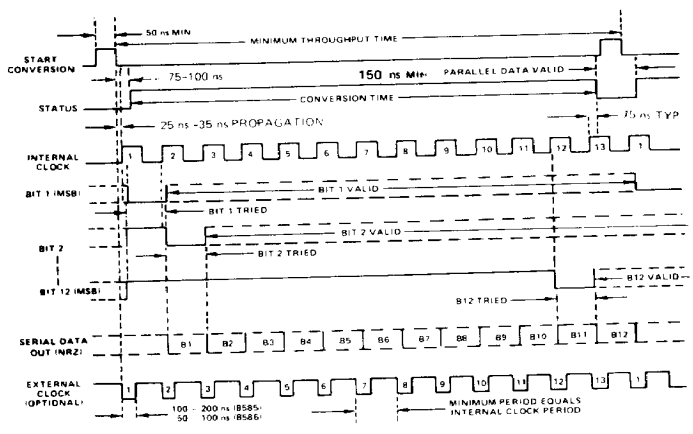


FIGURE 4. ADH-8585 AND ADH-8586 TIMING DIAGRAM

INPUT CONFIGURATIONS

INPUT RANGE:	0 to +5V	0 to +10V	±2.5V	±5V	±10V
NORMAL INPUT (Jumpers)					
Connect Pin 23	26	26	22	22	22
Connect Pin 25	22	–	22	–	Input
Connect Pin 30	26	26	26	26	26
Connect Input to Pin	24	24	24	24	25
BUFFERED INPUT (Jumpers)					
Connect Pin 23	26	26	22	22	22
Connect Pin 25	22	–	22	–	29
Connect Pin 29	24	24	24	24	25
Connect Input to Pin	30	30	30	30	30

OFFSET AND GAIN TRIM

The gain and offset of the ADH-8585 and ADH-8586 are factory trimmed to the values listed in the specifications table. Both errors can be trimmed to zero in the final application by using the potentiometer adjustment circuits shown in Figure 2.

To reduce noise, the GAIN ADJUST, pin 27, should be bypassed with an 0.01μF ceramic capacitor to analog ground as shown in Figure 2 even if no gain trim potentiometers are installed.

ACCURACY TESTING

The accuracies of the ADH-8585 and ADH-8586 are specified by their linearity error, gain, offset, and differential linearity. The relationships between these terms and the measured bit transitions listed in Figure 3 are discussed in the Bacground Information section for A/D converters in this catalog.

The arrangement shown in Figure 6 may be used to measure the bit transitions. Offset trim, gain trim, and other standard connections are not shown. Shielded twisted pair cable is used to connect the Precision Voltage Standard, and each of the twelve bits requires its own LED indicator. The inverting register is used to increase the duty cycle of the LSB bits since they are held at logic "1" during most of the timing cycle as indicated in the timing diagram. The NOT outputs (N) from the register are used so that a lighted LED will represent logic "1". Readings should be taken with the converter energized, in thermal equilibrium at 25°C, and after a warm-up time of 5 minutes. The Pulse Generator can be set at any frequency up to the maximum allowed for the converter. The power supply voltages should be at their nominal values.

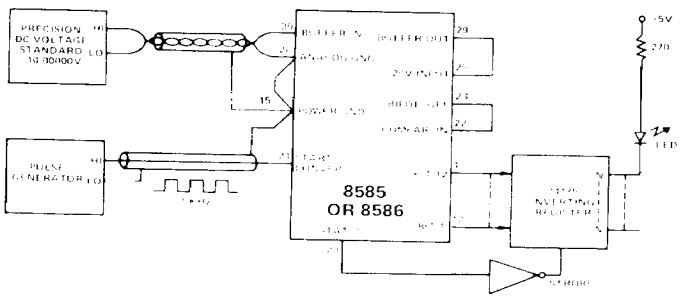


FIGURE 6. CIRCUIT FOR TESTING ACCURACY

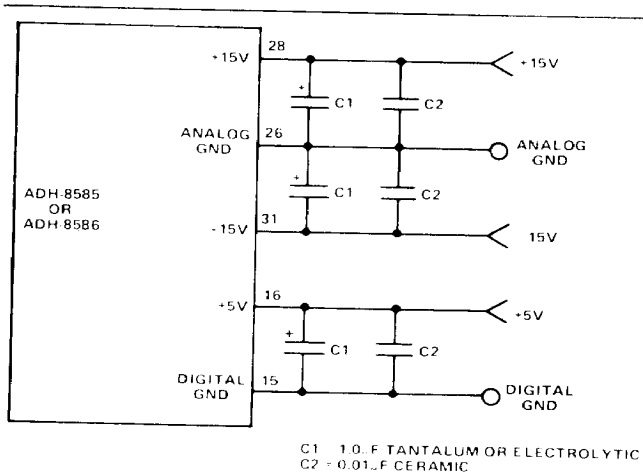


FIGURE 7. POWER SUPPLY DECOUPLING CAPACITORS

The suggested test procedure is as follows:

(1) Trim the offset by sweeping the input through the transition at − F.S. + 1/2 LSB in the transition value table, Figure 3. Adjust the Offset potentiometer until there is a 50% dither of the LSB.

(2) Trim the gain by sweeping the input through the transition at all bits ON in Figure 3 (+ F.S. + 3/2 LSB for bipolar coding). Adjust the Gain potentiometer for a 50% dither of the LSB.

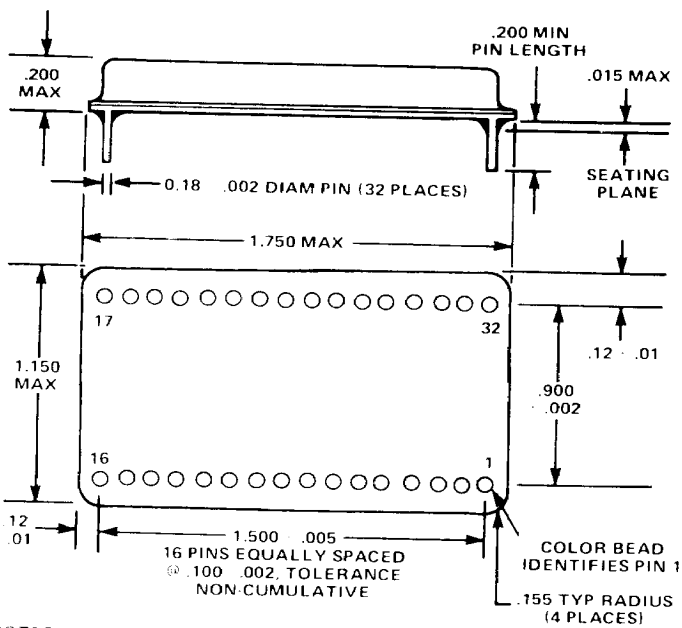
(3) Repeat steps (1) and (2) in case there is a slight interaction between the offset and gain trims.

(4) Measure the input voltage levels at which other transitions occur. The differences between these voltages and the theoretical values will be taken within ±1/2LSB.

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	17	CLOCK RATE CNTL
2	BIT 11	18	REF. OUT (+6.2V)
3	BIT 10	19	CLOCK OUT
4	BIT 9	20	STATUS
5	BIT 8	21	START CONVERT
6	BIT 7	22	COMPARATOR IN
7	BIT 6	23	BIPOLAR OFFSET
8	BIT 5	24	10V RANGE
9	BIT 4	25	20V RANGE
10	BIT 3	26	ANALOG GND
11	BIT 2	27	GAIN ADJ
12	BIT 1 (MSB)	28	+15 SUPPLY
13	$\overline{\text{BIT 1 (MSB)}}$	29	BUFFER OUT
14	SHORT CYCLE	30	BUFFER IN
15	DIG. GND	31	-15V SUPPLY
16	+5V SUPPLY	32	SERIAL OUT

MECHANICAL OUTLINE
32 PIN TRIPLE DIP



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

POWER SUPPLY DECOUPLING

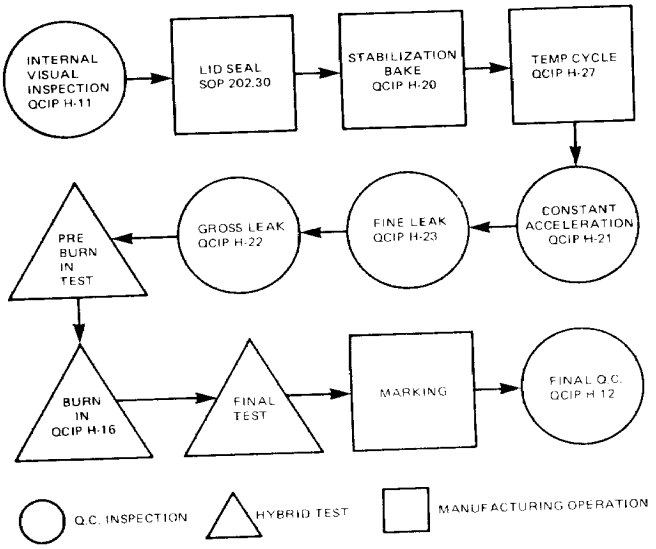
The power supplies should be bypassed with capacitors as shown in Figure 7 to assure noise free operation. These capacitors should be located as close to the converter as possible. The 0.01μF ceramic capacitors improve high frequency performance.

RELIABILITY

The use of MSI and thin film resistance networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All DDC hybrids are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on requirements of Method 5004/5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 1,600,000 hours, Ground Fixed, at 25°C case temperature.

DDC processing to MIL-STD-883 is as follows:



ORDERING INFORMATION

ADH-8585 – 12 – 1 – 883B

- 883B: MIL-STD-883 Processing: 883B = Conforms to MIL-STD-883B, DDC procedures. Blank = Same, except burn-in is omitted.
- 1: Operating Temperature Ranges (Case): 1 = –55°C to +125°C; 3 = –25°C to +85°C
- 12: Linearity: 12 = 12 bits (±.012% F.S.R.); 10 = 10 bits (±.048% F.S.R.)
- 8585: Model: 8585 = 10μs conversion time for 12 bits; 8586 = 5μs conversion time for 12 bits

MIL–STD–883 REQUIREMENT	DDC CONTROLLING PROCEDURES	TITLE	REMARKS
2017	QCIP H–11	Internal Visual	
None	SOP 202 30	Lid Seal	DDC Procedure
1008.1	QCIP H–20	Stabilization Bake	Condition B 24 hrs @ 125°C
1010.1	QCIP H–27	Temperature Cycling	Condition B 10 Cycles +25, –55, +25, +125°C
2001.1	QCIP H–21	Constant Acceleration	5000g Condition A
1014.1	QCIP H–23	Fine Leak	883 Test Condition A
	QCIP H–22	Gross Leak	883 Test Condition C
None	QCIP H–16	Burn In	DDC Procedure
2009.1	QCIP H–12	Final QC	External Visual