REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change package designation and add case outline figure. - jak	00-04-11	Monica L. Poelking
B	Add device type 02. - jak	00-05-30	Monica L. Poelking
C	Correct supply voltage nomenclature to comply with device characterization. Correct dimension A minimum values for Case Outline X in table of Figure 1. Update boilerplate to latest MIL-PRF-38535 requirements. - CFS	01-03-06	Thomas M. Hess
D	Add device type 03. - CFS	02-05-10	Thomas M. Hess

REV	D	D	D	D	D	D	D	D	D											
SHEET	35	36	37	38	39	40	41	42	43											
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Charles F. Saffle, Jr.

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
Charles F. Saffle, Jr.

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
99-05-10

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, SCHMITT 16-BIT BIDIRECTIONAL MULTI-PURPOSE TRANSCEIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

AMSC N/A

REVISION LEVEL
D

SIZE	CAGE CODE	
A	**67268**	**5962-98580**

SHEET
1 OF 43

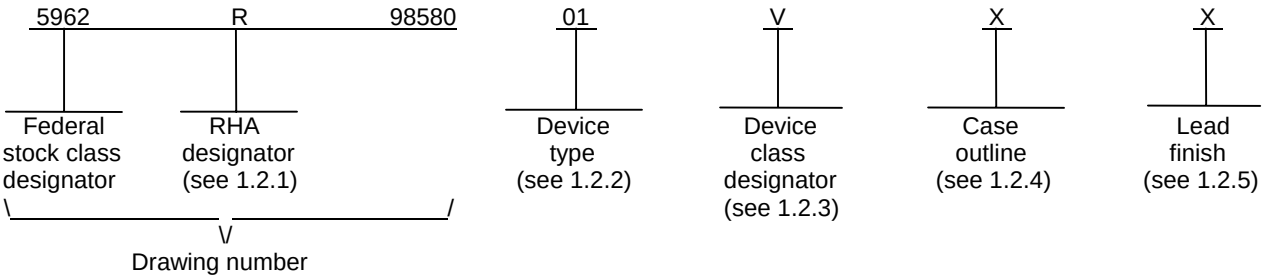
DSCC FORM 2233
APR 97

5962-E407-02

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS164245S	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs and cold sparing
02	54ACS164245S 1/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, and extended voltage range
03	54ACS164245S 1/ 2/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, extended voltage range, and extended industrial temperature range of -40°C to +125°C

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Flat pack

1/ Device types 02 and 03 have an extended voltage range.
2/ Device type 03 has an extended industrial temperature range of -40°C to +125°C.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage ranges (V_{DD}):
5.0 V supply (V_{DD1}) ..... -0.3 V dc to +6.0 V dc
3.3 V supply (V_{DD2}) ..... -0.3 V dc to +6.0 V dc
DC input voltage range (V_{IN}): 4/
A port ..... -0.3 V dc to V_{DD1} + 0.3 V dc
B port ..... -0.3 V dc to V_{DD1} + 0.3 V dc
DC output voltage range (V_{OUT}):
A port ..... -0.3 V dc to V_{DD1} + 0.3 V dc
B port ..... -0.3 V dc to V_{DD1} + 0.3 V dc
DC input current, any one input (I_{IN}):
A port ..... ±10 mA
B port ..... ±10 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C
Maximum power dissipation at T_A = +55°C (in still air) (P_D) ..... 1.0 W 5/

1.4 Recommended operating conditions. 2/ 3/ 6/

Supply voltage range (V_{DD}):
(V_{DD1}) Device type 01 ..... +4.5 V dc to +5.5 V dc
or 3.13 V dc to 3.6 V dc
(V_{DD1}) Device types 02 and 03 ..... +4.5 V dc to +5.5 V dc
or 3.0 V dc to 3.6 V dc
(V_{DD2}) Device type 01 ..... +3.13 V dc to +3.6 V dc
or +4.5 V dc to +5.5 V dc
(V_{DD2}) Device types 02 and 03 ..... +3.00 V dc to +3.6 V dc
or +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{DD1}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{DD1}
Case operating temperature range (T_C): (Device types 01 and 02) ..... -55°C to +125°C
(Device type 03) ..... -40°C to +125°C
Maximum input rise and fall time at V_{DD1} = 4.5 V (t_r, t_f) ..... 1 ns/V 7/

1.5 Radiation features. 8/

Maximum total dose available (dose rate = 50 - 300 rads (Si)/s) ..... 1×10^5 Rads (Si)
Single event phenomenon (SEP) effective linear energy
threshold (LET). No upsets (see 4.4.4.4) ..... > 80 MeV/(mg/cm^2)
Single event latch-up ..... > 120 MeV/(mg/cm^2)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C for device types 01 and 02, -40°C to +125°C for device type 03.
4/ For cold spare mode (V_{DD} = V_{SS}), VIN may be –0.3V to the maximum recommended operating V_{DD} + 0.3V.
5/ The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils
6/ Unused inputs must be held high or low to prevent them from floating.
7/ Derate system propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.
8/ Radiation testing is performed on the standard evaluation circuit.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Irradiation test connections. The irradiation test connections shall be as specified in table III.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified		Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
							Min	Max	
Schmitt trigger positive going threshold	V_{T+}	A Port = 3.3V		01	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3		$0.7V_{DD2}$	V
			M, D, P, L, R 5/	01		1		$0.7V_{DD2}$	
		A Port = 3.3V		02, 03	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3		$0.7V_{DD2}$	
			M, D, P, L, R 5/	02, 03		1		$0.7V_{DD2}$	
		A Port = 5.0V		All	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	1, 2, 3		$0.7V_{DD2}$	
			M, D, P, L, R 5/	All		1		$0.7V_{DD2}$	
		B Port = 3.3V		01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	
			M, D, P, L, R 5/	01		1		$0.7V_{DD1}$	
		B Port = 3.3V		02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	
			M, D, P, L, R 5/	02, 03		1		$0.7V_{DD1}$	
		B Port = 5.0V		01	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	
			M, D, P, L, R 5/	01		1		$0.7V_{DD1}$	
		B Port = 5.0V		02, 03	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	
			M, D, P, L, R 5/	02, 03		1		$0.7V_{DD1}$	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified		Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
							Min	Max	
Schmitt trigger negative going threshold	V_{T-}	A Port = 3.3V		01	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	$0.3V_{DD2}$		V
			M, D, P, L, R 5/	01		1	$0.3V_{DD2}$		
		A Port = 3.3V		02, 03	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	$0.3V_{DD2}$		
			M, D, P, L, R 5/	02, 03		1	$0.3V_{DD2}$		
		A Port = 5.0V		All	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	1, 2, 3	$0.3V_{DD2}$		
			M, D, P, L, R 5/	All		1	$0.3V_{DD2}$		
		B Port = 3.3V		01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		
			M, D, P, L, R 5/	01		1	$0.3V_{DD1}$		
		B Port = 3.3V		02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		
			M, D, P, L, R 5/	02, 03		1	$0.3V_{DD1}$		
		B Port = 5.0V		01	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		
			M, D, P, L, R 5/	01		1	$0.3V_{DD1}$		
		B Port = 5.0V		02, 03	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		
			M, D, P, L, R 5/	02, 03		1	$0.3V_{DD1}$		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified		Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
							Min	Max	
Schmitt trigger range of hysteresis	V_H 6/	A Port = 3.3V		01	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	0.4		V
			M, D, P, L, R 5/	01		1	0.4		
		A Port = 3.3V		02, 03	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	0.4		
			M, D, P, L, R 5/	02, 03		1	0.4		
		A Port = 5.0V		All	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	1, 2, 3	0.6		
			M, D, P, L, R 5/	All		1	0.6		
		B Port = 3.3V		01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	0.4		
			M, D, P, L, R 5/	01		1	0.4		
		B Port = 3.3V		02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	0.4		
			M, D, P, L, R 5/	02, 03		1	0.4		
		B Port = 5.0V		01	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	0.6		
			M, D, P, L, R 5/	01		1	0.6		
		B Port = 5.0V		02, 03	V_{DD1} =4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	0.6		
			M, D, P, L, R 5/	02, 03		1	0.6		
Input current high	I_{IH} 7/	A Port = 3.3V For input under test, $V_{IN} = V_{DD2}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}		All	V_{DD1} = 5.5 V, V_{DD2} = 3.6 V	1, 2, 3		3.0	µA
			M, D, P, L, R 5/	All		1		3.0	
		A Port = 5.0V For input under test, $V_{IN} = V_{DD2}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}		All	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1, 2, 3		3.0	
			M, D, P, L, R 5/	All		1		3.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
Input current high	I_{IH} 7/	B Port = 3.3V For input under test, $V_{IN} = V_{DD1}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} =3.6 V, V_{DD2} = 3.6 V	1, 2, 3		3.0	µA
		M, D, P, L, R 5/	All		1		3.0	
		B Port = 5.0V For input under test, $V_{IN} = V_{DD1}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} =5.5 V, V_{DD2} = 3.6 V	1, 2, 3		3.0	
		M, D, P, L, R 5/	All		1		3.0	
Input current low	I_{IL} 7/	A Port = 3.3V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} =5.5 V, V_{DD2} = 3.6 V	1, 2, 3	-1.0		µA
		M, D, P, L, R 5/	All		1	-1.0		
		A Port = 5.0V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1, 2, 3	-1.0		
		M, D, P, L, R 5/	All		1	-1.0		
		B Port = 3.3V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} = 3.6 V, V_{DD2} = 3.6 V	1, 2, 3	-1.0		
		M, D, P, L, R 5/	All		1	-1.0		
		B Port = 5.0V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} = 3.6 V	1, 2, 3	-1.0		
		M, D, P, L, R 5/	All		1	-1.0		
Input current cold spare mode	I_{CS}	A Port = B Port = 5.5 V = V_{IN} DIRn = 5.5V, $\overline{OE}$n = 5.5V	All	V_{DD1} = 0.0 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	µA
		M, D, P, L, R 5/	All		1	-1.0	5.0	
		A Port = B Port = 5.5 V = V_{IN} DIRn = 0.0V, $\overline{OE}$n = 5.5V	All	V_{DD1} = 0.0 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	
		M, D, P, L, R 5/	All		1	-1.0	5.0	
		A Port = B Port = 5.5 V = V_{IN} DIRn = 5.5V, $\overline{OE}$n = 0.0V	All	V_{DD1} = 0.0 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	
		M, D, P, L, R 5/	All		1	-1.0	5.0	
		A Port = B Port = 5.5 V = V_{IN} DIRn = 0.0V, $\overline{OE}$n = 0.0V	All	V_{DD1} = 0.0 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	
		M, D, P, L, R 5/	All		1	-1.0	5.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
Low level output voltage	V_{OL1} 8/	A Port = 3.3V, I_{OL} = 8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	01	V_{DD1} =4.5 V, V_{DD2} = 3.13 V	1, 2, 3		0.5	V
		M, D, P, L, R 5/	01		1		0.5	
		A Port = 3.3V, I_{OL} = 8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	02, 03	V_{DD1} =4.5 V, V_{DD2} = 3.0 V	1, 2, 3		0.5	
		M, D, P, L, R 5/	02, 03		1		0.5	
		A Port = 5.0V, I_{OL} = 8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} =4.5 V, V_{DD2} = 4.5 V	1, 2, 3		0.4	
		M, D, P, L, R 5/	All		1		0.4	
		B Port = 3.3V, I_{OL} = 8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} =3.13 V, V_{DD2} = 3.13 V	1, 2, 3		0.5	
		M, D, P, L, R 5/	01		1		0.5	
		B Port = 3.3V, I_{OL} = 8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1} =3.0 V, V_{DD2} = 3.0 V	1, 2, 3		0.5	
		M, D, P, L, R 5/	02, 03		1		0.5	
		B Port = 5.0V, I_{OL} = 8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3		0.4	
		M, D, P, L, R 5/	01		1		0.4	
		B Port = 5.0V, I_{OL} = 8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3		0.4	
		M, D, P, L, R 5/	02, 03		1		0.4	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
Low level output voltage	V_{OL2} 9/	A Port = 3.3V, I_{OL} = 100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3		0.2	V
		M, D, P, L, R 5/	01		1		0.2	
		A Port = 3.3V, I_{OL} = 100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	02, 03	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3		0.2	
		M, D, P, L, R 5/	02, 03		1		0.2	
		A Port = 5.0V, I_{OL} = 100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 4.5 V, V_{DD2} = 4.5 V	1, 2, 3		0.2	
		M, D, P, L, R 5/	All		1		0.2	
		B Port = 3.3V, I_{OL} = 100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1}= 3.13 V, V_{DD2} = 3.13 V	1, 2, 3		0.2	
		M, D, P, L, R 5/	01		1		0.2	
		B Port = 3.3V, I_{OL} = 100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1}= 3.0 V, V_{DD2} = 3.0 V	1, 2, 3		0.2	
		M, D, P, L, R 5/	02, 03		1		0.2	
		B Port = 5.0V, I_{OL} = 100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3		0.2	
		M, D, P, L, R 5/	01		1		0.2	
		B Port = 5.0V, I_{OL} = 100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3		0.2	
		M, D, P, L, R 5/	02, 03		1		0.2	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
High level output voltage	V_{OH1} 8/	A Port = 3.3V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD2} – 0.9V		V
		M, D, P, L, R 5/	01		1	V_{DD2} – 0.9V		
		A Port = 3.3V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	02, 03	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD2} – 0.9V		
		M, D, P, L, R 5/	02, 03		1	V_{DD2} – 0.9V		
		A Port = 5.0V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 4.5 V, V_{DD2} = 4.5 V	1, 2, 3	V_{DD2} – 0.7V		
		M, D, P, L, R 5/	All		1	V_{DD2} – 0.7V		
		B Port = 3.3V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} =3.13 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD1} – 0.9V		
		M, D, P, L, R 5/	01		1	V_{DD1} – 0.9V		
		B Port = 3.3V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1} =3.0 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD1} – 0.9V		
		M, D, P, L, R 5/	02, 03		1	V_{DD1} – 0.9V		
		B Port = 5.0V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD1} – 0.7V		
		M, D, P, L, R 5/	01		1	V_{DD1} – 0.7V		
		B Port = 5.0V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD1} – 0.7V		
		M, D, P, L, R 5/	02, 03		1	V_{DD1} – 0.7V		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
High level output voltage	V_{OH2} 9/	A Port = 3.3V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD2} - 0.2V		V
		M, D, P, L, R 5/	01		1	V_{DD2} - 0.2V		
		A Port = 3.3V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	02, 03	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD2} - 0.2V		
		M, D, P, L, R 5/	02, 03		1	V_{DD2} - 0.2V		
		A Port = 5.0V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 4.5 V, V_{DD2} = 4.5 V	1, 2, 3	V_{DD2} - 0.2V		
		M, D, P, L, R 5/	All		1	V_{DD2} - 0.2V		
		B Port = 3.3V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} =3.13 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD1} - 0.2V		
		M, D, P, L, R 5/	01		1	V_{DD1} - 0.2V		
		B Port = 3.3V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1} =3.0 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD1} - 0.2V		
		M, D, P, L, R 5/	02, 03		1	V_{DD1} - 0.2V		
		B Port = 5.0V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD1} - 0.2V		
		M, D, P, L, R 5/	01		1	V_{DD1} - 0.2V		
		B Port = 5.0V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD1} - 0.2V		
		M, D, P, L, R 5/	02, 03		1	V_{DD1} - 0.2V		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
Output current (Sink)	I_{OL} 10/	A Port = 3.3V $V_{IN} = V_{SS}$ $V_{OL} = 0.5\ V$	01	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.13\ V$	1, 2, 3	8.0		mA
			02, 03	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.0\ V$	1, 2, 3	8.0		
		A Port = 5.0V $V_{IN} = V_{SS}$ $V_{OL} = 0.4\ V$	All	$V_{DD1} = 4.5\ V$, $V_{DD2} = 4.5\ V$	1, 2, 3	8.0		
		B Port = 3.3V $V_{IN} = V_{SS}$ $V_{OL} = 0.5\ V$	01	$V_{DD1} = 3.13V$, $V_{DD2} = 3.13V$	1, 2, 3	8.0		
			02, 03	$V_{DD1} = 3.0V$, $V_{DD2} = 3.0V$	1, 2, 3	8.0		
		B Port = 5.0V $V_{IN} = V_{SS}$ $V_{OL} = 0.4\ V$	01	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.13\ V$	1, 2, 3	8.0		
			02, 03	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.0\ V$	1, 2, 3	8.0		
Output current (Source)	I_{OH} 10/	A Port = 3.3V $V_{IN} = V_{DD2}$ or V_{SS} $V_{OH} = V_{DD2} - 0.9\ V$	01	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.13\ V$	1, 2, 3	-8.0		mA
			02, 03	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.0\ V$	1, 2, 3	-8.0		
		A Port = 5.0V $V_{IN} = V_{DD2}$ or V_{SS} $V_{OH} = V_{DD2} - 0.7\ V$	All	$V_{DD1} = 4.5\ V$, $V_{DD2} = 4.5\ V$	1, 2, 3	-8.0		
		B Port = 3.3V $V_{IN} = V_{DD1}$ or V_{SS} $V_{OH} = V_{DD1} - 0.9\ V$	01	$V_{DD1} = 3.13V$, $V_{DD2} = 3.13V$	1, 2, 3	-8.0		
			02, 03	$V_{DD1} = 3.0V$, $V_{DD2} = 3.0V$	1, 2, 3	-8.0		
		B Port = 5.0V $V_{IN} = V_{DD1}$ or V_{SS} $V_{OH} = V_{DD1} - 0.7\ V$	01	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.13V$	1, 2, 3	-8.0		
			02, 03	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.0V$	1, 2, 3	-8.0		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified		Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
							Min	Max	
Three-state output leakage current high	I_{OZH} 7/	A Port = 3.3V For input under test, $V_{IN} = V_{DD2}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}		All	V_{DD1} = 5.5 V, V_{DD2} = 3.6 V	1, 2, 3		3.0	A
		$V_{OUT} = V_{DD2}$	M, D, P, L, R 5/	All		1		3.0	
		A Port = 5.0V For input under test, $V_{IN} = V_{DD2}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}		All	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1, 2, 3		3.0	
		$V_{OUT} = V_{DD2}$	M, D, P, L, R 5/	All		1		3.0	
		B Port = 3.3V For input under test, $V_{IN} = V_{DD1}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}		All	V_{DD1} = 3.6 V, V_{DD2} = 3.6 V	1, 2, 3		3.0	
		$V_{OUT} = V_{DD1}$	M, D, P, L, R 5/	All		1		3.0	
		B Port = 5.0V For input under test, $V_{IN} = V_{DD1}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}		All	V_{DD1} = 5.5 V, V_{DD2} = 3.6 V	1, 2, 3		3.0	
		$V_{OUT} = V_{DD1}$	M, D, P, L, R 5/	All		1		3.0	
Three-state output leakage current low	I_{OZL} 7/	A Port = 3.3V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}		All	V_{DD1} = 5.5 V, V_{DD2} = 3.6 V	1, 2, 3	-1.0		A
		$V_{OUT} = V_{SS}$	M, D, P, L, R 5/	All		1	-1.0		
		A Port = 5.0V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}		All	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1, 2, 3	-1.0		
		$V_{OUT} = V_{SS}$	M, D, P, L, R 5/	All		1	-1.0		
		B Port = 3.3V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}		All	V_{DD1} = 3.6 V, V_{DD2} = 3.6 V	1, 2, 3	-1.0		
		$V_{OUT} = V_{SS}$	M, D, P, L, R 5/	All		1	-1.0		
		B Port = 5.0V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}		All	V_{DD1} = 5.5 V, V_{DD2} = 3.6 V	1, 2, 3	-1.0		
		$V_{OUT} = V_{SS}$	M, D, P, L, R 5/	All		1	-1.0		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
Short circuit output current	I_{OS} 11/ 12/	A Port = 3.3V $V_{OUT} = V_{DD2}$ or V_{SS}	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	1, 2, 3	-100.0	100.0	mA
		A Port = 3.3V $V_{OUT} = V_{DD2}$ or V_{SS}	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	1, 2, 3	-100.0	100.0	
		A Port = 5.0V $V_{OUT} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	1, 2, 3	-200.0	200.0	
		B Port = 3.3V $V_{OUT} = V_{DD1}$ or V_{SS}	01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	1, 2, 3	-100.0	100.0	
		B Port = 3.3V $V_{OUT} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0V and 3.6 V	1, 2, 3	-100.0	100.0	
		B Port = 5.0V $V_{OUT} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	1, 2, 3	-200.0	200.0	
		B Port = 5.0V $V_{OUT} = V_{DD1}$ or V_{SS}	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	1, 2, 3	-200.0	200.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
Power dissipation	P_D 11/ 13/ 14/	A Port = 3.3V C_L = 50 pF, per switching output	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	4, 5, 6		1.5	mW/ MHz
		A Port = 3.3V C_L = 50 pF, per switching output	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	4, 5, 6		1.5	
		A Port = 5.0V C_L = 50 pF, per switching output	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	4, 5, 6		2.0	
		B Port = 3.3V C_L = 50 pF, per switching output	01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	4, 5, 6		1.5	
		B Port = 3.3V C_L = 50 pF, per switching output	02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0 V and 3.6 V	4, 5, 6		1.5	
		B Port = 5.0V C_L = 50 pF, per switching output	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	4, 5, 6		2.0	
		B Port = 5.0V C_L = 50 pF, per switching output	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	4, 5, 6		2.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
Quiescent supply current	I_{DDQ}	A Port = 5.0V $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1		10.0	µA
					2, 3		100.0	
		M, D, P, L, R 5/	All		1		500.0	
		B Port = 5.0V $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1		10.0	
					2, 3		100.0	
		M, D, P, L, R 5/	All		1		500.0	
Input capacitance	C_{IN}	f = 1 MHz, See 4.4.1c	All	V_{DD1}, V_{DD2} = 0.0 V	4		15	pF
Output capacitance	C_{OUT}	f = 1 MHz, See 4.4.1c	All	V_{DD1}, V_{DD2} = 0.0 V	4		15	pF
Functional test	15/	$V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$ See 4.4.1b	01	V_{DD1} = 4.5 V and 5.5 V,	7, 8	L	H	
		M, D, P, L, R 5/	01	V_{DD2} =3.13 V and 3.6 V	7	L	H	
		$V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$ See 4.4.1b	02, 03	V_{DD1} = 4.5 V and 5.5 V,	7, 8	L	H	
		M, D, P, L, R 5/	02, 03	V_{DD2} =3.0 V and 3.6 V	7	L	H	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
						Min	Max	
Propagation delay time, data to bus (active low)	t_{PLH} 16/	B Port = 5V, A Port = 3.3V, C_L = 50 pF, see figure 4	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
		M, D, P, L, R 5/	01		9	1.0	20.0	
		B Port = 5V, A Port = 3.3V, C_L = 50 pF, see figure 4	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
		M, D, P, L, R 5/	02, 03		9	1.0	20.0	
		A Port = B Port, 5V operation, C_L = 50 pF, see figure 4	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
		M, D, P, L, R 5/	All		9	1.0	15.0	
		A Port = B Port 3.3 V operation, C_L = 50 pF, see figure 4	01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	20.0	
		M, D, P, L, R 5/	01		9	1.0	20.0	
		A Port = B Port 3.3V operation, C_L = 50 pF, see figure 4	02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
		M, D, P, L, R 5/	02, 03		9	1.0	20.0	
Propagation delay time, data to bus (active high)	t_{PHL} 16/	B Port = 5V, A Port = 3.3V, C_L = 50 pF see figure 4	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
		M, D, P, L, R 5/	01		9	1.0	20.0	
		B Port = 5V, A Port = 3.3V, C_L = 50 pF see figure 4	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
		M, D, P, L, R 5/	02, 03		9	1.0	20.0	
		A Port = B Port, 5V operation, C_L = 50 pF see figure 4	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
		M, D, P, L, R 5/	All		9	1.0	15.0	
		A Port = B Port 3.3 V operation, C_L = 50 pF, see figure 4	01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	20.0	
		M, D, P, L, R 5/	01		9	1.0	20.0	
		A Port = B Port 3.3 V operation, C_L = 50 pF, see figure 4	02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
		M, D, P, L, R 5/	02, 03		9	1.0	20.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified		Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
							Min	Max	
Propagation delay time, output enable, OEn to bus (active low)	t_{PZL} 16/	B Port = 5V, A Port = 3.3V C_L = 50 pF see figure 4		01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	18.0	ns
			M, D, P, L, R 5/	01		9	1.0	18.0	
		B Port = 5V, A Port = 3.3V C_L = 50 pF see figure 4		02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
			M, D, P, L, R 5/	02, 03		9	1.0	18.0	
		A Port = B Port, 5V operation C_L = 50 pF, see figure 4		All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	12.0	
			M, D, P, L, R 5/	All		9	1.0	12.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4		01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	18.0	
			M, D, P, L, R 5/	01		9	1.0	18.0	
		A Port = B Port 3.3V operation C_L = 50 pF see figure 4		02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
			M, D, P, L, R 5/	02, 03		9	1.0	18.0	
Propagation delay time, output enable, OEn to bus (active high)	t_{PZH} 16/	B Port = 5V, A Port = 3.3V C_L = 50 pF see figure 4		01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	18.0	ns
			M, D, P, L, R 5/	01		9	1.0	18.0	
		B Port = 5V, A Port = 3.3V C_L = 50 pF see figure 4		02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
			M, D, P, L, R 5/	02, 03		9	1.0	18.0	
		A Port = B Port, 5V operation C_L = 50 pF see figure 4		All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	12.0	
			M, D, P, L, R 5/	All		9	1.0	12.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4		01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	18.0	
			M, D, P, L, R 5/	01		9	1.0	18.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4		02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
			M, D, P, L, R 5/	02, 03		9	1.0	18.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified		Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
							Min	Max	
Propagation delay time, output disable, OEn to bus (high impedance)	t_{PLZ} 16/	B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
				01		9	1.0	20.0	
		B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
				02, 03		9	1.0	20.0	
		A Port = B Port 5V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
				All		9	1.0	15.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	
				01		9	1.0	20.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
				02, 03		9	1.0	20.0	
Propagation delay time, output disable, OEn to bus (high impedance)	t_{PHZ} 16/	B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
				01		9	1.0	20.0	
		B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
				02, 03		9	1.0	20.0	
		A Port = B Port 5V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
				All		9	1.0	15.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	
				01		9	1.0	20.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
				02, 03		9	1.0	20.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified		Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
							Min	Max	
Propagation delay time, output enable, DIRn to bus (active low)	t_{PZL} 17/	B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	18.0	ns
				01		9	1.0	18.0	
		B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
				02, 03		9	1.0	18.0	
		A Port = B Port 5V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	12.0	
				All		9	1.0	12.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	18.0	
				01		9	1.0	18.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
				02, 03		9	1.0	18.0	
Propagation delay time, output enable, DIRn to bus (active high)	t_{PZH} 17/	B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	18.0	ns
				01		9	1.0	18.0	
		B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
				02, 03		9	1.0	18.0	
		A Port = B Port 5V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	12.0	
				All		9	1.0	12.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	18.0	
				01		9	1.0	18.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
				02, 03		9	1.0	18.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified		Device type	V_{DD} 3/	Group A subgroups	Limits 4/		Unit
							Min	Max	
Propagation delay time, output disable, DIRn to bus (high impedance)	t_{PLZ} 17/	B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
				01		9	1.0	20.0	
		B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
				02, 03		9	1.0	20.0	
		A Port = B Port 5V Operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
				All		9	1.0	15.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	20.0	
				01		9	1.0	20.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
				02, 03		9	1.0	20.0	
Propagation delay time, output disable, DIRn to bus (high impedance)	t_{PHZ} 17/	B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
				01		9	1.0	20.0	
		B Port = 5V A Port = 3.3V C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
				02, 03		9	1.0	20.0	
		A Port = B Port 5V Operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
				All		9	1.0	15.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	01	V_{DD1} =3.13 V and 3.6 V, V_{DD2} =3.13 V and 3.6 V	9, 10, 11	1.0	20.0	
				01		9	1.0	20.0	
		A Port = B Port 3.3 V operation C_L = 50 pF see figure 4	M, D, P, L, R 5/	02, 03	V_{DD1} =3.0 V and 3.6 V, V_{DD2} =3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
				02, 03		9	1.0	20.0	

See footnotes on next page.

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{DD} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, $V_{IN} = V_{SS}$ or $V_{IN} \geq 3.13$ V for device type 01 and 3.0 V for device types 02 and 03.

2/ Temperature range for device type 03 is -40°C to +125°C.

2/ This device requires both V_{DD1} and V_{DD2} power supplies for operation. The power supply will be indicated followed by the voltage to which the power supply is set to for the given test

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to V_{SS} and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ Devices supplied to this drawing meet all levels M, D, P, L, and R of irradiation. However, these devices are only tested at the "R" level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

5/ Guaranteed; tested on a sample of pins per device at 3.6 V, 4.5 V, and 5.5 V. Tested on all pins at 3.13 V for device type 01 and 3.0 V for device types 02 and 03.

6/ Guaranteed; tested on a sample of pins at 3.6 V. Tested on all pins at 5.5 V.

7/ Guaranteed; tested on a sample of pins at 3.13 V for device type 01 and 3.0 V for device types 02 and 03. Tested on all pins at 4.5 V.

8/ Guaranteed; tested on a sample of pins at 3.13 V for device type 01 and 3.0 V for device types 02 and 03, and 4.5 V.

9/ Guaranteed based on characterization data but not tested.

10/ This parameter is supplied as design limit but not guaranteed or tested.

11/ No more than one output should be shorted at a time for a maximum duration of one second.

12/ Power does not include power contribution of any CMOS output sink current.

13/ Power dissipation specified per switching output.

14/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(\text{min} + 20\%, - 0\%)$; $V_{IL} = V_{IL}(\text{max} + 0\%, - 50\%)$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices are guaranteed to $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

15/ For propagation delay tests, all paths must be tested.

16/ Guaranteed by design but not tested.

Case outline X

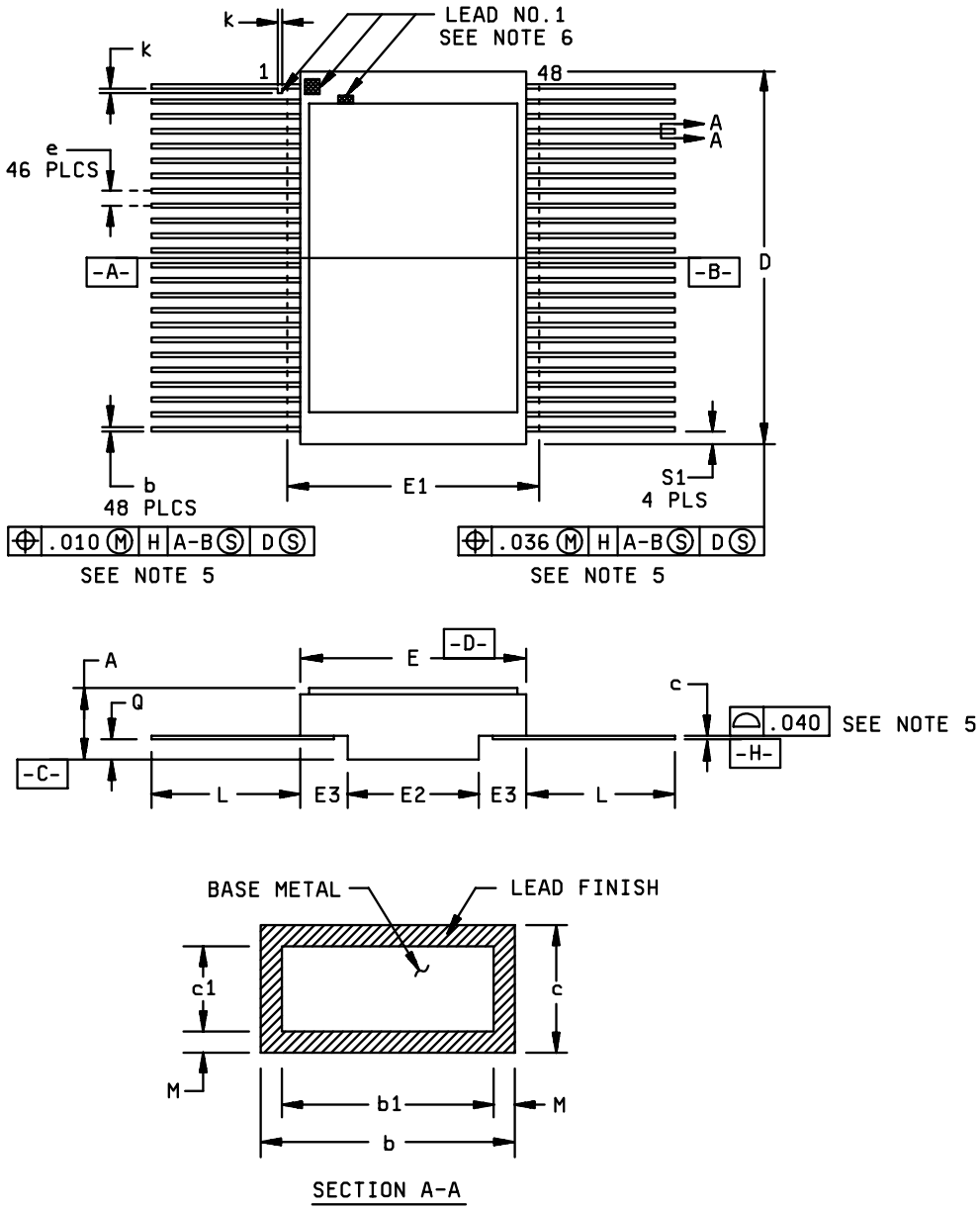


FIGURE 1. Case outline

Case outline X						
Symbol	Inches			Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	.080		.120	2.032		3.048
b	.006		.015	0.1524		0.381
b1	.006		.013	0.1524		0.3302
c	.004		.010	0.1016		0.254
c1	.004		.008	0.1016		0.2032
D	.610		.640	15.494		16.256
E	.370		.390	9.398		9.906
E1	.430		.470	10.922		11.938
E2	.180			4.572		
E3	.030			0.762		
e	.025 BSC			0.635		
k	N/A			N/A		
L	.250		.370	6.35		9.398
Q	.026		.045	0.6604		1.143
S1	.005			0.127		
M			.0015			0.0381
N	48			48		

NOTES:
1/ All exposed metalized areas must be gold plated over electroplated nickel per MIL-PRF-38535.
2/ The lids are electrically connected to V_{SS}.
3/ Lead finishes are in accordance with MIL-PRF-38535.
4/ Dimension symbology is in accordance with MIL-PRF-38535.
5/ Lead position and coplanarity are not measured.
6/ ID mark symbol is vendor option: No alphanumerics. One or both ID methods may be used for pin 1 ID.

FIGURE 1. Case outline - Continued.

Device type	All		
Case outlines	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DIR1	25	OE2
2	1B1	26	2A8
3	1B2	27	2A7
4	VSS	28	VSS
5	1B3	29	2A6
6	1B4	30	2A5
7	V_{DD1}	31	V_{DD2}
8	1B5	32	2A4
9	1B6	33	2A3
10	VSS	34	VSS
11	1B7	35	2A2
12	1B8	36	2A1
13	2B1	37	1A8
14	2B2	38	1A7
15	VSS	39	VSS
16	2B3	40	1A6
17	2B4	41	1A5
18	V_{DD1}	42	V_{DD2}
19	2B5	43	1A4
20	2B6	44	1A3
21	VSS	45	VSS
22	2B7	46	1A2
23	2B8	47	1A1
24	DIR2	48	OE1

Pin description	
Terminal symbol	Description
OEn	Output Enable inputs (active low)
DIRn	Direction control inputs
nAn	Side A inputs or 3-state outputs (3.3 V Port)
nBn	Side B inputs or 3-state outputs (5.0 V Port)

FIGURE 2. Terminal connections.

Inputs		Operation
Enable OEn	Direction DIRn	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High voltage level
L = Low voltage level
X = Irrelevant

Port A	Port B	Operation
3.3 Volts	5.0 Volts	Voltage Translator
5.0 Volts	5.0 Volts	Non-Translating
3.3 Volts	3.3 Volts	Non-Translating
V_{SS}	V_{SS}	Cold Spare
3.3 V or 5.0 V	V_{SS}	Port B Cold Spare

NOTE:

Control signals DIRx and $\overline{OEx}$ are 5 volt tolerant inputs. When V_{DD2} is at 3.3 volts, either 3.3 or 5.0 volt CMOS logic levels can be applied to all control inputs. For proper operation, connect power to all V_{DD} and ground all V_{SS} pins (i.e., no floating V_{DD} or V_{SS} input pins). Tie unused inputs to V_{SS}.

If V_{DD1} and V_{DD2} are not powered up together, then V_{DD2} should be powered up first for proper control of DIRx and OEx. The internal state of DIRx and OEx is unknown when V_{DD2} is not powered, because the internal circuitry for these pins is powered by V_{DD2}. Until V_{DD2} reaches 2.75 V ±5%, control of the outputs by DIRx and OEx cannot be guaranteed. During operation of the part, after power up, insure $V_{DD1} \geq V_{DD2}$.

FIGURE 3. Truth table.

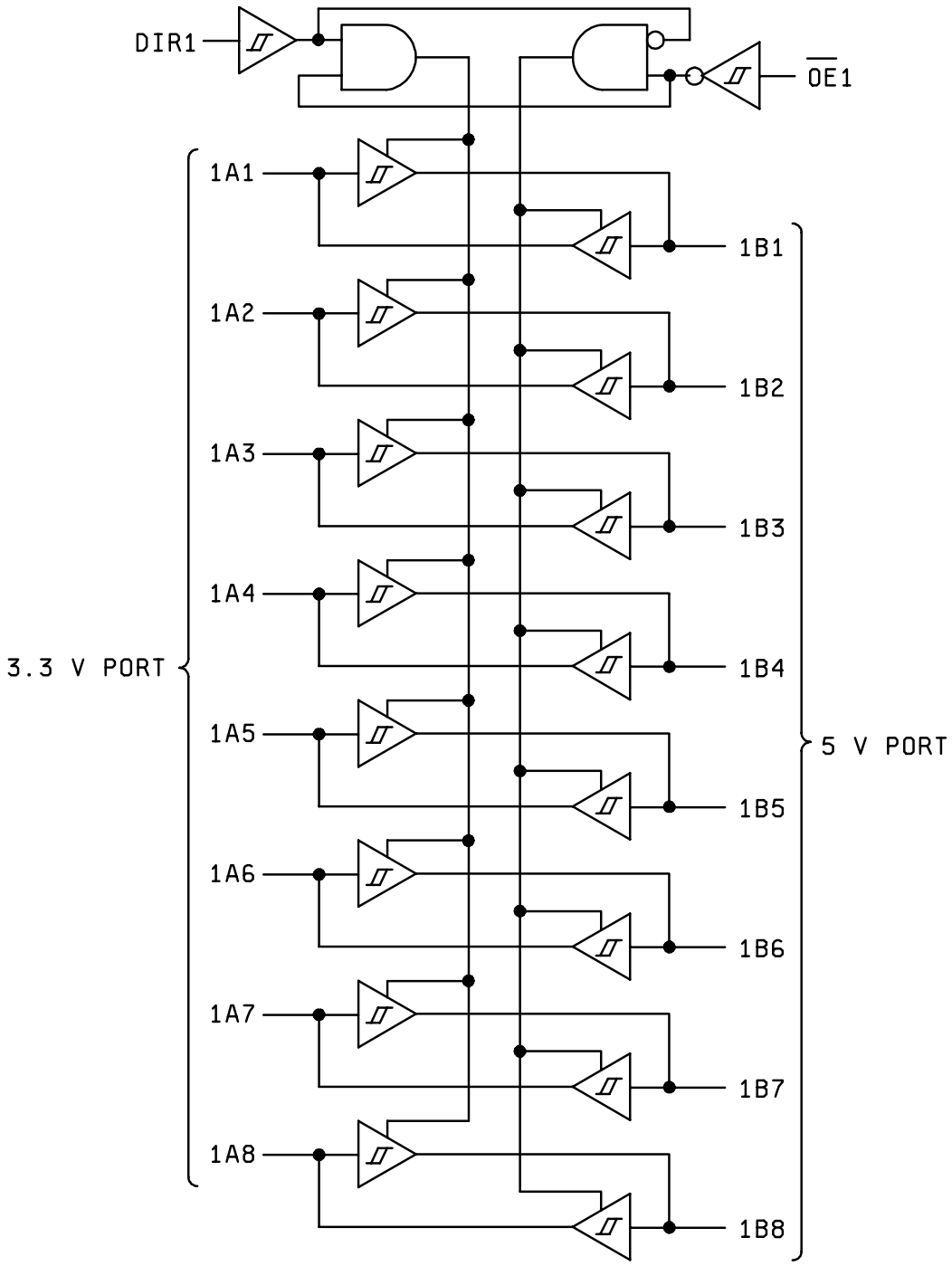


FIGURE 4. Logic diagram.

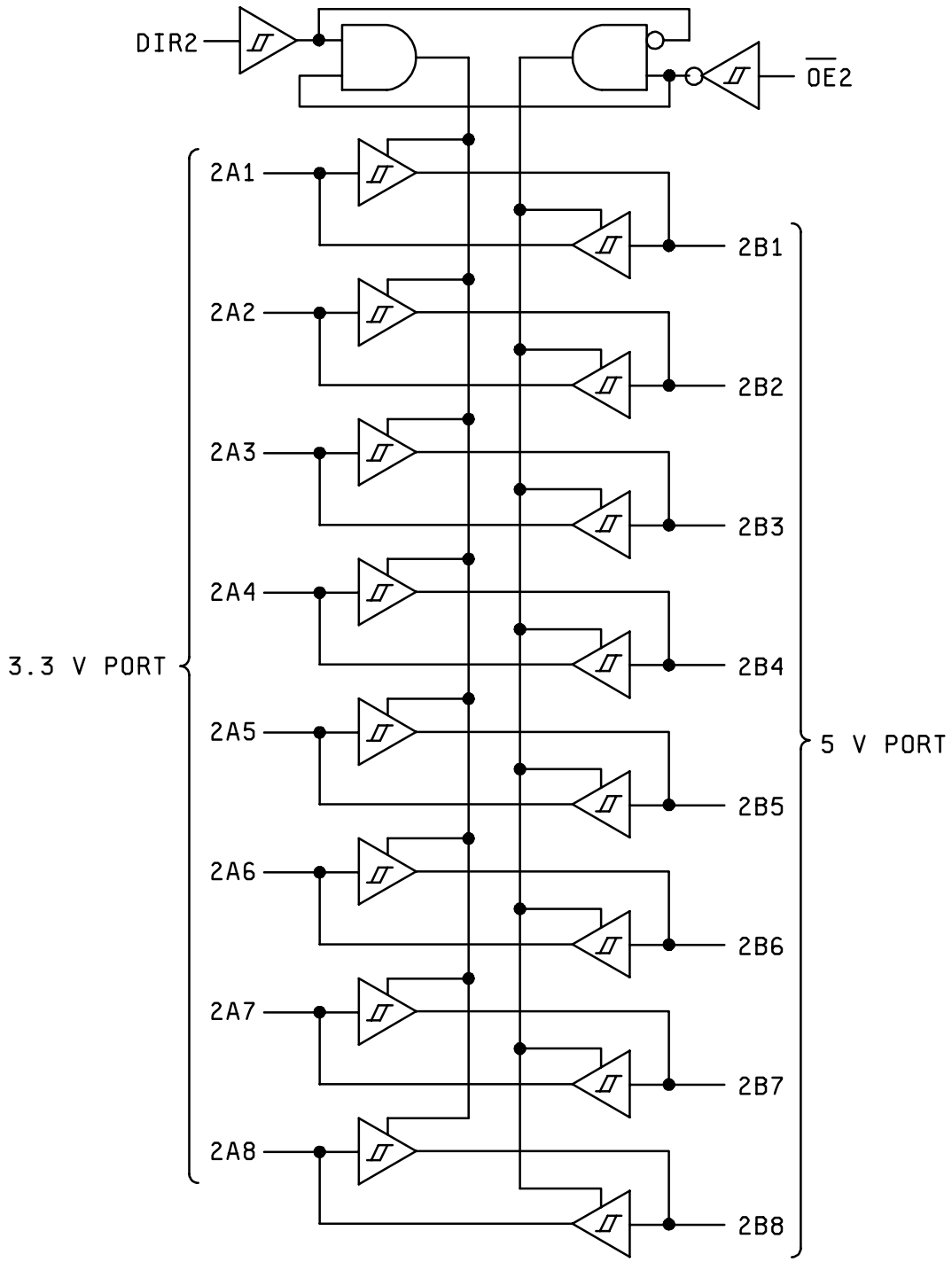


FIGURE 4. Logic diagram - Continued.

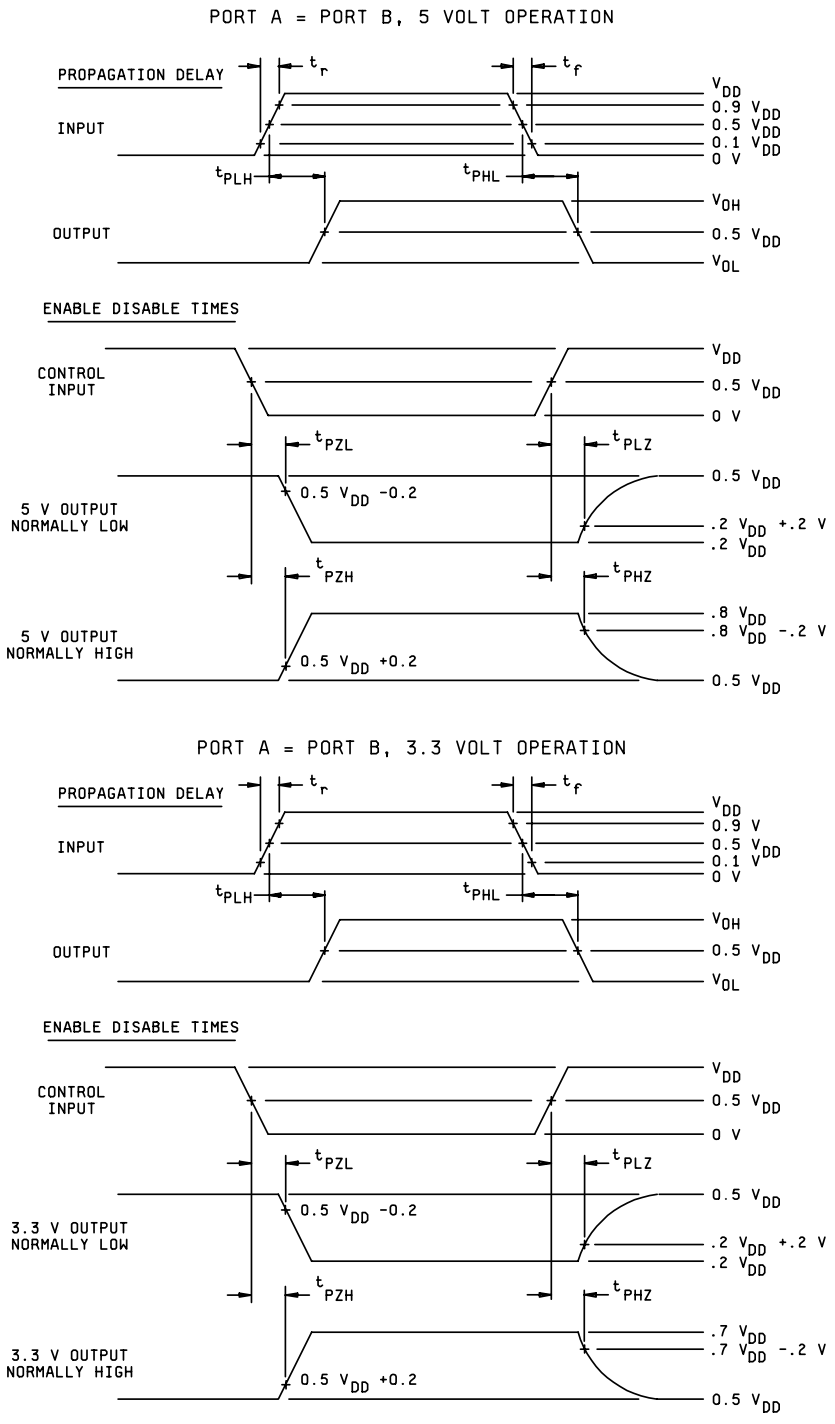
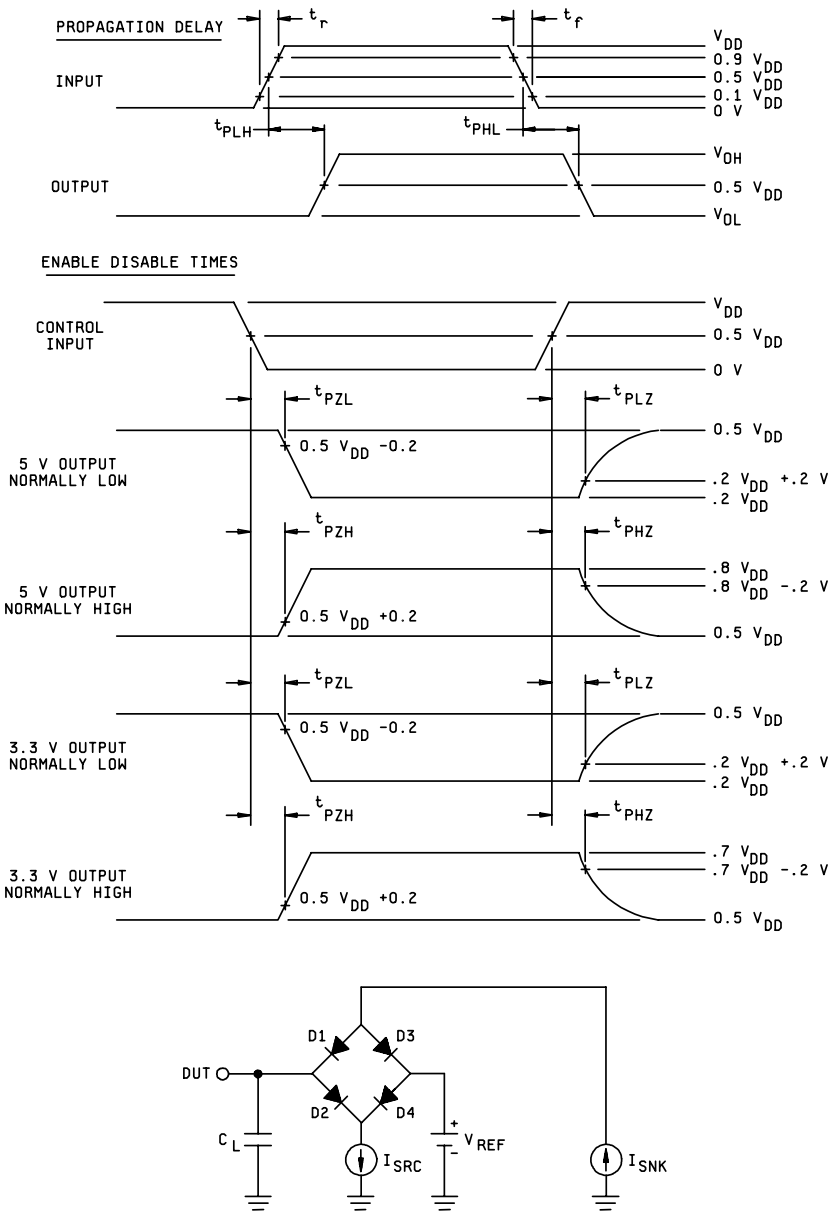


FIGURE 5. Switching waveforms and test circuit.

PORT B = 5 VOLT,PORT A = 3.3 VOLT



Notes:

1/ $V_{REF} = 0.5V_{DD}$.
2/ C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
3/ I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} and t_{PLH} measurements.
4/ Input signal from pulse generator: V_{IN} = 0.0 V to V_{DD}; f ≤ 10 MHz; t_r = 1.0 V/ns "0.3 V/ns; t_f = 1.0 V/ns "0.3 V/ns; t_r and t_f shall be measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD}, respectively.

FIGURE 5. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C 3/	V_{DD1} = 4.5 V		Bias for latch-up test V_{DD} = 5.5 V no latch-up LET = 3/ 4/
		Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section	
All	+25°C	LET ≥ 80	6 x 10^{-9} cm^2/bit	≥ 120

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature is T_A ≥ +125°C.
4/ Tested to a LET of ≤ 120 MeV/(mg/cm^2), with no latch-up (SEL).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	3/ 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroups 1 and 7.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits as specified in table IIB herein shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, Delta parameters (+25°C).

Parameters	Symbol	Delta limits
Output voltage low	V_{OL}	±100 mV
Output voltage high	V_{OH}	±100 mV

TABLE III. Irradiation test connections.

Device types	Open	Ground	V_{DD} = 5.0 V ±0.5 V
All	13, 14, 16, 17, 19, 20, 22, 23, 37, 38, 40, 41, 43, 44, 46, 47	1, 2, 4, 5, 8, 10, 11, 15, 21, 25, 26, 28, 29, 32, 34, 35, 39, 45, 48	3, 6, 7, 9, 12, 18, 24, 27, 30, 31, 33, 36, 42

NOTE: Each pin except 4, 7, 10, 15, 18, 21, 28, 31, 34, 39, 42 and 45 will have a resistor of 2.49 kΩ ±5% for irradiation testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{OUT}, shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, test method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated aging testing. Accelerated aging testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C for the upset measurements and the maximum rated operating temperature ±10°C for the latchup measurements.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

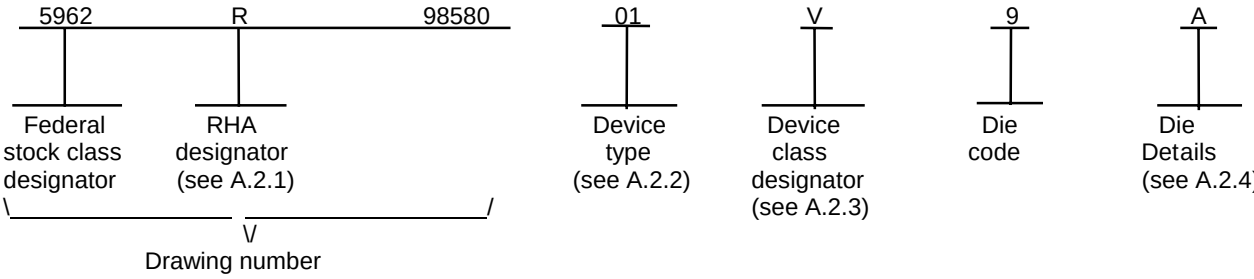
6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX A

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN shall be as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS164245S	Radiation hardened, Schmitt 16-bit bidirectional mult-purpose transceiver with three-state outputs and cold sparing
02	54ACS164245S 1/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, and extended voltage range
03	54ACS164245S 1/ 2/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, extended voltage range, and extended industrial temperature range of -40°C to +125°C

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

1/ Device types 02 and 03 have an extended voltage range.
2/ Device type 03 has an extended industrial temperature range of -40°C to +125°C.

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die Physical dimensions.

Die Type	Figure number
01, 02, 03	A-1

A.1.2.4.2 Die Bonding pad locations and Electrical functions.

Die Type	Figure number
01, 02, 03	A-1

A.1.2.4.3 Interface Materials.

Die Type	Figure number
01, 02, 03	A-1

A.1.2.4.4 Assembly related information.

Die Type	Figure number
01, 02, 03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2. APPLICABLE DOCUMENTS

A.2.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item Requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die Physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table(s). The truth table(s) shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.7 of the body of this document.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4. QUALITY ASSURANCE PROVISIONS

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer Lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph A.3.4 herein).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5. DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6. NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.

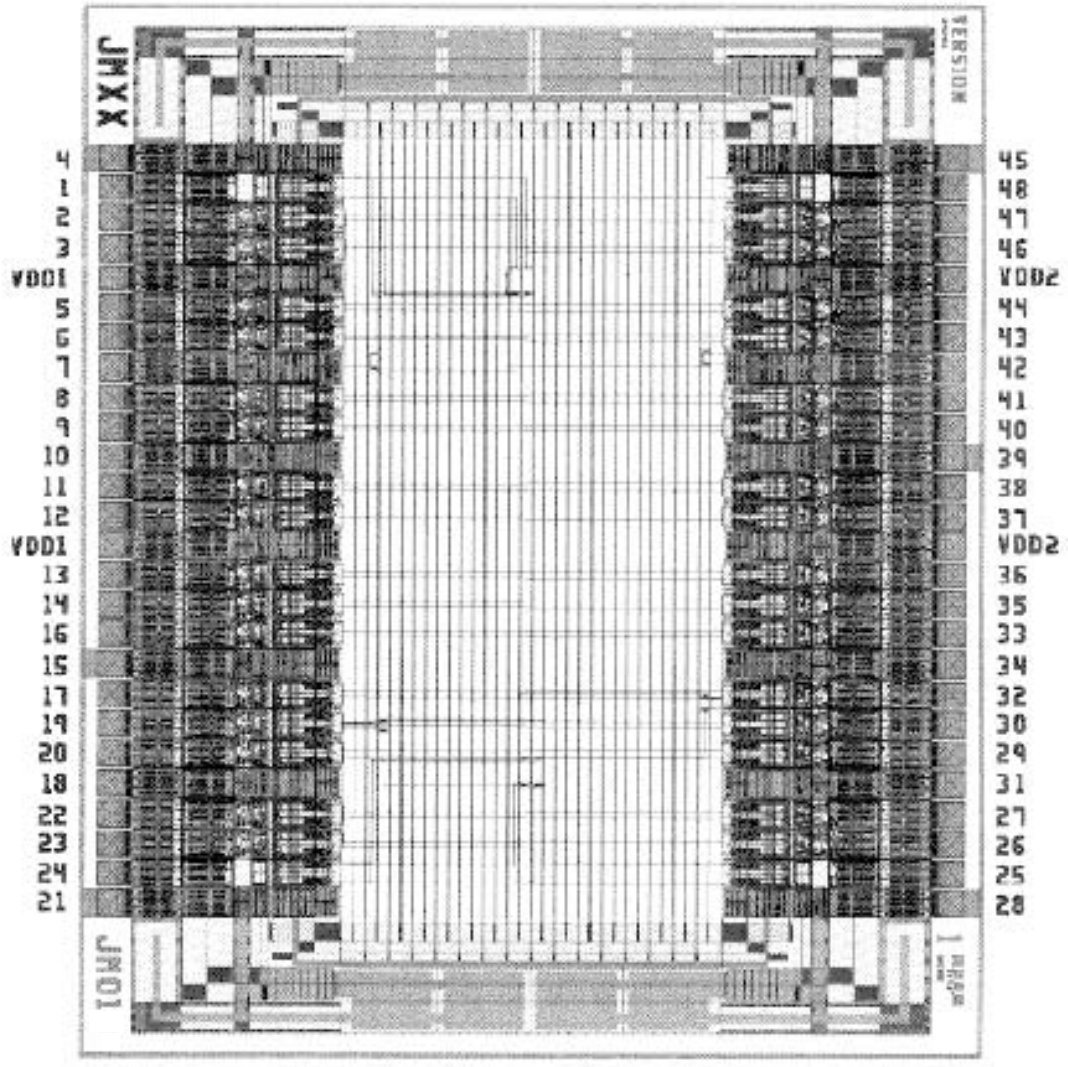
APPENDIX A

FIGURE A-1

DIE PHYSICAL DIMENSIONS

Die Size:	132.97 x 115.827 mils.
Die Thickness:	17.5 +/- 1 mils.

DIE BONDING PAD LOCATIONS AND ELECTRICAL FUNCTIONS



NOTE: Pad numbers reflect terminal numbers when placed in Case Outline X (see Figure 2).

INTERFACE MATERIALS

Top Metallization:	Si Al Cu	6.2kA – 7.6kA
Backside Metallization:	None.	
Glassivation		
Type:	Oxide/Nitride	
Thickness:	9kA - 11kA	
Substrate:	Epitaxial Layer on Single crystal silicon.	

ASSEMBLY RELATED INFORMATION

Substrate Potential:	Tied to V_{SS}.
Special assembly instructions:	None.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 02-05-10

Approved sources of supply for SMD 5962-98580 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9858001QXC	65342	UT54ACS164245SUCC
5962R9858001VXC	65342	UT54ACS164245SUCCR
5962-9858001Q9A	65342	UT54ACS164245S-Q DIE
5962R9858001V9A	65342	UT54ACS164245S-V DIE
5962-9858002QXC	65342	UT54ACS164245SUCC 3/
5962R9858002VXC	65342	UT54ACS164245SUCCR 3/
5962-9858002Q9A	65342	UT54ACS164245S-Q DIE 3/
5962R9858002V9A	65342	UT54ACS164245S-V DIE 3/
5962-9858003QXC	65342	UT54ACS164245SUCC 3/ 4/
5962R9858003VXC	65342	UT54ACS164245SUCCR 3/ 4/
5962-9858003Q9A	65342	UT54ACS164245S-Q DIE 3/ 4/
5962R9858003V9A	65342	UT54ACS164245S-V DIE 3/ 4/

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ These parts have an extended voltage range.
4/ These parts have an extended industrial temperature range of -40°C to +125°C.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronic Systems 4350 Centennial Boulevard Colorado Springs, CO 80907-3486