EXAR

XR-8000

T-52-33-01

Microprocessor Support IC

GENERAL DESCRIPTION

The XR-8000 provides simplicity in monitoring of microprocessor controlled systems. The features included in XR-8000 are: on-board 5V/50mA voltage regulator, undervoltage reset, delay reset on powerup, watchdog monitor, short circuit protection and low quiescent current.

The on-board regulator will provide power for all supporting logic and memory circuitry up to 50mA load current. Hence, low power systems will not require a separate voltage regulator IC, which will provide system cost savings.

The low voltage detect level is internally set to 4.4V. It is also externally adjustable with an addition of one external 1MΩ potentiometer. The recommended capacitor value for both external timing capacitors is 0.1uF. With the recommended capacitor values, the nominal turn-on delay time and the oscillation period of the internal oscillator will be 90msec and 65msec, respectively. Both the XR-8000 and XR-8001 (inverted reset) are available in 8 pin PDIP.

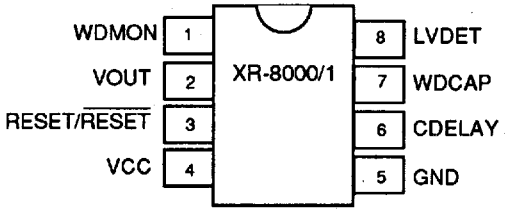
FEATURES

Powerup reset with adjustable delay.
Undervoltage reset with adjustable level.
Watchdog monitor with adjustable timeout period.
5V/50mA on board regulator.
Internal current limit.
7V to 24V supply voltage operating range.
RESET or $\overline{\text{RESET}}$ output.

ABSOLUTE MAXIMUM RATINGS

VCC		-0.3V to 26V
VOUT		-0.3V to 7V
Reset/$\overline{\text{Reset}}$ Output		-0.3V to 26V
Operating Temperature Range		-40°C to +85°C
Package Type		8 PIN PDIP
Power Dissipation	8 PIN PDIP	750mW @ 25°C
		300mW @ 85°C
Storage Temperature Range		-65°C to +160°C
Lead Temperature (soldering 10 sec.)		300°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8000IP	8 pin PDIP	-40°C to +85°C
XR-8001IP	8 pin PDIP	-40°C to +85°C

SYSTEM DESCRIPTION

Fig.1 shows the block diagram for the XR-8000, Fig. 2 shows the timing diagram for the pins of interest and Fig. 3 shows an applications circuit. Whenever the regulator output drops below 4.4 volts, the RESET pin is pulled high. At the same time, the delay and the watchdog oscillator capacitors are discharged (reset). When the regulator output voltage returns above 4.5 volts, the delay capacitor starts charging up and provides 90msec delay time before the RESET pin is returned to its low state. At the same time when the RESET switches from high to low, the WDCAP capacitor starts charging. The microprocessor has 90msec to provide a positive going pulse on the WDMON pin before a reset signal is issued. In absence of the pulse on the WDMON pin, the RESET pin will continue to issue reset pulses (controlled by the watchdog oscillator) until the microprocessor issues a pulse on the WDMON pin. The microprocessor needs to issue at least one pulse every 65msec to prevent the RESET pin from issuing a reset signal. The RESET pin is also delayed by 90msec during powerup. See Fig. 2 for timing diagrams.

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XR-8000

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ELECTRICAL SPECIFICATIONS:

Vin=14V, Iout=5mA, CDELAY=0.1µF, WDCAP=0.1µF, CL=1µF, T_A=25°C unless otherwise specified. RESET output specs apply to RESET output.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
REGULATOR						
VOUT	Output Voltage	4.65	5.0	5.35	V	IL = 50MA
IOUT	Output Current	50	75		MA	VOUT>4.65V
ICC	Supply Current		600	800	µA	IL=0
IMAX	Short Circuit Current Limit	50	120	200	MA	VOUT=0V
WATCHDOG						
VLDT	Low Voltage Detect Threshold	4.25	4.40	4.55	V	RL(RESET)=10K
VLDH	Low Voltage Detect Hysteresis		20		MV	RS(RESET)=10K
IWD	WDMON Input Current		350	500	µA	VWDMON=5V
			120	175	µA	VWDMON=2.4V
			12	17	µA	VWDMON=.8V
VWD	WDMON Threshold	0.8	1.6	2.4	V	
V_{reset}	VRESET		.25	0.4	V	IRESET=1MA
I_{reset}	IRESET	1.0	2.0		MA	VRESET=.4V
I_{leak}	IRESET (LEAKAGE)		.05	1.0	µA	VRESET=5V

AC SPECIFICATIONS:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
WATCHDOG						
tPUD	Powerup Reset Delay		90		MSEC	VWDMON=5V
TOSC	Reset Oscillation Period		65		MSEC	VWDMON=.8V
tRPW	Reset Pulse Width		2.0		MSEC	VWDMON=.8V
t_f	Reset Fall Time		0.8		µSEC	RL(RESET)=10K
t_r	Reset Rise Time		0.5		µSEC	RL(RESET)=10K
t_{reset}	Reset Delay		90		MSEC	PW=5USEC
tWDPW	WDMON Pulse Width	5			µSEC	(NOTE 1)
TWD	WDMON Period			90	MSEC	PW=5USEC

NOTE 1: Pulse widths less than 5µsec, down to 1µsec, can be used with at least two pulses issued in one RESET oscillation period.

SYSTEM DESCRIPTION (cont.)

For systems with power supply rise time greater than 90msec, the powerup delay time (DELAY cap.) should be increased to allow the supply to reach its final value before the RESET pin is released.

The delay time on powerup is set by an external capacitor (CDELAY) and an internal current source. Similarly, the oscillator frequency is set by an external capacitor and two internal current sources. Thus, the powerup reset delay and the watchdog oscillation frequency can be set by selecting proper external capacitor values to conform to the system requirements. The following equations define the relationship between the external component values and the desired parameters:

Powerup Delay Time(nominal) = K1CDELAY,
where K1 = 900msec/μF

Watchdog Oscillator Period(nominal) = K2CWD,
where K2 = 650msec/μF

Reset Pulse Width = K3CWD
where K3 = 20msec/μF

K1, K2 and K3 constants will have manufacturing tolerances associated with standard IC fabrication techniques. The low voltage threshold level will also have a tolerance proportional to the internal bandgap reference. The nominal value of the bandgap reference is 1.2V ± 40mV. As a result, the low voltage threshold level will have ± 3.3% tolerance (neglecting resistor matching tolerance). To obtain better accuracy, a 1 MegΩ trim pot, connected between regulated output and ground with the wiper arm connected to the LVDET pin, can be used and adjusted until the desired threshold voltage level is obtained.

The watchdog monitor pulse width (issued by a microprocessor) is restricted by the WDCAP discharge time and will be proportional to the WDCAP capacitor value. The WDCAP voltage waveform, shown in Fig. 2, shows the WDCAP being discharged to its reset level during each WDMON pulse. This will be true if WDMON pulse widths are 5μsec or greater with WDCAP capacitor value of 0.1μF. As the WDMON pulse width is reduced, the WDCAP low voltage level will start to rise. Therefore, the WDMON pulse frequency needs to be increased to prevent the WDCAP voltage from reaching its upper threshold level. Inversely, if the WDMON capacitor value is increased, the WDMON pulse width needs to be increased proportionally. The following equation defines the relationship between the WDCAP capacitor value and minimum WDMON pulse width.

PW(min) = K4WDCAP
where K4 = 50 μsec/μF

Due to propagation delay times, the minimum pulse width is restricted to 500nsec. When the pulse width becomes significant with respect to the RESET OSCILLATION PERIOD, the WDMON period can be increased by the same amount as the pulse width. For example, with the nominal capacitor values and 20 msec WDMON pulse width, the WDMON period can be increased by 20 msec. One should keep in mind that when a long WDMON pulse width is used, the total RESET DELAY time will be increased by the amount of the pulse width. This feature provides an advantage for obtaining an increase in the RESET DELAY time without increasing the WDCAP capacitor value.

The XR-8000 can be used in any system that requires voltage level monitoring, with or without microprocessor controller. The XR-8001 has identical specifications as the XR-8000 with the RESET pin providing an inverted RESET function. The watchdog function can be defeated by connecting the WDMON pin through a 10K resistor to the VOUT pin on either the XR-8000 or XR-8001 IC.

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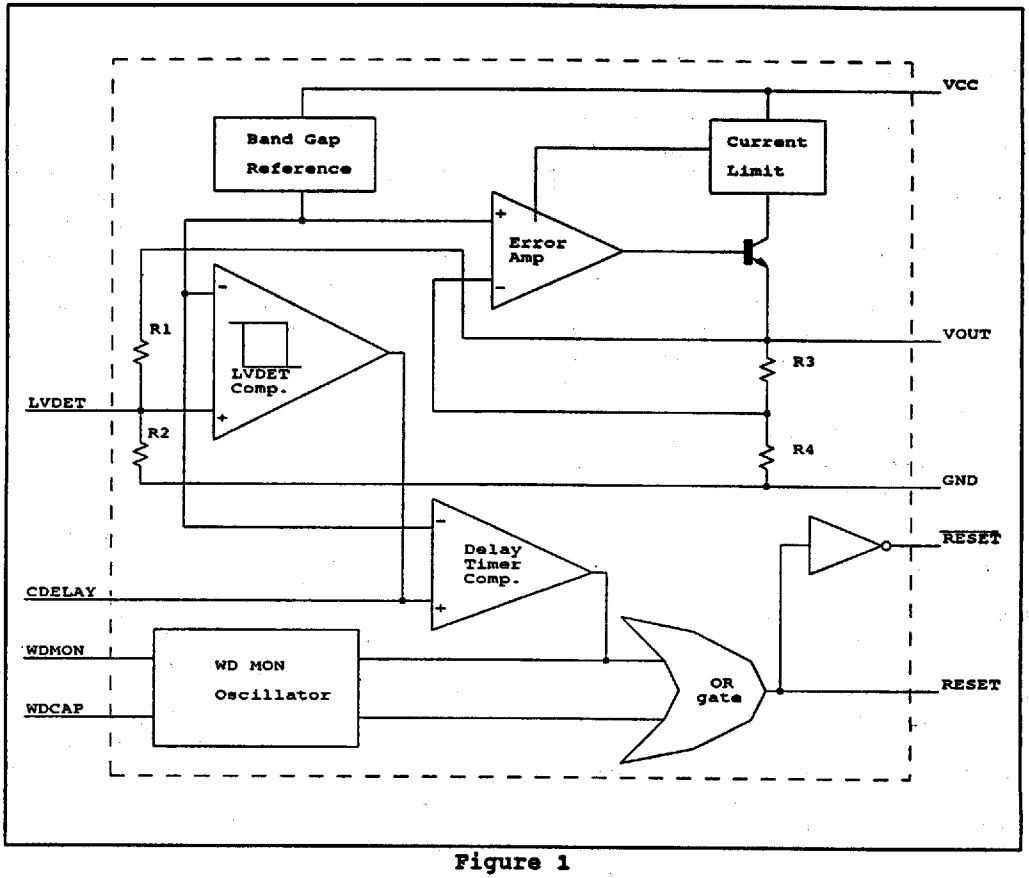
VCC
Band Gap
Reference
Current
Limit
Error
Amp
R1
LVDET
Comp.
VOUT
R3
LVDET
R2
R4
GND
Delay
Timer
Comp.
RESET
CDELAY
WDMON
WD MON
Oscillator
OR
gate
RESET
WDCAP

Figure 1

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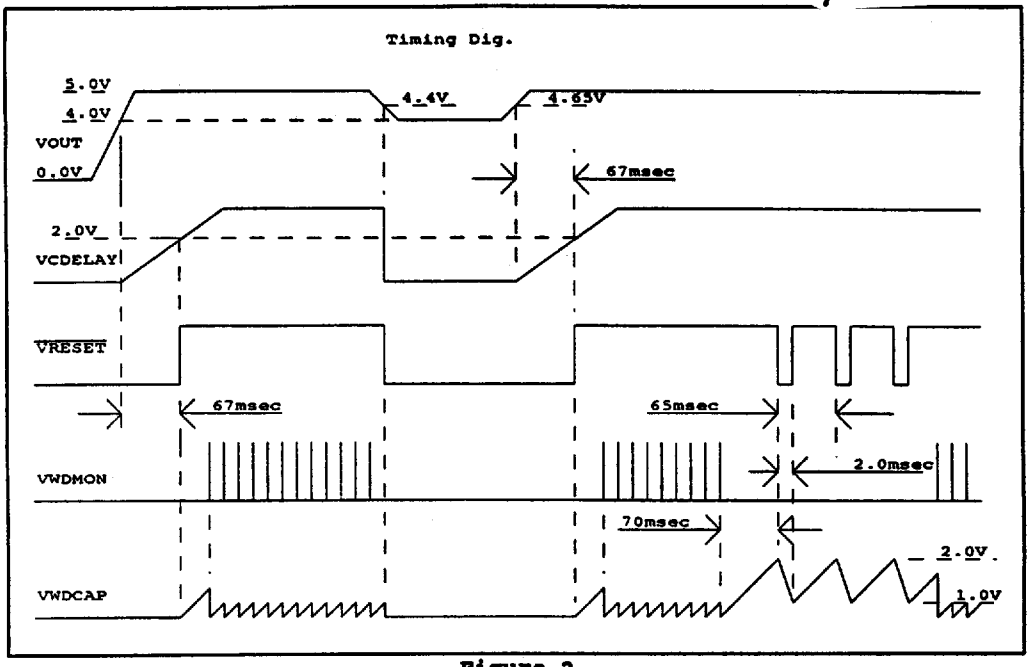

Figure 2

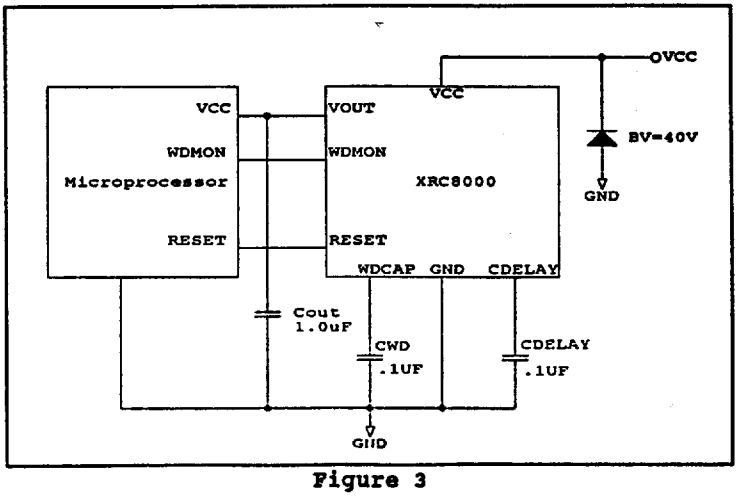

Figure 3