ABRIDGED VERSION

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SSI 34P3400
45 Mbit/s Read Channel w/Adaptive Threshold Qualifier

Advance Information

January 1996

DESCRIPTION

The SSI 34P3400 device is a high performance BiCMOS single chip read channel IC that contains all the functions necessary to implement a complete zoned recording disk drive system. Functional blocks include a pulse detector with adaptive threshold qualifier, programmable filter, 4-burst servo capture, time base generator, and data synchronizer with raw data interface. Raw data rates from 9 to 45 Mbit/s can be programmed by digital commands without external component switching.

The SSI 34P3400 allows complete flexibility in read channel configuration. Essentially all critical parameters can be programmed by a microprocessor via a bi-directional serial port and a bank of internal registers. Thus, a low component count and low cost zoned recording system can be implemented.

The SSI 34P3400 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

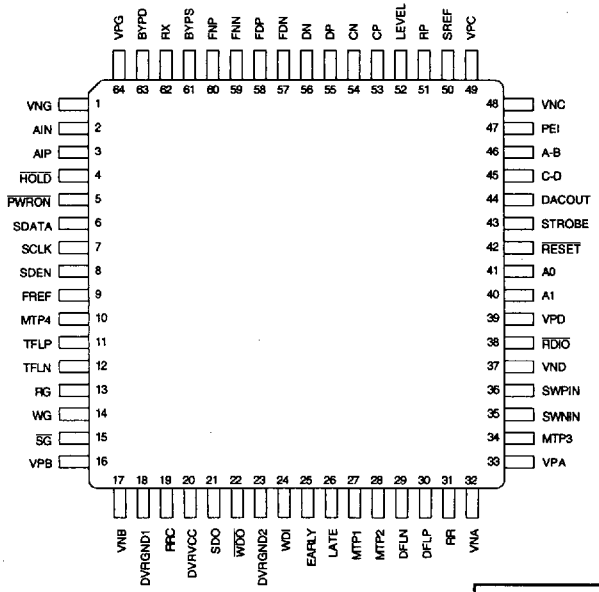
FEATURES

GENERAL

- **9 to 45 Mbit/s raw data rate**
- **Bi-directional serial port for access to internal registers**
- **Complete zoned recording application support**
- **Low power operation (< 550 mW typical @ 45 Mbit/s and 5V)**
- **Programmable power management (Sleep mode < 1 mW)**
- **Power supply range (4.5 to 5.5V)**
- **Small footprint 64-pin TQFP package**

(continued)

PIN DIAGRAM



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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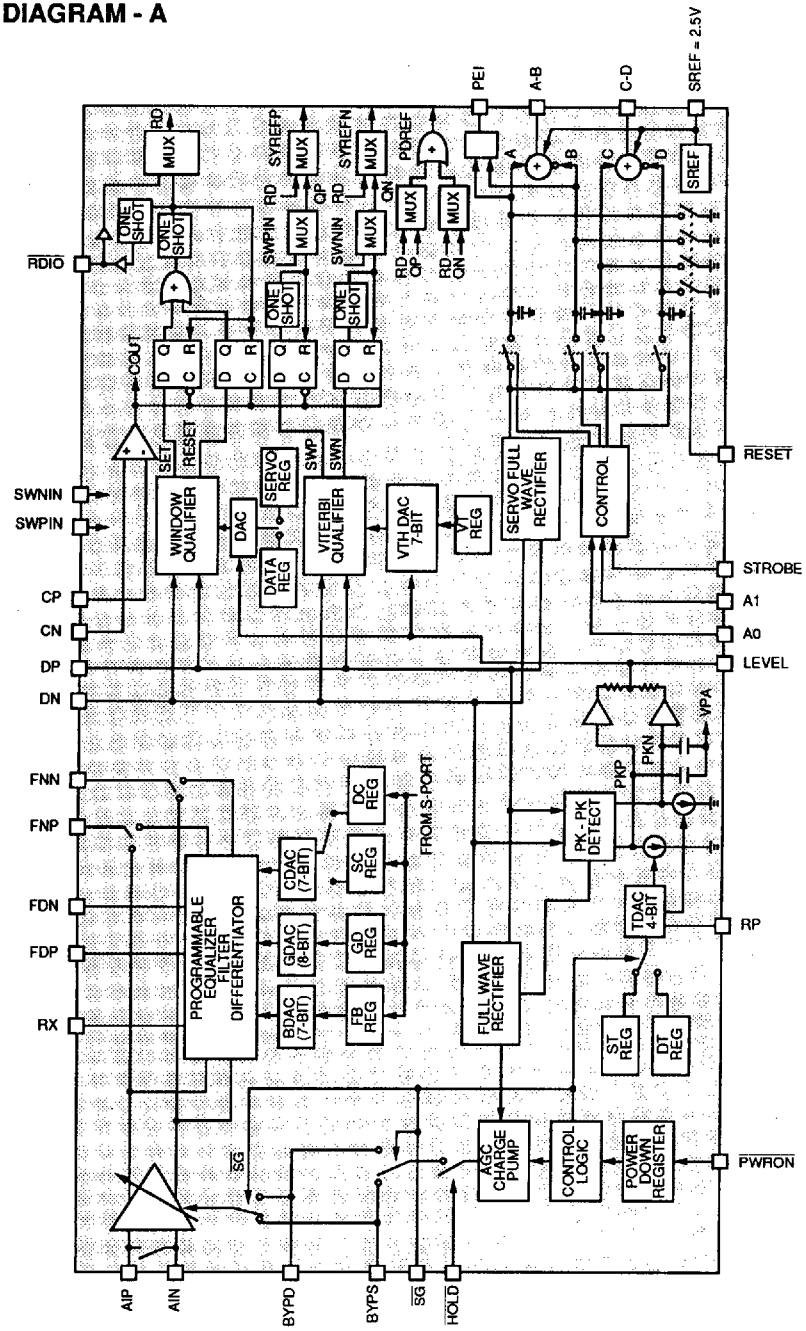
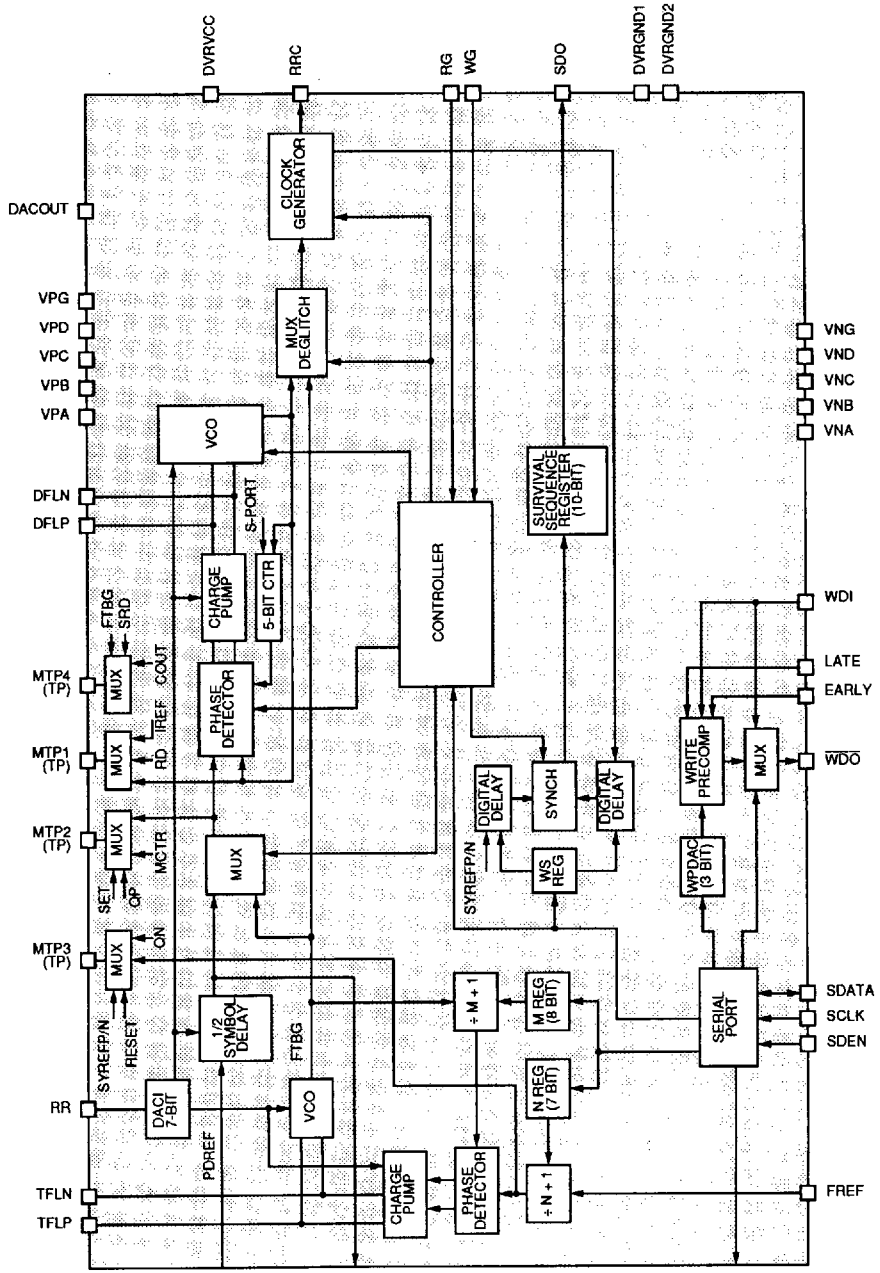
SSI 34P3400
45 Mbit/s Read Channel
w/Adaptive Threshold Qualifier

BLOCK DIAGRAM - A



BLOCK DIAGRAM - B



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SSI 34P3400
45 Mbit/s Read Channel w/Adaptive Threshold Qualifier

FEATURES (continued)

AGC

- Temperature compensated, exponential control AGC
- Fast attack/decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Low drift AGC hold circuitry
- Internal LOW-Z and fast decay timing for rapid transient recovery and AGC acquisition
- Fast decay mode is self-timed for optimal AGC recovery

PULSE DETECTOR

- Adaptive threshold qualifier for data extraction
- Traditional window qualifier for timing extraction
- Programmable pulse qualification threshold level
- CMOS $\overline{RDIO}$ signal output for servo timing support
- 0.5 ns max pulse pairing with sine wave input
- Independent window voltage qualification threshold in servo & data modes
- Independent qualification thresholds for data and timing extraction

SERVO CAPTURE

- 4-burst servo capture with PEI output, A-B, and C-D output
- Internal servo burst hold capacitors

PROGRAMMABLE FILTER

- Programmable cutoff frequency of 2 to 16 MHz
- Programmable boost of 0 to 13 dB
- Programmable group delay equalization (up to 30% change in group delay)
- Independent cutoff frequency setting in data mode and servo mode
- Boost setting available in data mode and servo mode
- Matched normal and differentiated outputs
- ±10% fc accuracy from 10 to 16 MHz
- Less than 1% total harmonic distortion from 10 to 16 MHz
- Less than 1.5% total harmonic distortion from 2 to 10 MHz

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 90 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SYNCHRONIZER

- Fully integrated data synchronizer
  - no external delay lines or active components required
  - no external active PLL components required
- Selectable PLL input from adaptive threshold qualifier or traditional window qualifier
- Selectable data synchronizer input from adaptive threshold qualifier or traditional window qualifier
- Fast PLL acquisition phase lock loop
  - zero phase restart technique
  - programmable phase detector gain gear shift
- Programmable decode window symmetry
  - window shift control ± 30% of decode window
  - includes delayed read data and VCO reference monitor points
- Programmable write precompensation
- External/Internal write precomp control
- PLL and data detection circuits capable of operating with d = 0 encoding

FUNCTIONAL DESCRIPTION

The SSI 34P3400 is a complete high performance read channel device with the following functions:

- AGC & adaptive threshold pulse qualification
- 4-burst servo demodulator
- programmable active filter
- time base generator
- data synchronizer

It supports raw data rates from 9 to 45 Mbit/s. Designed for low power applications, it allows completely flexible power management. Figure 1 shows the Block diagram of the device.

Most critical system parameters are user-programmable by writing to a bank of 8-bit registers. These registers can be written to or read back via a 3-line bi-directional serial interface. Upon application of power to the device, these registers must be written to an appropriate state as they will come up random data. However, they are not disturbed in a sleep mode power down.

AGC & PULSE DETECTOR DESCRIPTION

The adaptive threshold qualifier, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wideband variable gain amplifier, a wideband & high precision fullwave rectifier, a dual rate charge pump, and an advanced adaptive threshold qualifier. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The AGC amplifier gain is controlled by the voltage at:

- the BYPD pin if $\overline{SG}$ = '1', i.e., in non-servo mode, or
- the BYPS pin if $\overline{SG}$ = '0', i.e., in servo mode.

External integrating capacitors, CBYPD and CBYPS, should be connected between VCC and the BYPD pin and the BYPS pin, respectively.

In non-servo mode, a dual rate charge pump drives CBYPD with a charging/discharging current that depends on the instantaneous differential voltage at the DP/DN pins.

Attack currents, out of CBYPD, lower VBYPD which reduces the amplifier gain, while decay currents, into CBYPD, increase VBYPD which increases the amplifier gain. When the signal at DP/DN is greater than 1 Vp-pd (volt peak-to-peak differential), the nominal attack current of approximately 0.13 mA is used to reduce the amplifier gain. If the signal is greater than 1.25 Vp-pd, a fast attack current of approximately 1.04 mA is sunk to reduce the gain.

A constant decay current of approximately 3 µA acts to increase the amplifier gain when the signal at DP/DN is less than 1 Vp-pd. The large ratio (0.13 mA:3µA) of the nominal attack and nominal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. This dual rate approach allows the AGC gain to be decreased quickly when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A fast decay current mode is provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is increased by a factor of 20. The execution of fast decay is explained in the next section.

The FDCT bit in the Control A Register , when set to '1', forces the AGC charge pump into the continous fast decay test mode. In normal operation, this bit should be set to '0'. The nominal attack & fast attack remain active in the fast decay test mode. This FDCT bit is intended for device testing purposes only.

AGC CONTROL MODE

AGC Hold

The AGC action can be suspended by external control. Driving the $\overline{HOLD}$ pin to 0 forces the dual rate charge pump output current to zero. In this mode, V_{BYP_X} will be held constant subject to leakage current only.

Read Mode & Idle Mode

In the read mode (RG = 1, WG = 0 and $\overline{SG}$ = 1) or in idle mode (RG = 0, WG = 0 and $\overline{SG}$ = 1), the nominal decay, nominal attack and fast attack are active based on the instantaneous DP/DN voltage.

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AGC CONTROL MODE (continued)

Write Mode

With WG = 1, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. The device also enters the Low-Z mode in which the input impedances of both the AGC amplifier and the data qualifier are reduced.

After a write cycle, WG transitions from 1 to 0. The device remains in the Low-Z mode for 1µs for quick recovery of the AC coupling capacitors. Following this 1µs Low-Z mode, the AGC enters the fast decay mode for 1µs to allow rapid acquisition of the proper AGC level. The fast decay current will stay active until the signal reaches 125% or 1µs has elapsed, whichever comes first.

Pulse Detector Power Down

When the pulse detector is powered down, either by $\overline{\text{PWRON}}$ = 1 or setting the PD bit in the Power Down Register, the V_{BYP_X} will be held constant subject to leakage current only. Upon power-up, the Low-Z/fast decay sequence is executed to rapidly recover from any transients or drift which may have occurred on the BYPX hold capacitor.

The servo AGC is discussed in the next section. At the end of a servo cycle, $\overline{\text{SG}}$ transitions from 0 to 1 and the fast decay is executed for 1µs.

Servo AGC

When $\overline{\text{SG}}$ transitions from 1 to 0, i.e. into servo mode, the following events occur:

- the AGC loop is switched from the BYPD pin to the BYPS pin
- the filter cutoff is switched to the setting specified in the Servo Cutoff Register
- the filter boost is disabled if SB = 0
- the PKP and PKN decay current is controlled by the servo threshold decay, TS
- qualification threshold percentage of the window qualifier is controlled by the Servo Threshold Register

The servo AGC action is identical to that in the data mode. The AGC charge current is supplied by the AGC charge pump into/out of the BYPS pin.

Adaptive Threshold Qualifier

The adaptive threshold qualifier performs amplitude qualification using a floating threshold level. The absolute threshold level is continuously calculated based upon the amplitude of the previous significant pulse. The previous significant pulse is defined to be either the opposite polarity pulse or the most recent same polarity pulse which exceeded the absolute threshold set earlier. While the absolute threshold levels float with the signal amplitude, the threshold window (defined to be the distance between the positive threshold & the negative threshold) is programmable as a percentage of the peak-to-peak amplitude.

The floating threshold method offers two main advantages. It makes an excellent qualifier to use with asymmetrical signals because it does not assume that the qualification window must be centered around zero. It is able to adapt its qualification window around the mean of the peak to peak signal levels. As a second advantage, it will allow consutive same polarity peaks to be detected. Yet, it differs from the window qualifier approach in that only the highest amplitude peak will survive instead of all qualified peaks.

The qualifier accepts as inputs the low pass filtered read signal from the filter and a half threshold window voltage, VTH. Based on VTH and the absolute qualification threshold computed from the previous significant pulse, the qualifier outputs two digital pulse streams (SW+ and SW-). SW+ goes high when the signal exceeds the absolute positive threshold, SW- goes high when the signal falls below the absolute negative threshold (Figure 3). A small amount (20%) of hysteresis is provided at the threshold level to stretch out the falling edges of the output pulses. This eases the timing requirements for the timing detector.

A peak to peak detector is used to generate the half threshold window voltage, VTH, as a percentage of the incoming read signal. It operates by storing the amplitude of both the positive and negative peaks on the internal hold capacitors connected to PKP and PKN, respectively. Programmable pull down currents are provided on the PKP and PKN nodes to set the decay time of the capacitor voltage. The pull down current is controlled by the 4-bit T-DAC, which has independent inputs in the data mode or the servo mode. The voltages on PKP and PKN are buffered and averaged to determine the peak-to-peak amplitude. This average voltage is provided on the LEVEL pin. The LEVEL pin can be used to monitor

the average voltage, to filter the voltage, or to set the threshold voltage with an external source. The voltage at the LEVEL pin drives a 7-bit multiplying DAC that is used to set the threshold voltage, V_{TH}. A minimum threshold clamp circuit prevents the threshold voltage from going below a minimum setting of:

$$V_{TH}\ (min) = 0.1 \bullet VTHDAC/127$$

This helps to prevent false pulses which might occur when no read signal is applied. Mathematically, the above can be summarized as:

V @ PKP = Peak of (DP - DN) + V_{RC}

V @ PKN = Peak of (DN - DP) + V_{RC}

V @ LEVEL = 0.69 • (V @ PKP + V @ PKN) + V_{RC}

V_{RC} = Internal bandgap reference from VPG = ~ 2.7V with VPG = 5V

V_{TH} = 0.72 • (V @ LEVEL - V_{RC}) • VD/127, where VD = 7-bit DAC code

Qual % = 2 • VTH/(DP/DN Peak-to-Peak)

Qual % = 100% • VD/127 where $0 \le VD \le 127$

Because the AGC circuit is based on the fullwave rectified DP/DN, it will force the DP/DN signal to 0.5 Vp-pd (zero-to-peak differential). With an asymmetrical read signal, the peak-to-peak differential signal at DP/DN will be less than 1 Vp-pd.

The SW+ and SW- signals are then used to qualify the clock signal which is generated by detecting zero crossings on the filter differentiated output applied to CP/CN. A clock signal that occurs while the signal is above the positive threshold or below the negative threshold produces a read data pulse (RD). This pulse stream is used to drive the PLL circuit in the data synchronizer. When the VCO has become phase-locked to the read data signal, a read reference clock (RRC) becomes available. The read data signal is then synchronized to the RRC which then feeds a steering circuit. The steering circuit divides the read data bit stream into synchronized positive and negative bit streams, RDP and RDN (Figure 4). RDP and RDN are fed into a survival sequence register to generate synchronized read data that can be decoded. The survival sequence register is designed to reject the early pulses of the same polarity which were not followed immediately by a pulse of the opposite polarity.

TABLE 1: Nominal Values of PKP and PKN Current Sources

Gives the nominal values of the PKP and PKN current sources for each DAC bit and for each mode, allowing a calculation of decay rate for each DAC setting. The internal capacitors of the peak-to-peak detector are a nominal 6 pF each.

DATA MODE					SERVO MODE				
TD3	TD2	TD1	TD0	PKP, PKN	TS3	TS2	TS1	TS0	PKP, PKN
0	0	0	1	0.13 µA	0	0	0	1	0.065 µA
0	0	1	0	0.26 µA	0	0	1	0	0.13 µA
0	1	0	0	0.52 µA	0	1	0	0	0.26 µA
1	0	0	0	1.04 µA	1	0	0	0	0.52 µA

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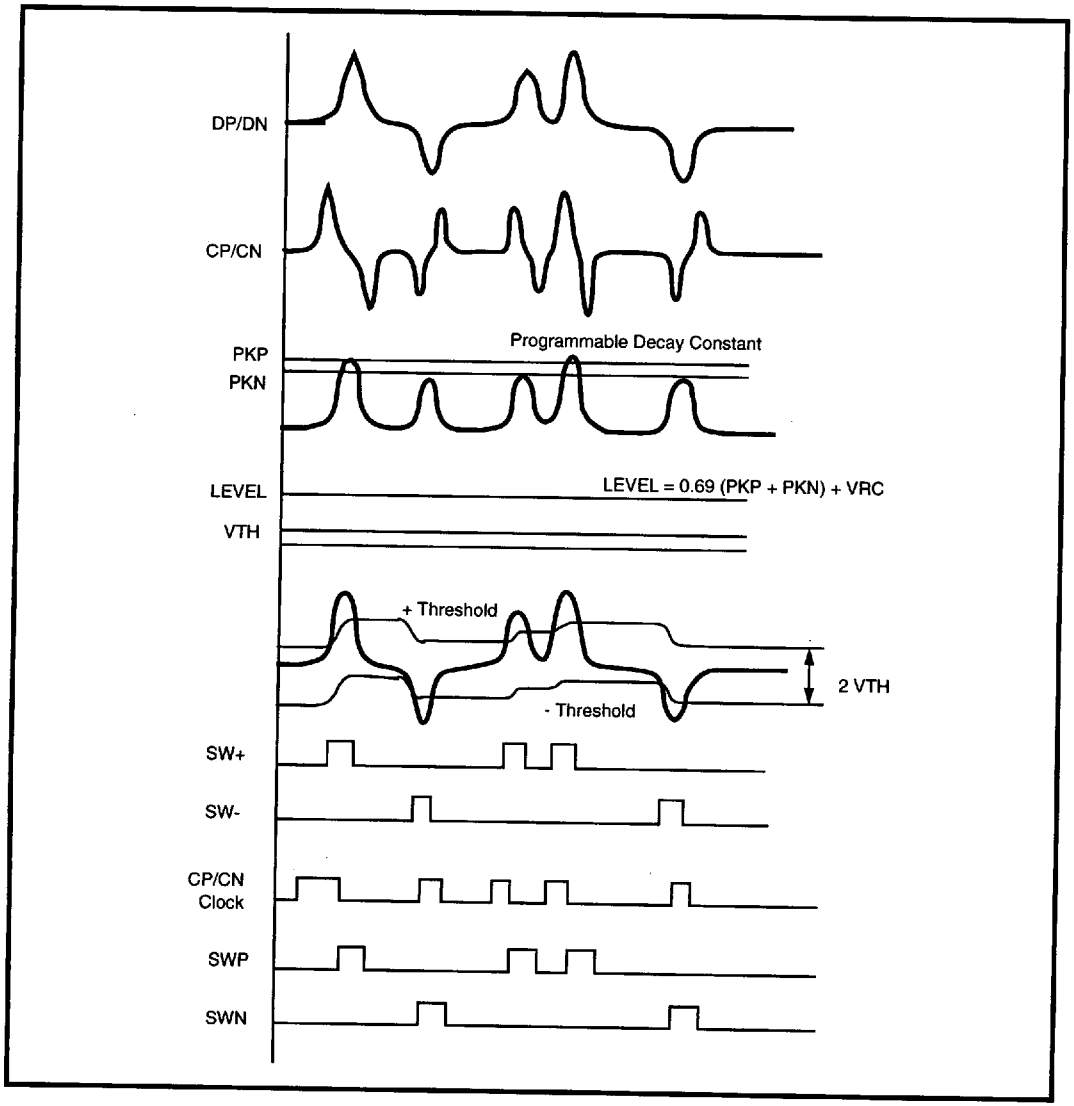

FIGURE 3: Adaptive Threshold Qualifier Timing

AGC & PULSE DETECTOR DESCRIPTION (continued)

Window Qualifier

In addition to the Adaptive Threshold Qualifier, the SSI 34P3400 also provides a traditional window qualifier for minimal noise disturbance in timing recovery.

In window threshold qualification mode, independent positive and negative threshold qualification comparators are used. Any peak, regardless of polarity, which exceeds the programmed threshold level triggers the read data one-shot. Qualification thresholds from 0% to 100% may be set with a resolution of 1%. The independent positive and negative thresholds are set symmetrically about ground. Separate qualification thresholds are available for data and servo modes.

A slight amount of local hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator.

$\overline{\text{RDIO}}$ Output Pin

A CMOS compatible, 23 ns wide(min), inverted Read Data I/O ($\overline{\text{RDIO}}$) is provided to monitor the traditional peak detector output. This pin will be held high when either RG or WG are high to reduce noise and accompanying jitter during read or write modes. Its falling edge indicates the occurence of valid data pulse from the window qualifier. This pin can be configured as an input pin for testing the data synchronizer by setting RDI = 1 in the Control B Register.

PROGRAMMABLE FILTER DESCRIPTION

Ideal for constant density application, the SSI 34P3400 includes a programmable low pass filter with the following four key features:

- programmable cutoff frequency from 2 to 16 MHz
- programmable boost from 0 to 13 dB at the cutoff frequency
- programmable phase equalization
- normal low pass output and time-differentiated output

The normal low pass filter is of a seven-pole two-real-zero type. Figure 6 illustrates the normalized transfer function. While the cutoff frequency is scaled with replacing s by $s/2\pi fc$, the boost & group delay equalization are controlled by varying the α and β.

With a zero at the origin, the filter provides a time-differentiated filter output. This is used in time qualification of the peak detection. To ease the timing requirement in peak detection of a signal slightly above the qualification threshold, the time-differentiated output is purposely delayed by 1.2 ns relative to the normal low pass output.

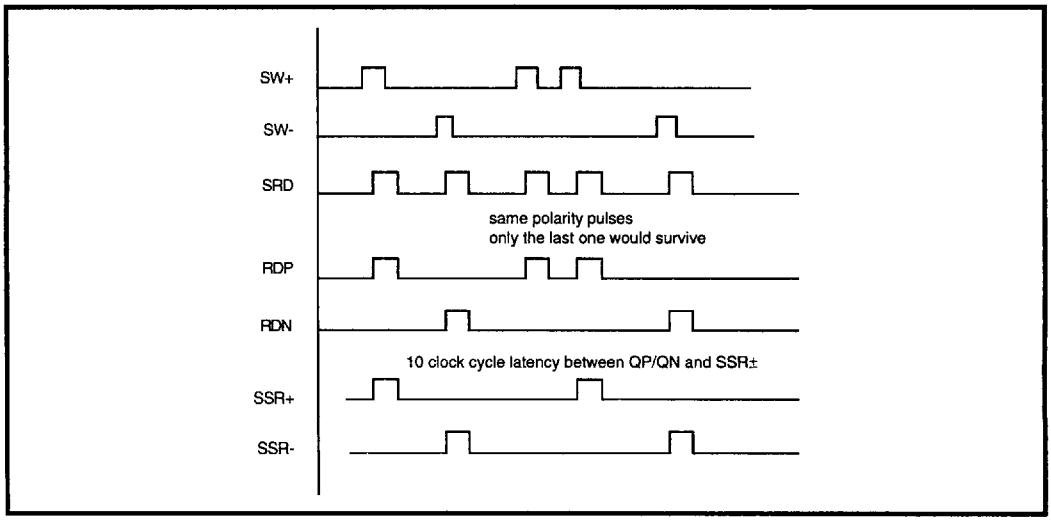

FIGURE 4: Steering Circuit & Survival Register Functionality

FUNCTIONAL DESCRIPTION (continued)

PROGRAMMABLE FILTER DESCRIPTION

The normal low pass output feeds the data qualifier (DP/DN), and the differentiated output feeds the clock comparator (CP/CN).

Five definitions are introduced for the programmable filter control discussion (Figure 7):

Cutoff Frequency: The cutoff frequency is the -3 dB low pass bandwidth with no boost & group delay equalization, i.e., $\alpha = 0$ and $\beta = 0$.

Actual Boost: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha \neq 0$ and/or $\beta \neq 0$.

Alpha Boost: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha \neq 0$ and without group delay equalization. In general, the actual boost with group delay equalization is higher than the alpha boost. However, with >3 dB alpha boost, the difference is minimal.

Group Delay Δ%: The group delay Δ% is the percentage change in absolute group delay at DC with respect to that without equalization applied ($\beta = 0$).

Group Delay Variation: The group delay variation is the change in group delay from DC to the cutoff frequency. This can be expressed as a percentage defined as: (change in group delay ÷ absolute group delay with $\beta = 0$) • 100%. An alternative is to express the group delay variation in nanoseconds. Because the absolute group delay variation in nanoseconds is scaled by the programmed cutoff frequency, the percentage expression is used in this specification.

Filter Operation

Direct coupled differential signals from the AGC amplifier output are applied to the filter. The programmable bandwidth and equalization characteristics of the filter are controlled by 3 internal DACs (C, B, and G). The five registers for these DACs are programmed through the serial port. The current reference for the DACs is set using a single external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current. This establishes the excellent temperature stability for the filter characteristics.

The cutoff frequency can be set independently in the servo mode and the data mode. In the data mode, the cutoff frequency is controlled by the Data Cutoff (DC) Register. In the servo mode, the cutoff frequency is controlled by the Servo Cutoff (SC) Register. The boost function is controlled by the Filter Boost (FB) Register contents and by $\overline{SG}$. In the data mode, the boost function is controlled by the register contents only. In the servo mode, boost is also set by the register, but if the MSB is 0, boost is disabled.

Cutoff Control

The programmable cutoff frequency from 2 to 16 MHz is set by the 7-bit linear CDAC. The DC and SC registers hold the 7-bit CDAC control value. The cutoff frequency is set as:

$$fc\ (\text{MHz}) = 0.125984 \bullet \text{CDAC}\ 0 \leq \text{CDAC} \leq 127$$

The filter cutoff (fc) is defined as the -3 dB bandwidth with no boost applied. When boost/equalization is applied, the actual -3 dB point will move out. The ratio of the actual -3 dB bandwidth to the programmed cutoff is tabulated in Table 2 as a function of applied boost & group delay equalization.

Boost Control

The programmable alpha boost from 0 to 13 dB is set by the 7-bit linear BDAC. The DB and SB registers hold the 7-bit DAC control value. The alpha boost is set as:

$$\text{Alpha Boost (dB)} = 20 \log [0.0273 \bullet \text{BDAC} + 1]\ 0 \leq \text{BDAC} \leq 127$$

The programmed alpha boost is the magnitude gain at the cutoff frequency with no group delay equalization. When finite group delay equalization is applied, the actual boost is higher than the programmed alpha boost. However, the difference becomes negligible when the programmed alpha boost is >3 dB. Table 3 tabulates the actual boost as a function of the applied alpha boost & group delay equalization.

Group Delay Equalization

The group delay Δ% can be programmed between -30% to +30% by the 8-bit linear GDAC. The GD register holds the 8-bit DAC control value. The group delay Δ% is set as:

$$\text{Group Delay } \Delta\% = 0.2362 \bullet (\text{GD} - 128) \bullet 1\%,\ 0 < \text{GD} \leq 255$$

The group delay Δ% is defined to be the percentage change of the absolute group delay due to equalization from the absolute group delay without equalization at DC.

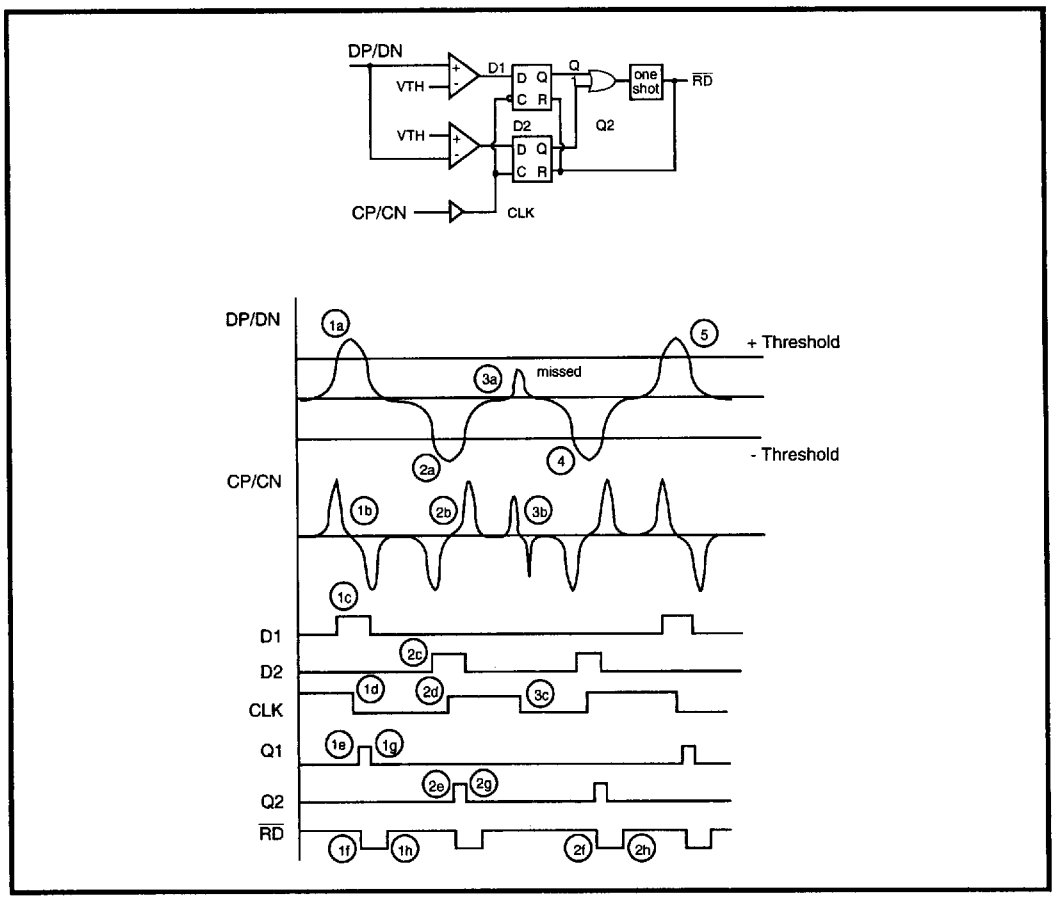

FIGURE 5: Window Threshold Qualification

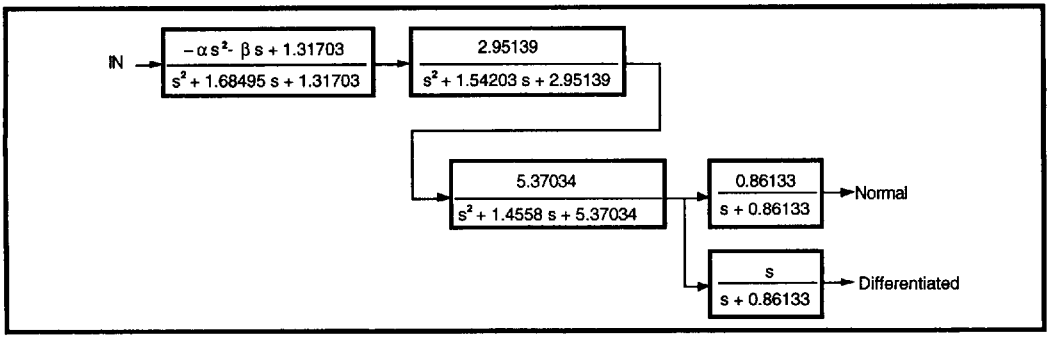

FIGURE 6: Programmable Filter Normalized Transfer Function

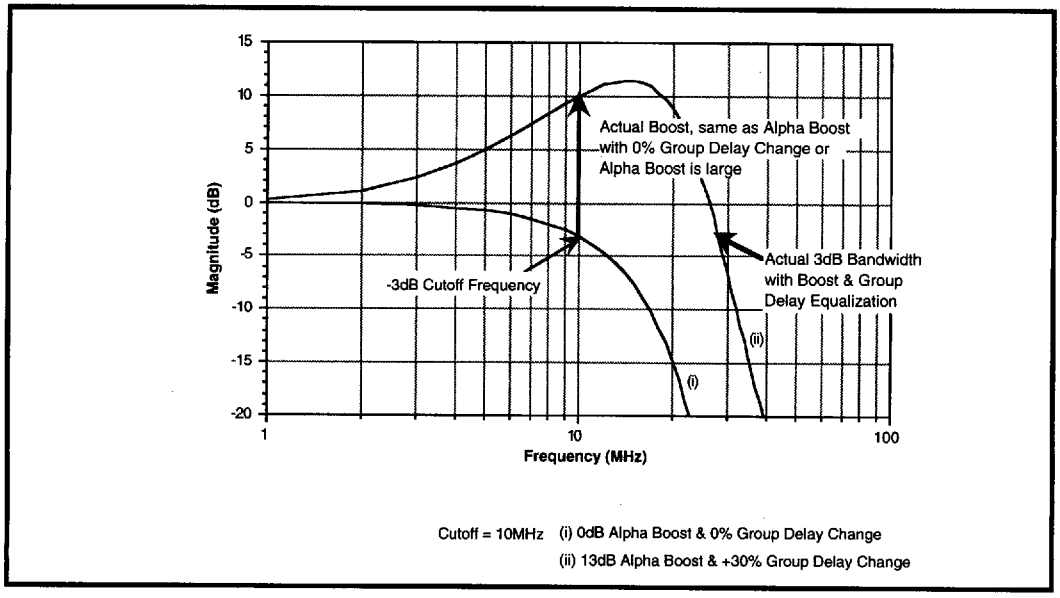

FIGURE 7a: Filter Magnitude Response

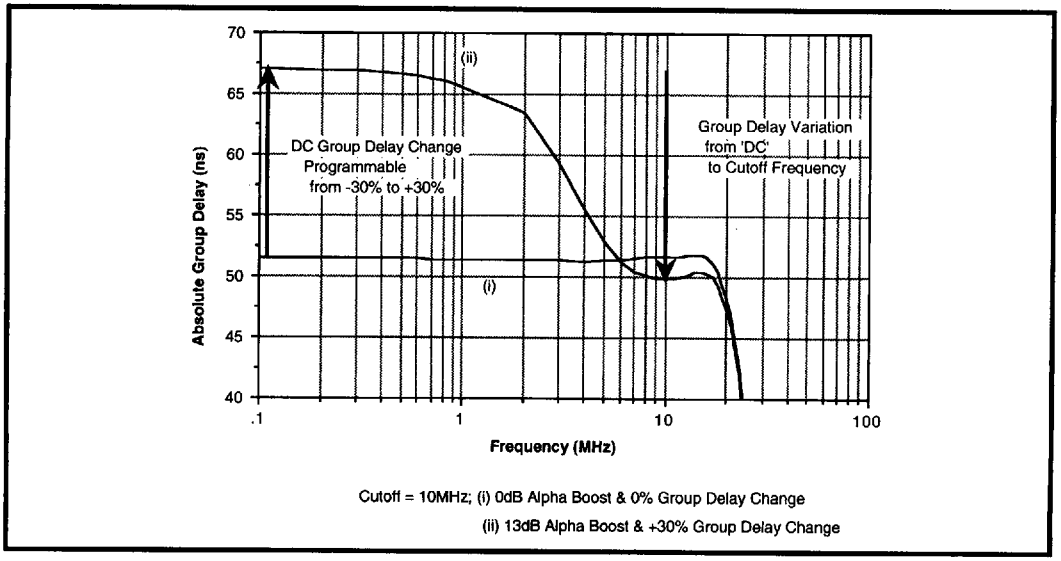

FIGURE 7b: Filter Group Delay Response

TABLE 2: Ratio of Actual -3 dB Bandwidth to Cutoff Frequency

ALPHA	GROUP DELAY Δ%						
BOOST	±30%	±25%	±20%	±15%	±10%	±5%	0%
0 db	1.58	1.45	1.30	1.17	1.07	1.02	1.00
1	1.67	1.57	1.47	1.36	1.27	1.21	1.19
2	1.78	1.71	1.64	1.56	1.50	1.46	1.44
3	1.90	1.85	1.80	1.76	1.72	1.70	1.69
4	2.01	1.98	1.96	1.93	1.91	1.90	1.90
5	2.13	2.11	2.09	2.08	2.07	2.06	2.06
6	2.23	2.22	2.21	2.20	2.20	2.20	2.20
7	2.33	2.32	2.32	2.31	2.31	2.31	2.31
8	2.42	2.41	2.41	2.41	2.41	2.40	2.40
9	2.50	2.50	2.50	2.49	2.49	2.49	2.49
10	2.58	2.58	2.58	2.58	2.57	2.57	2.57
11	2.66	2.66	2.66	2.66	2.66	2.66	2.66
12	2.73	2.73	2.73	2.73	2.73	2.73	2.73
13	2.80	2.80	2.80	2.80	2.80	2.80	2.80

TABLE 3: Actual Boost vs Alpha Boost & Group Delay Change

ALPHA	GROUP DELAY Δ%						
BOOST	±30%	±25%	±20%	±15%	±10%	±5%	0%
0 db	2.92	2.21	1.54	0.93	0.44	0.12	0.00
1	3.46	2.84	2.27	1.76	1.35	1.07	1.00
2	4.05	3.52	3.03	2.61	2.28	2.17	2.00
3	4.26	4.25	3.84	3.49	3.23	3.06	3.00
4	5.40	5.02	4.68	4.40	4.18	4.05	4.00
5	6.15	5.83	5.55	5.32	5.15	5.04	5.00
6	6.94	6.67	6.44	6.25	6.12	6.03	6.00
7	7.76	7.54	7.36	7.20	7.09	7.02	7.00
8	8.61	8.44	8.28	8.16	8.07	8.02	8.00
9	9.50	9.35	9.22	9.13	9.06	9.02	9.00
10	10.40	10.30	10.20	10.10	10.10	10.00	10.00
11	11.30	11.20	11.10	11.10	11.00	11.00	11.00
12	12.30	12.20	12.10	12.10	12.00	12.00	12.00
13	13.20	13.10	13.10	13.10	13.00	13.00	13.00

FUNCTIONAL DESCRIPTION (continued)

SERVO DEMODULATOR DESCRIPTION

The SSI 34P3400 supports 4-channel servo burst detection in any desired sequence. The signal at the DP/DN pins is full-wave-rectified and applied to four peak detectors, each with its own 10pf memory capacitor. The capacitors are reset to zero at the beginning of a servo acquisition interval by driving the $\overline{\text{RESET}}$ pin low.

The 2-bit address word, A0 and A1, selects which peak detector is to be activated. When the STROBE pin is driven high, the selected peak detector capacitor is charged to the peak value of the servo burst through a series resistance. When the STROBE pin falls low, the voltage on the memory capacitor remains constant until reset, except for slow drift caused by leakage currents.

A1	A0	Channel
0	0	A
0	1	B
1	0	C
1	1	D

Noise immunity is enhanced by the integration effect of the series resistance in each peak detector. The time constant is controlled by a 3-bit word (SD0-SD2) in the Gain Shift register. Nominal time constants are defined as follows:

SD2	SD1	SD0	Time Constant
0	0	0	0.1 µs
0	0	1	0.2 µs
0	1	0	0.3 µs
0	1	1	0.4 µs
1	0	0	0.5 µs
1	0	1	0.6 µs
1	1	0	0.7 µs
1	1	1	0.8 µs

The capacitor voltage is buffered to minimize leakage current and amplified to restore the channel gain to 1 referenced to the DP/DN pins. Two servo outputs are provided: A-B and C-D, each with a dynamic range of ±1V into a 10 kΩ load. An internal bandgap reference voltage of 2.5V (SREF) provides the zero-signal baseline for each output. The reference is also available on its own pin for external use.

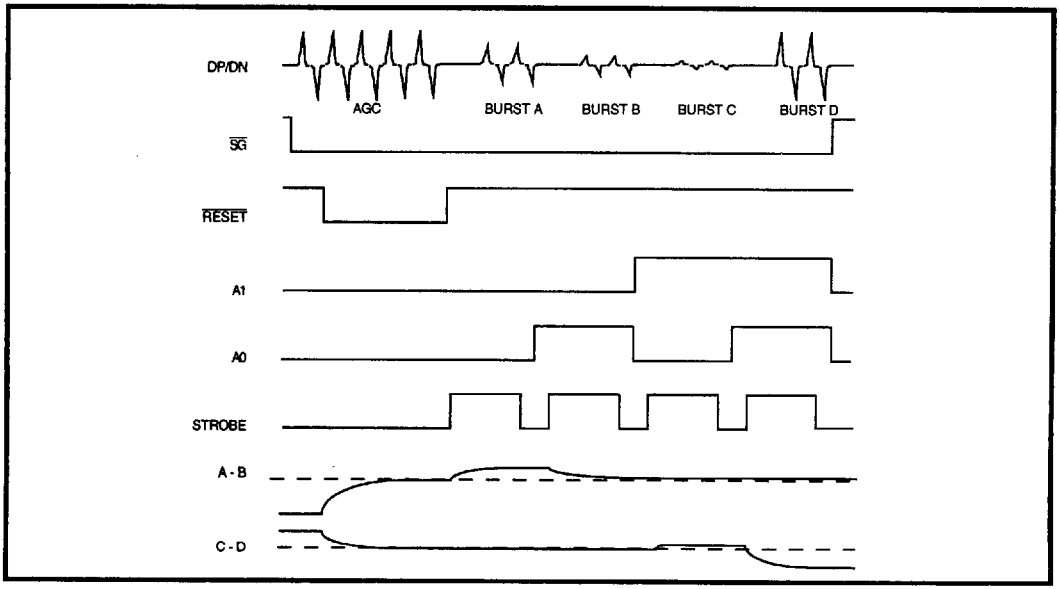

FIGURE 8: Servo Sample Timing Diagram

The servo demodulator also provides a digital Position Error Indicator (PEI) output. The A-B output voltage is continuously compared to two thresholds equally spaced above and below the zero-signal level SREF. The spacing is controlled by a 6-bit word in the Position Error register, and can be varied from 0.1 to 1V. Any excursion of the A-B servo signal outside of either threshold level will cause the PEI pin to switch to the high state.

TIME BASE GENERATOR DESCRIPTION

The time base generator, a PLL based circuit, provides a programmable reference frequency to the data synchronizer for constant density recording applications. The data synchronizer reference frequency runs at 2 times the read reference clock. This time base generator output frequency can be programmed with a better than 1% accuracy via the M, N and DR Registers.

The time base generator requires an external passive loop filter to control its PLL locking characteristics. This filter is fully-differential and balanced in order to suppress the common mode noise generated, for example, from the data synchronizer's PLL.

In read, write and idle modes, the time base generator is programmed to provide a stable reference frequency for the data synchronizer. In write and idle modes, the MTP4 pin (a multiplexed test point output) can be configured as the output of the time base generator. This test point can be disabled by resetting the TP4E bit in the Control A Register. To minimize jitter coupled to the data synchronizer PLL in read mode, the time base generator output test point is disabled after the internal VCO lock signal is asserted (i.e. after 19 positive transitions). The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$F_{TBG} = FREF\ [(M + 1) \div (N + 1)]$$

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The DR register must be set to the correct VCO center frequency. The time base generator PLL responds to any changes to the M and N registers, only after the DR register is updated.

The DR register value, with an external 49.9 kΩ RR resistor, sets the following:

- center frequency of the time base generator VCO
- center frequency of the data synchronizer VCO
- phase detector gain of the time base generator phase detector
- phase detector gain of the data synchronizer phase detector
- 1/2 symbol delay in the data synchronizer

The VCO center frequency is programmed by the following equation and should be set close to 2 times the read reference clock.

$$FVCO\ (MHz) = (0.746 \bullet DR) + 6.8$$

DATA SYNCHRONIZER DESCRIPTION

In the read mode, the data synchronizer performs sync field search and data synchronization. In the write mode, the circuit provides write precompensation. Data rate is established by the time base generator and the interval reference DACI controlled by the DR register. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/2 symbol delay.

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a read data pulse. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency (from the Time Base Generator). By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO phase transient is minimized and false lock to read data is eliminated.

The phase detector incorporates a differential charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is again fully-differential and balanced in order to suppress the common mode noise generated from the Time Base Generator's PLL.

DATA SYNCHRONIZER DESCRIPTION (continued)

The READ GATE (RG) and WRITE GATE (WG) inputs control the device operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output write data pulse. The RG and WG inputs are overridden when $\overline{SG}$ is driven low. If RG and WG inputs are driven high simultaneously, the device goes into idle mode.

RG	WG	$\overline{SG}$	MODE
X	X	0	Servo
0	0	1	Idle
0	1	1	Write
1	0	1	Read
1	1	1	Idle

Clock Extraction & Data Synchronizer Source

In data recovery, a clock signal must be extracted from the serial bit stream to establish the proper decode window. In the write mode, the PLL is frequency locked to the time base generator output. In the read mode, the SSI 34P3400 offers flexibility in selecting the reference sources to the data synchronizer phase locked loop and data synchronizer.

The PDREF bit in the Window Shift Register selects the PLL reference input source. If PDREF = '1', the PLL is phase locked to the window qualifier output. If PDREF = '0', it is locked to the Viterbi qualifier output.

Assuming a clock is extracted and the proper decode window is established, the data bit is re-synchronized. The data input source to the data synchronizer is also user programmable via the DSREF bit in the Window Shift Register. If DSREF = '1', the window qualifier output is used. If DSREF = '0', the Viterbi qualifier output is used.

Read Operation

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal RD input and low level selects the reference clock.

Each qualified RD pulse triggers the 1/2 symbol delay one-shot to generate the delayed read data pulse ($\overline{DRD}$).

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO ÷ 2. As depicted in Figure 9, $\overline{DRD}$ is a half code period pulse whose leading edge is defined by the leading edge of read data RD. A decode window is developed from the falling edges of the VCO ÷ 2 clock.

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Register and programmed through the serial port.

In the non-read modes, the PLL is locked to the reference clock coming from the Time Base Generator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next $\overline{DRD}$ input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

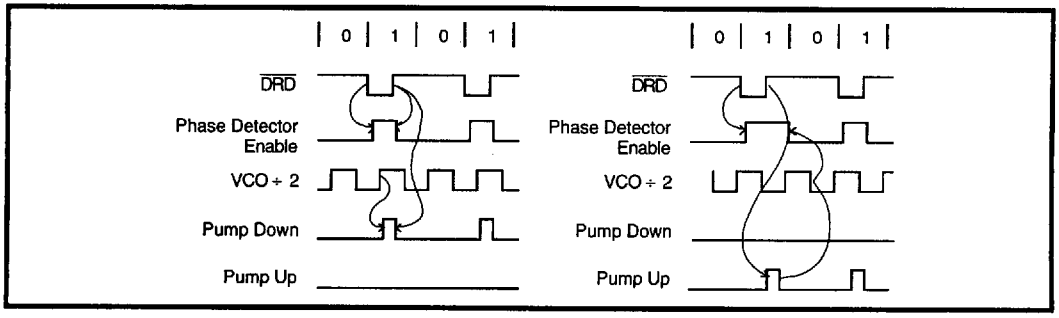

FIGURE 9: Data Synchronizer Phase Detector Data Locking Mechanism

Preamble Search

After Read Gate (RG) has been asserted, an internal counter is clocked by positive transitions of the incoming read data, RD. Once the counter reaches count 3 (3 consutive positive transitions found) the internal read gate enables, switching the phase detector from the reference clock to the delayed read data input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data.

VCO Lock and Bit Sync Enable

The SSI 34P3400 data synchronizer PLL phase detector has two operating modes: high gain mode and constant gain mode.

In non-read mode, the phase detector gain remains at a nominal level. Following the 3rd $\overline{DRD}$ transition after RG rise, the phase detector gain is increased to 3X nominal for fast acquisition.

If the GS bit in the Control B Register is reset to 0, the phase detector gain remains at the 3X nominal for the entire read cycle.

If the GS bit in the Control B Register is set to 1, the phase detector gain stays at the 3X nominal for a specified number of RRC periods into the read cycle. The phase detector gain then returns to the 1X nominal for lower bandwidth and better jitter performance.

The Gain Shift Register contains a 5-bit code which is loaded into an internal 5-bit counter. If the GS bit in the Control B Register is set to 1, the counter is decremented at each RRC period. When the counter reaches 0, the phase detector gain returns to the 1X nominal level.

After the internal read gate is enabled (i.e., following 3 $\overline{DRD}$ transitions after RG is asserted), the data synchronizer PLL starts to lock onto $\overline{DRD}$. After 16 additional transitions, an internal VCO lock signal is asserted. The RRC clock switches from TBG VCO ÷ 2 to Data Synchronizer VCO ÷ 2. No short duration pulses will occur in this transition. The raw data output, SDO, which is inactive in non-read mode, is a low impedance output. The bit synchronization circuitry is activated.

The SSI 34P3400 outputs raw data in a single bit serial data format at the SDO pin. The bits are ordered sequentially, with the RRC data clock running at one-half times the VCO frequency (equal to the raw data rate), or 45 MHz at the maximum raw data rate of 45 Mbit/s.

Write Mode

Write mode is entered by asserting Write Gate (WG) while the RG is held low. During write mode the VCO and the RRC are referenced to the internal time base generator signal.

Direct Write Function

The SSI 34P3400 includes a Direct Write (DW) function that allows the WDI data to bypass the write precomp circuitry. When the DW bit is set in Control B Register, the data applied to WDI will bypass the write precomp and directly control the WDO output buffer. This allows the user to perform DC erase and media tests.

Write Precompensation

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The write precompensation magnitude is set using the Write Precomp Register.

The SSI 34P3400 also allows external control of write precompensation through the Early and Late pins. External control of precomp is enabled by setting the XWP bit in the Write Precomp Register.

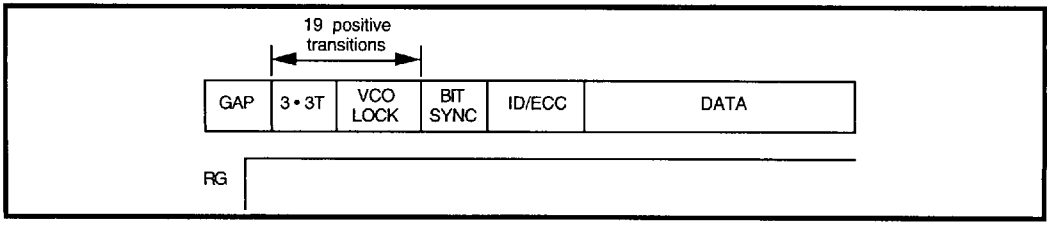

FIGURE 10: VCO Lock and Bit Sync Enable

FUNCTIONAL DESCRIPTION (continued)

SERIAL PORT INTERFACE & REGISTER DEFINITIONS

The serial port interface is a bi-directional data port for writing to internal registers and reading the contents of internal registers. The serial port is enabled for data transfers when the Serial Data Enable (SDEN) pin is high ("1"). SDEN should be asserted high prior to any transmission and it should remain high until the completion of the transfer. At the end of each transfer SDEN should be brought low ("0").

When SDEN is high, data applied to the Serial Data (SDATA) pin can be clocked into the device. The data is clocked serially into an internal shift register on each rising edge of the Serial Clock (SCLK). The SCLK should toggle only when a valid bit of address/instruction or data is being transferred across the serial data line. Serial data is transmitted across the interface in 16-bit packets. If more than 16 SCLK pulses are received during the time that SDEN is high, the additional SCLK and SDATA information will be ignored. During a serial data transmission, if SDEN is switched low before 16 SCLK pulses are received, that serial transmission will be aborted. For all valid transmissions, the data is latched into the internal register on the falling edge of SDEN.

Each transmission includes 1 R/W instruction bit, 7 address bits and 8 data bits. The instruction bit is used as a flag to put the port into read mode or write mode. The address bits select the internal register to be written to or read from (depending on the state of the R/W bit.) The address and data fields are input LSB first, MSB last, where LSB is defined as Bit 0. Figure 14 shows the serial interface timing diagram.

POWER MANAGEMENT MODES

The power management modes are controlled by the $\overline{\text{PWRON}}$ input and/or the control bits of the Power Down Register.

The two most common power management modes are full power down (sleep mode) and servo mode. In the sleep mode, both the front end (the pulse detector, servo demodulator, and filter) and the back end (the data synchronizer and time base generator) are powered off. This mode is activated by having $\overline{\text{PWRON}}$ pin '1'. Note that the serial port interface is always active.

In the servo mode, all circuitry in the front end is active. In the back end, the PLLs of both the data synchronizer and the time base generator are also powered up. In a servo mode that requires the PLLs to be shut down, the DS and TBG bits of the PD register should be set high ("1") to disable these circuits.

When the $\overline{\text{PWRON}}$ bit is low ("0"), all blocks that have their corresponding control bit set to high ("1") are powered off. Thus each section of the device can be powered down individually through the Power Down Register.

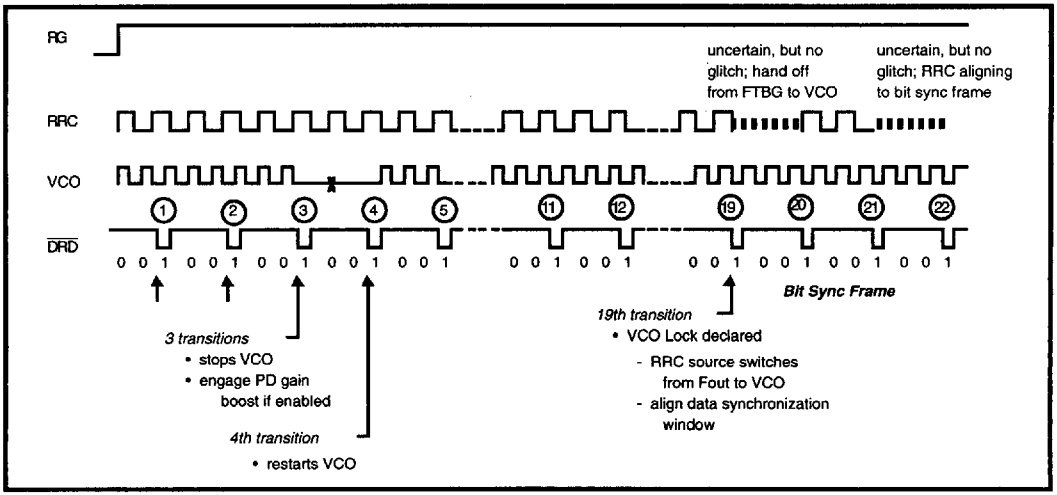

FIGURE 11: Read Sequence Timing

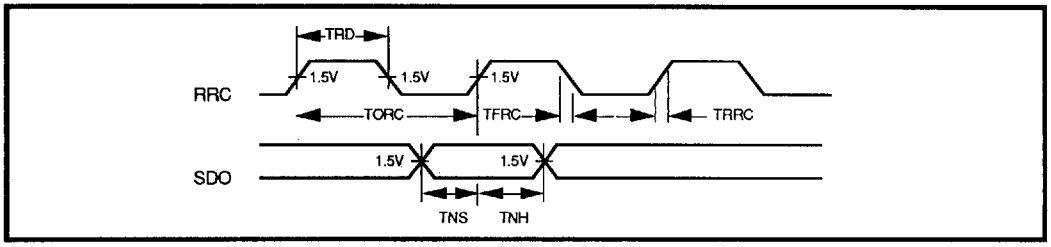

FIGURE 12: Read Data Timing

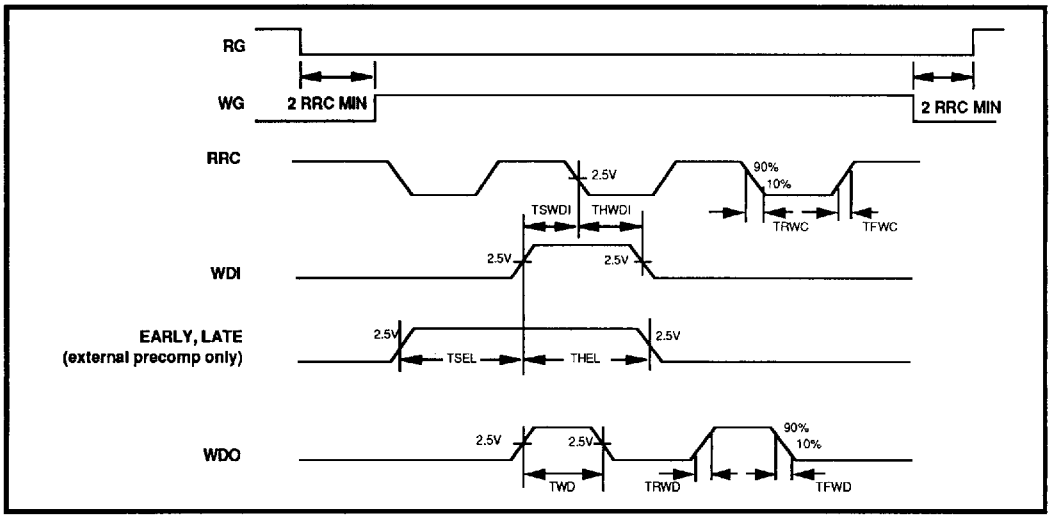

FIGURE 13: Write Mode Data Timing

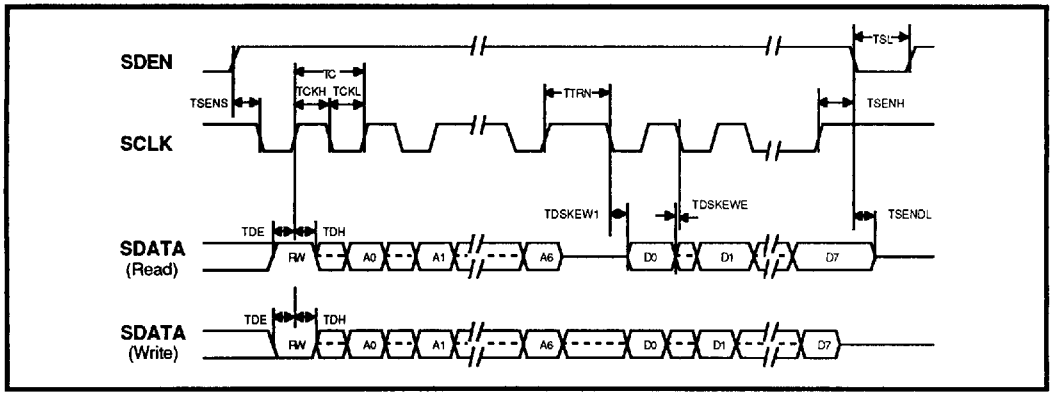

FIGURE 14: Serial Interface Timing Diagram

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REGISTER DESCRIPTION

Eighteen internal registers are used to configure the SSI 34P3400. Each register definition is as follow:

Power Down Control Register		(Address = 000 0010 = 02h = 2d)
Bit 7 (MSB)	BIT 1	CMOS output buffer speed control bit (MSB)
Bit 6	BIT 0	CMOS output buffer speed control bit (LSB) BIT 1,0 00 = slow 01 = medium 10 = fast 11 = very fast
Bit 5	X	Not used; don't care
Bit 4	TBG	Time Base Generator power down
Bit 3	DS	Data synchronizer power down
Bit 2	FLTR	AGC/Filter gain fixed to 1 V/V
Bit 1	SD	Servo Demodulator power down
Bit 0	PD	Pulse Detector/Filter power down 1 = power down; 0 = power up
Data Cutoff Register		(Address = 000 0011 = 03h = 3d)
Bit 7 (MSB)	DCBYP	Bypass Filter function 1 = filter bypassed-FNP/FNN is AGC amp output 0 = filter in use
Bits 6-0	DC6-0	Data cutoff frequency setting fc (MHz) = 0.125984 • DC $0_{dec} \leq DC \leq 127_{dec}$
Servo Cutoff Register		(Address = 001 0011 = 13h = 19d)
Bit 7 (MSB)	SCBYP	Bypass Filter function 1 = filter bypassed-FNP/FNN is AGC amp output 0 = filter in use
Bits 6-0	SC6-0	Servo cutoff frequency setting fc (MHz) = 0.125984 • SC $0_{dec} \leq SC \leq 127_{dec}$
Filter Boost Register		(Address = 000 1011 = 0Bh = 11d)
Bit 7 (MSB)	SB	Boost enable in servo mode 1 = enabled; 0 = disabled
Bits 6-0	FB6-0	Filter alpha boost setting Alpha Boost (dB) = 20 log [0.0273 • DB +1] $0_{dec} \leq DB \leq 127_{dec}$
Viterbi Threshold Register		(Address = 010 1010 = 2Ah = 42d)
Bit 7 (MSB)	X	Not used; don't care
Bits 6-0	VT6-0	Qualification threshold % Qual % = 100% • VT/127 $38_{dec} \leq VT \leq 127_{dec}$

REGISTER DESCRIPTION (continued)

Group Delay Register		(Address = 001 1011 = 1Bh = 27d)			
Bits 7-0	GD7-0	Filter group delay Δ% setting Group Delay D% = 0.2362 • (GD - 128) • 1% $0_{dec} < GD \leq 255_{dec}$			
Window Data Threshold Register		(Address = 000 1010 = 0Ah = 10d)			
Bit7 (MSB)	X	Not used; don't care			
Bits 6-0	WDT6-0	Qualification threshold % in data mode Qual % = 100% • WDT/127 $38_{dec} \leq WDT \leq 127_{dec}$			
Window Servo Threshold Reg.		(Address = 001 0010 = 12h = 18d)			
Bit7 (MSB)	X	Not used; don't care			
Bits 6-0	WST6-0	Qualification threshold % in servo mode Qual % = 100% • WST/127 $38_{dec} \leq WST \leq 127_{dec}$			
Control A Register		(Address = 001 0101 = 15h = 21d)			
Bits 7-6	TMS1,TMS0	Multiplexed test point source select control			
(MSB)		MTP1	MTP2	MTP3	MTP4
		00 = VCOR	PDREF	SYREF	FTBG
		01 = VCOR	SET	RESET	SRD
		10 = RD	QP	QN	COUT
		11 = IFREF	MCTR	NCTR	FTBG
Bit 5	TP123E	MTP1, MTP2, MTP3 enable 1 = enabled; 0 = static '1'			
Bit 4	TP4E	MTP4 enable 1 = enabled; 0 = static '1'			
Bit 3	FDCT	AGC fast decay test mode 1 = fast decay current continuously on 0 = in normal operating mode			
Bit 2	BYPT	Bypass Time Base Generator Function 1 = Data synchronizer reference frequency is FREF 0 = Data Synchronizer reference is TBG output			
Bits 1-0	TPD1-0	Time Base Generator phase detector control 00 = in normal operating mode 01 = in pump down test mode 10 = in pump up test mode 11 = both pump up & down off			

REGISTER DESCRIPTION (continued)

Control B Register		(Address = 000 1100 = 0Ch = 12d)
Bit 7-5 (MSB)	X	Not used; don't care
Bits 4-3	DPD1-0	Data Synchronizer phase detector control 00 = in normal operating mode 01 = in pump down test mode 10 = in pump up test mode 11 = both pump up & down off
Bit 2	RDI	RDIO, SWPIN and SWNIN pins input/output control 1 = input to Data Synchronizer test mode 0 = output RDIO only.
Bit 1	GS	Data Synchronizer Phase Detector Gain Shift enable 1 = enabled; 0 = disabled
Bit 0	DW	Direct Write 1 = TBG bypassed 0 = TBG in use
M Counter Register		(Address = 000 1101 = 0Dh = 13d)
Bits 7-0	M7-0	M Counter value
N Counter Register		(Address = 000 0101 = 05h = 5d)
Bit 7	FOEN	Filter oscillator enable 1 = enabled; 0 = disabled
Bits6-0	N6-0	N Counter value FTBG = FREF • [(M+1) + (N+1)]
Data Rate Register		(Address = 000 0100 = 04h = 4d)
Bit 7	X	not used, don't care
Bits 6-0	DR6-0	VCOs' center frequency biasing FVCO = 2 • Raw Data Rate (= 0.746 • DR) + 6.8
Threshold Decay Register		(Address = 001 1010 = 1Ah = 26d)
Bits 7-4	TS3-0	Decay current control at LEVEL in servo mode
Bits 3-0	TD3-0	Decay current control at LEVEL in data mode Decay current = 0.13 • TD μA in data mode 0.065 • TS μA in servo mode
Position Error Register		(Address = 010 0010 = 22h = 34d)
Bit 7-6	X	Not used; don't care
Bits 5-0	PE5-0	Position Error threshold

REGISTER DESCRIPTION (continued)

Window Shift Register		(Address = 001 1100 = 1Ch = 28d)
Bit 7	PDREF	Phase Detector reference control 1 = from Window Qualifier 0 = from Viterbi Qualifier
Bit 6	DSREF	Data Synchronizer reference control 1 = from Window Qualifier 0 = from Viterbi Qualifier
Bit 5	X	Test Mode: Set to zero
Bit 4	WSD	Window shift direction 1 = late; 0 = early
Bits 3-0	$\overline{WS3}$ - $\overline{WS0}$	Window shift magnitude % VCO Period = 1% • (15 - $\overline{WS}$) example: 0100 = > 11% window shift 1111 = > no window shift
Write Precomp Register		(Address = 010 0100 = 24h = 36d)
Bits 7-5	TDAC2-0	Multiplexed DAC test point control 000 = CDAC - filter cutoff 001 = BDAC - filter boost 010 = GDAC - filter group delay 011 = VTH DAC - qual threshold voltage 100 = DR DAC - data rate (VCOs center bias) 101 = TDAC - qual threshold decay time constant 111 = WP DAC - write precomp
Bit 4	XWP	External write precompensation enable 1 = enabled; 0 = disabled
Bit 3	WPE	Internal write precompensation enable 1 = enabled; 0 = disabled
Bits 2-0	$\overline{WP2}$ - $\overline{WP0}$	Write precomp magnitude Magnitude = (7 - $\overline{WP}$) • 0.031 • T_{TBG} T_{TBG} = TBG output period example: 011 = > 0.124 • T_{TBG}
Gain Shift Register		(Address = 001 0100 = 14h = 20d)
Bits 7-5	SD2-0	Servo time constant control Time constant = 0.1 µs • (SDI + 1)
Bits 4-0	GS4-0	Data Synchronizer phase detector gear shift counter

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REG#	REGISTER NAME	ADDRESS A6						A0	R/W	DATA BIT MAP D7	D6	D5	D4	D3	D2	D1	D0
R2	POWER DOWN CONTROL	0	0	0	0	0	1	0	0	I/O SPEED BIT1	I/O SPEED BIT0	--	TBG 1=Disable 0=Enable	DATA SYNC 1=Disable 0=Enable	FILTER 1=Disable 0=Enable	SERVO DEMOD 1=Disable 0=Enable	PULSE DET 1=Disable 0=Enable
R3	DATA CUTOFF	0	0	0	0	0	1	1	0	DCBYP 1=Bypass 0=In Use	DC6	DC5	DC4	DC3	DC2	DC1	DC0
R4	DATA RATE	0	0	0	0	1	0	0	0	--	DR6	DR5	DR4	DR3	DR2	DR1	DR0
R5	N COUNTER	0	0	0	0	1	0	1	0	FOEN 1=Enable 0=Disable	N6	N5	N4	N3	N2	N1	N0
R10	WINDOW DATA THRESH.	0	0	0	1	0	1	0	0	--	WDT6	WDT5	WDT4	WDT3	WDT2	WDT1	WDT0
R11	FILTER BOOST	0	0	0	1	0	1	1	0	Servo Boost 1=Enable 0=Disable	FB6	FB5	FB4	FB3	FB2	FB1	FB0
R12	CONTROL B	0	0	0	1	1	0	0	0	--	--	--	DPD1	DPD0	RDI 1=Input 0=Output	GS 1=Enable 0=Disable	DW 1=Bypass 0=In Use
R13	M COUNTER	0	0	0	1	1	0	1	0	M7	M6	M5	M4	M3	M2	M1	M0
R18	WINDOW SERVO THRESH.	0	0	1	0	0	1	0	0	--	WST6	WST5	WST4	WST3	WST2	WST1	WST0
R19	SERVO CUTOFF	0	0	1	0	0	1	1	0	SCBYP 1=Bypass 0=In Use	SC6	SC5	SC4	SC3	SC2	SC1	SC0
R20	GAIN SHIFT	0	0	1	0	1	0	0	0	SD2	SD1	SD0	GS4	GS3	GS2	GS1	GS0
R21	CONTROL A	0	0	1	0	1	0	1	0	TMS1	TMS0	TP123E 1=Enable 0="Static 1"	TP4E 1=Enable 0="Static 1"	FDTC 1=Continuous 0=Normal	BYPT 1=FREF 0=TBG	TPD1	TPD0
R26	THRESHOLD DECAY	0	0	1	1	0	1	0	0	TS3	TS2	TS1	TS0	TD3	TD2	TD1	TD0
R27	GROUP DELAY	0	0	1	1	0	1	1	0	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0
R28	WINDOW SHIFT	0	0	1	1	1	0	0	0	PDREF 1=Window 0=Viterbi	DSREF 1=Window 0=Viterbi	TEST MODE	WSD 1=Late 0=Early	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
R34	POSITION ERROR	0	1	0	0	0	1	0	0	--	--	PE5	PE4	PE3	PE2	PE1	PE0
R36	WRITE PRECOMP	0	1	0	0	1	0	0	0	TDAC2	TDAC1	TDAC0	XWP 1=Enable 0=Disable	WPE 1=Enable 0=Disable	$\overline{WP2}$	$\overline{WP1}$	$\overline{WP0}$
R42	VITERBI THRESHOLD	0	1	0	1	0	1	0	0	--	VT6	VT5	VT4	VT3	VT2	VT1	VT0

FIGURE 15: Serial Port Register Mapping

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data Synchronizer PLL analog circuit supply
VPB	-	Time Base Generator PLL analog circuit supply
VPC	-	Internal ECL, CMOS logic digital supply
VPD	-	I/O Buffer (non-TTL or PECL) digital supply
VPG	-	Pulse Detector/Servo Demodulator/Filter analog circuit supply
DVRVCC	-	CMOS output buffer supply
VNA	-	Data Synchronizer PLL analog circuit ground
VNB	-	Time Base Generator PLL analog circuit ground
VNC	-	Internal ECL, CMOS logic digital ground
VND	-	I/O Buffer (non-TTL) digital ground
VNG	-	Pulse Detector/Servo Demodulator/Filter analog circuit ground
DVRGND1	-	CMOS output buffer ground
DVRGND2	-	CMOS output buffer ground

ANALOG INPUT PINS

AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator
FREF	I	REFERENCE FREQUENCY INPUT: Reference frequency for the time base generator. Pin FREF has an internal bias circuit which sets its DC input level at 1.4V nominal. In the test mode that the time base generator function is bypassed (BYPT = 1), the FREF frequency required is at 3 times the data rate. FREF may be driven either by a direct coupled 1 Vp-p signal or by an ac coupled ECL signal.

PIN DESCRIPTIONS (continued)

ANALOG OUTPUT PINS

NAME	TYPE	DESCRIPTION
FNP, FNN	O	FILTER NORMAL OUTPUTS: With BYPF = 0 in the appropriate Cutoff Register, these are the filter normal low pass output. They should be AC coupled to the data comparator in the pulse qualifier. With BYPF = 1, these are the AGC amplifier output.
FDP, FDN	O	FILTER DIFFERENTIATED OUTPUTS: These are the filter time differentiated low pass output. They should be AC coupled, for low DC offset, to the clock comparator in the pulse qualifier.
RP	O	PULSE DETECTOR REFERENCE: Precision current reference for the Pulse Detector. Connect a 47 kΩ resistor from RP to Analog GND.
A-B	O	SERVO DIFFERENCE A-B: This voltage, which has a baseline of SREF, provides the difference between the captured "A" Burst and "B" Burst.
C-D	O	SERVO DIFFERENCE C-D: This voltage, which has a baseline of SREF, provides the difference between the captured "C" Burst and "D" Burst.
SREF	O	SERVO REFERENCE: A regulated 2.5V bandgap voltage
LEVEL	O	Buffered output of the peak-to-peak averaging circuit. This pin provides the reference voltage to the threshold setting DAC. The pin may be driven by an external voltage. Its nominal output resistance is 5 kΩ.
DACOUT	O	DAC OUTPUT: Test point output for the internal DACs. The TDAC2-0 bits in the Write Precomp Register select the signal source for DACOUT. When not in use, the preferred setting is to select CDAC.

ANALOG CONTROL PINS

BYPD	O	The data AGC integrating capacitor, CBYPD, is connected between BYPD and VCC. This pin is used when in data read mode ($\overline{SG}$ = 1).
BYPS	O	The servo AGC integrating capacitor CBYPS, is connected between BYPS and VCC. This pin is used when in servo read mode ($\overline{SG}$ = 0).
TFLP, TFLN	-	PLL LOOP FILTER: Differential connection points for the time base generator PLL loop filter components. The common mode voltage at these pins should be 2V.
DFLP,DFLN	-	PLL LOOP FILTER: Differential connection points for the data synchronizer PLL loop filter components. The common mode voltage at these pins should be 2V.
RR	I	REFERENCE RESISTOR INPUT: An external 1% 49.9 kΩ resistor is connected from this pin to VNA to establish a precise internal reference current for the data synchronizer and the time base generator. A nominal 1.5V should appear on this pin.
RX	I	REFERENCE RESISTOR INPUT: An external 1% 12.1 kΩ resistor is connected from this pin to VNG to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

DIGITAL INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{\text{PWRON}}$	I	POWER CONTROL: CMOS compatible power control pin. When set to logic high, the entire chip is in sleep mode with all circuitry, except serial port, shut down. This pin should be set to logic low in normal operating mode. Selected circuitry can be shut down by the Power Down Register.
$\overline{\text{HOLD}}$	I	HOLD CONTROL INPUT: CMOS compatible control pin which, when pulled low, holds the input AGC amplifier gain constant. The AGC loop is active when this pin is high.
A0, A1	I	BURST ADDRESS BITS: Two CMOS compatible inputs when decoded select peak detectors A, B, C, or D.
STROBE	I	PEAK DETECTOR CONTROL INPUT: CMOS compatible input which turns the selected peak detector on when driven high. When this input is low, the peak detector is in the Hold mode.
$\overline{\text{RESET}}$	I	RESET CONTROL INPUT: CMOS compatible input that will discharge the internal servo burst hold capacitors on Channels A through D when set to a logic low.
RG	I	READ GATE: CMOS compatible input that, when pulled high, selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the RD input ($\overline{\text{DRD}}$) and enables the read mode/address detect sequences. A low level selects the time base generator output. It is overridden when $\overline{\text{SG}}$ is low.
WDI	I	WRITE DATA: CMOS compatible input to the precomp when WG is pulled high
WG	I	WRITE GATE: CMOS compatible input that, when pulled high, enables the write mode
$\overline{\text{SG}}$	I	SERVO GATE: CMOS compatible input that, when pulled low, enables the servo read mode.
SWPIN	I	POSITIVE VITERBI READ PULSE: This pin allows positive peaks to be input to the survival shift register for test purposes only. A pulse is clocked into the register on the falling edges of this CMOS compatible signal when the RDI bit is set high in the serial port.
SWNIN	I	NEGATIVE VITERBI READ PULSE: This pin allows negative peaks to be input to the survival shift register for test purposes only. A pulse is clocked into the register on the falling edges of this CMOS compatible signal when the RDI bit is set high in the serial port.
EARLY	I	EARLY WRITE PRECOMPENSATION: CMOS compatible write precompensation input to shift write data pulse early.
LATE	I	LATE WRITE PRECOMPENSATION: CMOS compatible write precompensation input to shift write data pulse late.

PIN DESCRIPTIONS (continued)

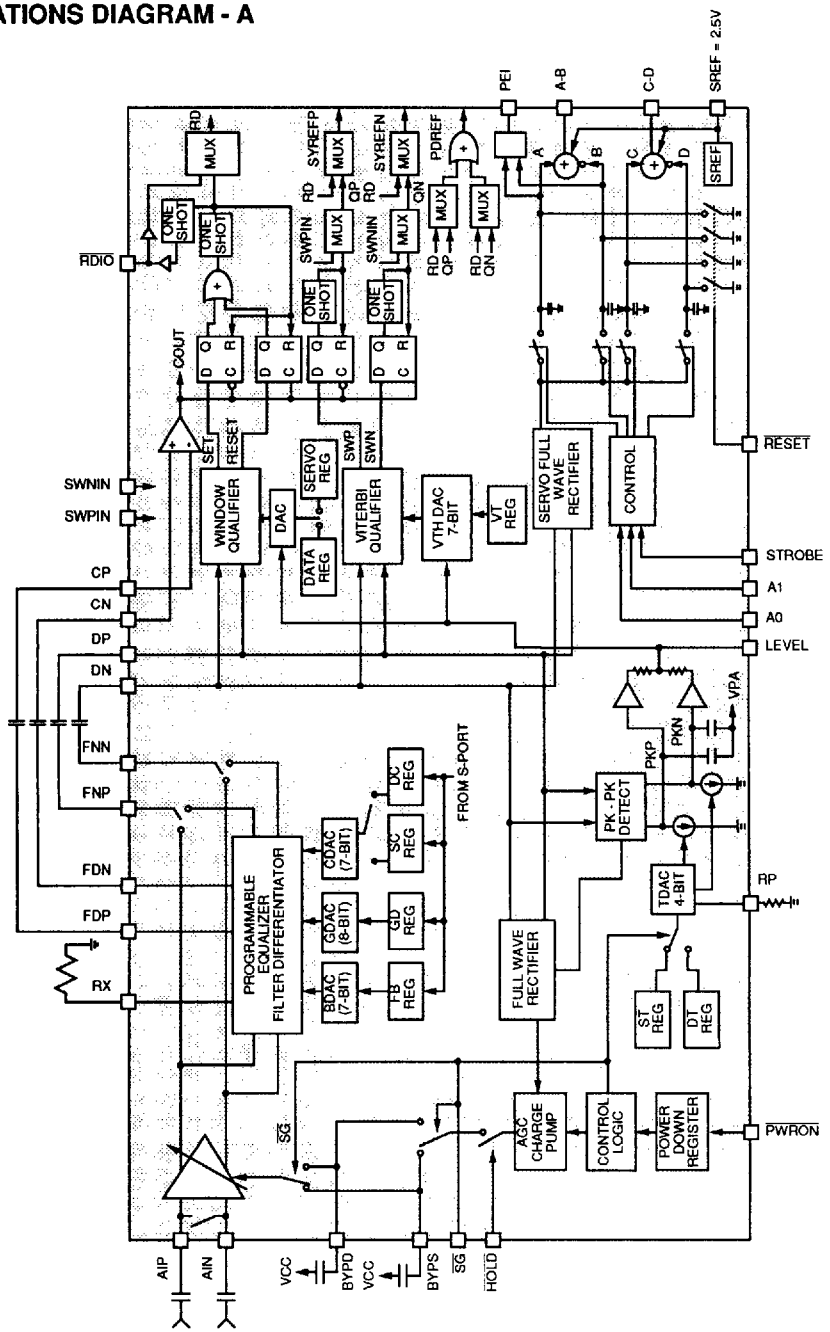
DIGITAL OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RDIO}$	O	READ DATA I/O: Bi-directional CMOS pin. When the RDI bit in the Control B Register is '0', the $\overline{RDIO}$ pin is a low impedance output pin. A active low pulse is present when a valid peak is detected either in the servo mode or when both RG and WG are '0'. With either RG or WG being '1', the $\overline{RDIO}$ output is held at '1'. If the RDI bit is '1', the $\overline{RDIO}$ is an input to the data synchronizer in a test mode.
RRC	O	READ REFERENCE CLOCK: A multiplexed clock source used by the controller. When RG is low, RRC is synchronized to the time base generator output, F_{TBG}, divided by 2. When RG goes high, RRC remains synchronized to $F_{TBG} \div 2$ until the bit sync is completed. At that time, RRC is synchronized to the data synchronizer $F_{VCO} \div 2$. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. CMOS output levels.
$\overline{WDO}$	O	WRITE DATA OUTPUT: CMOS write data output. The data is synchronized to the reference clock F_{TBG}, unless in Direct Write or external precomp mode. In Direct Write mode, WDO is simply a buffered WDI. Write precomp moves the falling edge of $\overline{WDO}$.
MTP1,MTP2, MTP3,MTP4	O	MULTIPLEXED TEST POINT OUTPUT: An open emitter pseudo-ECL output test point. The test point signal source is controlled by the Control A Register. External resistors (261Ω pullup to VPD and 402Ω pulldown to VND) are needed to monitor the test points. These resistors should be removed in normal operation for low power dissipation.
SDO	O	SERIAL DATA OUTPUT: This CMOS output produces raw data from the survival register of the data synchronizer.
PEI	O	POSITION ERROR INDICATOR: CMOS output which switches high when the amplitude difference between Servo Burst A and Servo Burst B exceeds a preset value set in the Position Error register of the serial port.

SERIAL PORT PINS

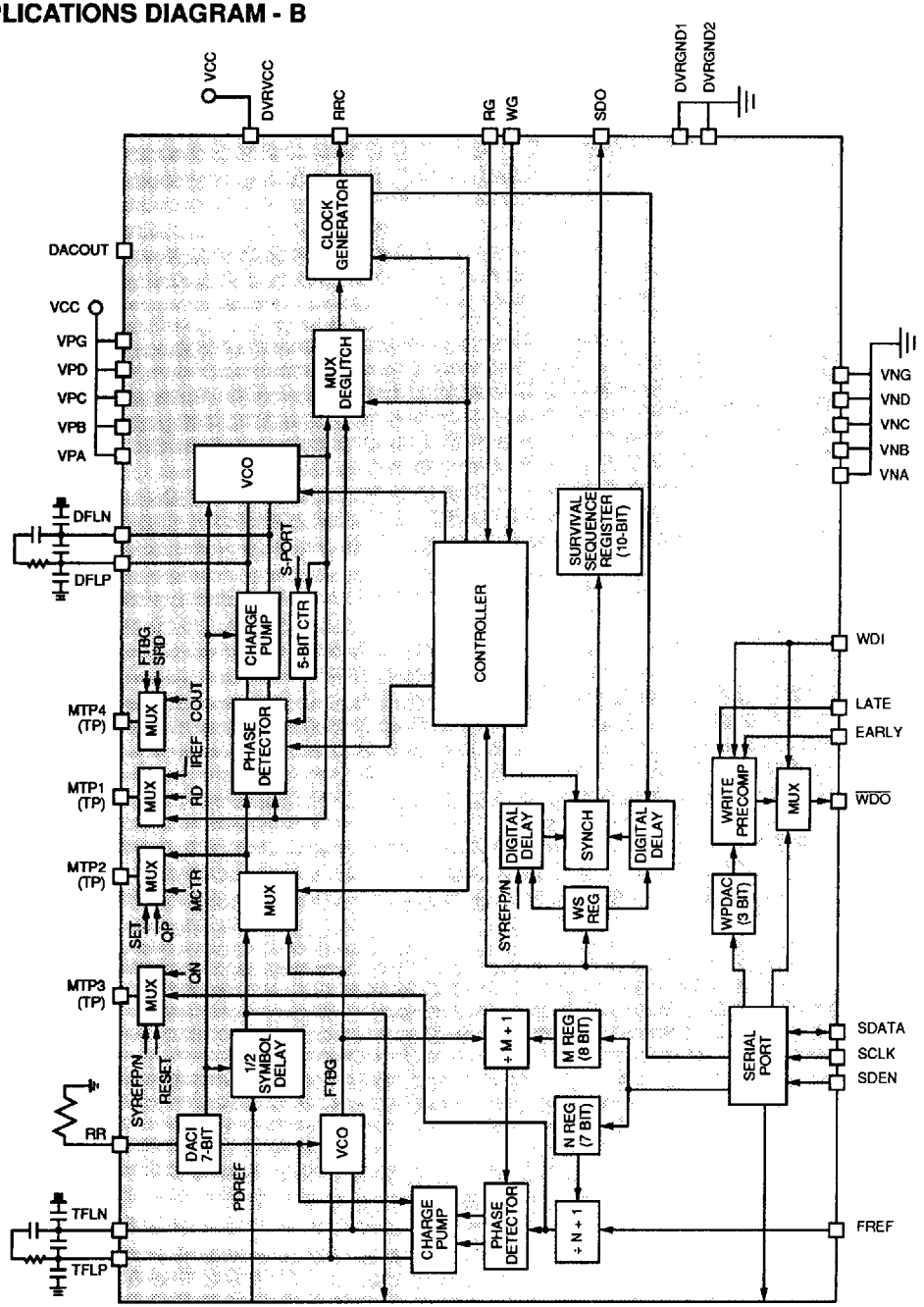
SCLK	I	SERIAL DATA CLOCK: Positive edge triggered clock input for the serial data. CMOS input level.
SDATA	I/O	SERIAL DATA: Input/output pin for serial data; 8 instruction/address bits first followed by 8 data bits. CMOS input/output levels.
SDEN	I	SERIAL DATA ENABLE: Active high input pin for enable the serial port. CMOS input levels.

APPLICATIONS DIAGRAM - A



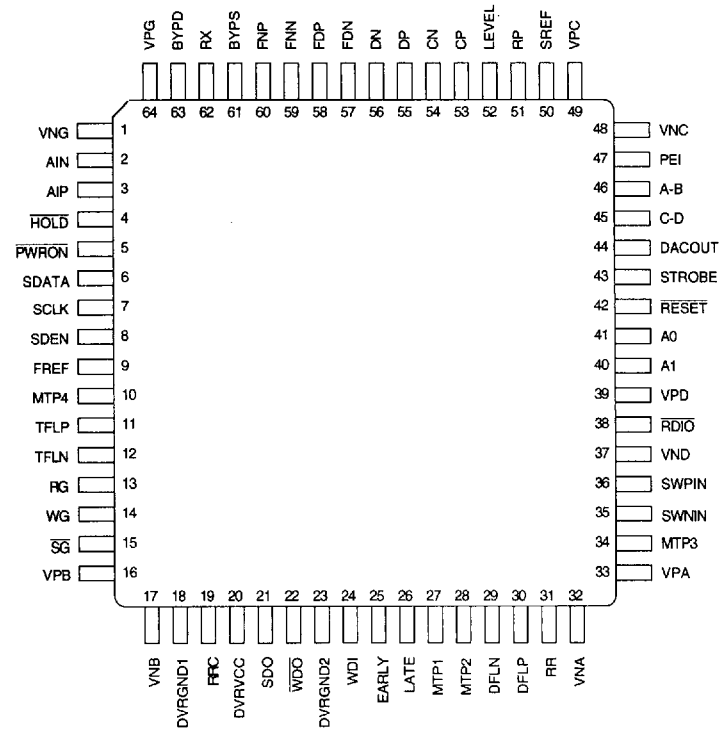
SSI 34P3400
45 Mbit/s Read Channel
w/Adaptive Threshold Qualifier

APPLICATIONS DIAGRAM - B



PACKAGE PIN DESIGNATIONS

(Top View)



64-Lead TQFP

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CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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