

Description

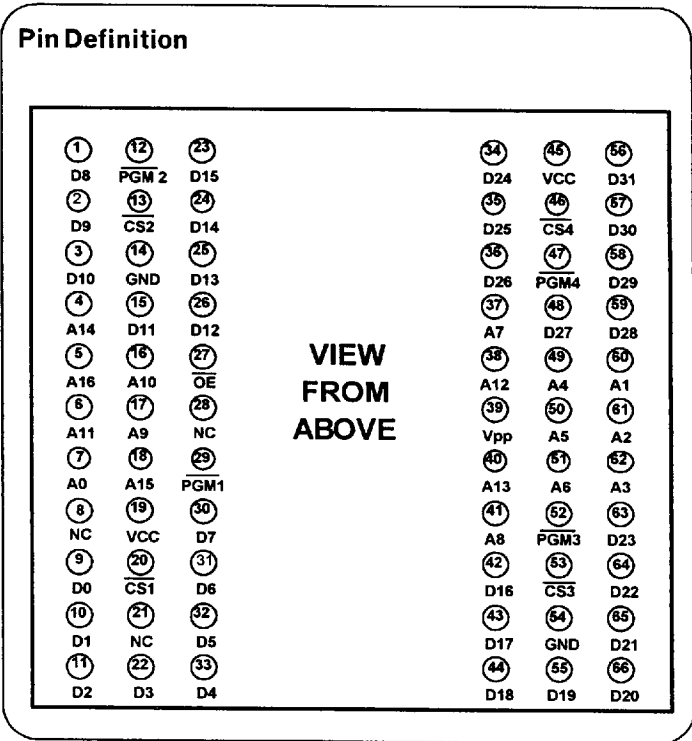
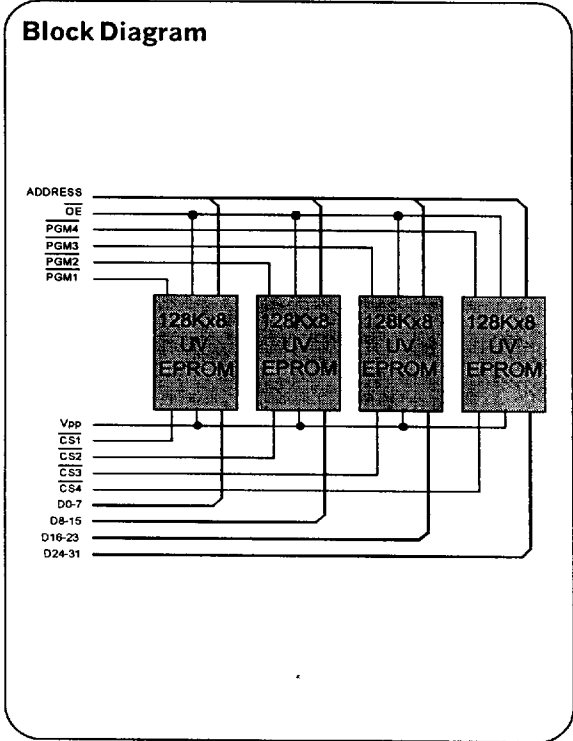
The PUMA2U4000 is a 4 Mbit CMOS High Speed UV EPROM in a 66 pin PGA package with access times of 120ns and 150ns. The output width is user configurable as 8, 16 or 32 bits wide. It has a low power standby mode of 2.2 mW(max) and complete device programming can be completed in 14 seconds. The package has on-board decoupling capacitors and is suitable for thermal ladder applications.

May be screened in accordance with MIL-STD-883.

4,194,304 bit CMOS UV EPROM

Features

- Fast Access times of 120/150 ns
- Pin grid array gives 2:1 improvement over DIL.
- Package Suitable for Thermal Ladder Applications.
- On board decoupling capacitors.
- Configurable as 8 / 16 / 32 bit wide.
- Operating Power 182 / 341 / 660 mW(max)
- Standby Power 2.2 mW(max)
- V_{pp} Voltage of 12.5±0.3V.
- Complete Device Programming in 14 seconds(typ)
- May be screened in accordance with MIL-STD-883.



Pin Functions

A0 - A16	Address Inputs	D0 - D31	Data Inputs/Outputs
CS1-4	Chip Select	OE	Output Enable
PGM1-4	Program Enable	NC	No Connect
V_{pp}	Programming Voltage	V_{cc}	Power(+5V)
GND	Ground		

DC OPERATING CHARACTERISTICS**Absolute Maximum Ratings** ⁽¹⁾

Voltage on pins V_{PP} and A_9 ⁽²⁾	V_{TPP}	-0.6V to +13.5	V
Voltage on pin V_{CC}	V_{TCC}	-0.6V to + 7.0	V
Voltage on any other pins ⁽²⁾	V_T	-0.6V to + 7.0	V
Power Dissipation	P_T	2	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width - 1.0V for less than 50 ns.

Recommended Operating Conditions

Parameter		min	typ	max	
Supply Voltage	V_{CC}	4.75	5.0	6.25	V
DC Program Voltage	V_{PP}	12.2	12.5	12.8	V
Input High Voltage	V_{IH}	2.2	-	$V_{CC}+1$ ⁽²⁾	V
Input Low Voltage	V_{IL}	-0.3 ⁽¹⁾	-	0.8	V
Operating Temperature	T_A	0	-	70	°C(2U4000)
	T_{AI}	-40	-	85	°C(2U4000I)
	T_{AM}	-55	-	125	°C(2U4000M, MB)

Notes (1) Pulse width - 1.0V for less than 50 ns.

(2) $V_{CC}+1.5V$ for pulse width - 20 ns. If V_{IH} is over the specified max. value, Read operation cannot be guaranteed.

Capacitance ($V_{CC}=5V\pm 5\%$, $T_A=25^\circ C$)

Parameter		Symbol	Test Condition	typ	max	Unit
Input Capacitance	Address, \overline{OE}	C_{IN1}	$V_{IN}=0V$	-	40	pF
	PGM1-4, $\overline{CS1}$ -4	C_{IN2}	$V_{IN}=0V$	-	10	pF
I/O Capacitance	32 Bit Mode	$C_{I/O}$	$V_{I/O}=0V$	-	15	pF

Note: These parameters are calculated and not measured.

Read Operation ($T_A = -55$ to $+125^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Test Condition	min	typ ⁽²⁾	max	Unit
Input Leakage Current	Address, $\overline{\text{OE}}$	I_{L11} $V_{IN} = 0\text{V}$ to V_{CC}	-	-	20	μA
	Other Pins	I_{L11} $V_{IN} = 0\text{V}$ to V_{CC}	-	-	20	μA
Output Leakage Current	32 bit	I_{OUT} $V_{OUT} = 5.25\text{V}$	-	-	40	μA
V_{PP} Leakage Current		I_{PP} $V_{PP} = 5\text{V}$	-	4	80	μA
Operating Supply Current	32 bit	I_{CC} $\overline{\text{CS}}^{(1)} = V_{IL}$, $I_{OUT} = 0\text{mA}$	-	-	200	mA
Average Supply Current	32 bit	I_{CC32} $f = 10\text{MHz}$, $I_{OUT} = 0\text{mA}$	-	-	200	mA
	16 bit	I_{CC16} As Above	-	-	102	mA
	8 bit	I_{CC8} As Above	-	-	53	mA
Standby Supply Current	TTL	I_{SB} $\overline{\text{CS}}^{(1)} = V_{IH}$, $I_{OUT} = 0\text{mA}$	-	-	5	mA
	CMOS	I_{SB1} $\overline{\text{CS}}^{(1)} = V_{CC} - 0.3\text{V}$, $0.2\text{V} < V_{IN} < V_{CC} - 0.2\text{V}$	-	4	400	μA
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V

Notes (1) $\overline{\text{CS}}$ above are accessed through CS1-4. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) Typical figures measured at 25°C .

(3) **CAUTION:** the PUMA 2U4000 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

Programming Operation ($T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6.0\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.5\text{V} \pm 0.3\text{V}$)

The following information is provided for design purposes only.

Parameter	Symbol	Test Condition	min	typ ⁽²⁾	max	Unit
V_{CC} Program Supply Current	32 bit	I_{CCP32} Programming in operation	-	-	120	mA
	16 bit	I_{CCP32} As Above	-	-	60	mA
	8 bit	I_{CCP32} As Above	-	-	30	mA
V_{PP} Program Supply Current	32 bit	I_{PPB32} Single Byte Programming	-	-	160	mA
	16 bit	I_{PPB16} As Above	-	-	80	mA
	8 bit	I_{PPB8} As Above	-	-	40	mA
	32 bit	I_{PPP32} Page Mode Programming	-	-	200	mA
	16 bit	I_{PPP16} As Above	-	-	100	mA
	8 bit	I_{PPP8} As Above	-	-	50	mA
Identifier Select Voltage	V_H		11.5	12.0	12.5	V
Programming Voltage	V_{PP}		12.2	12.5	12.8	V
Supply Voltage	V_{CCP}		5.75	6.0	6.25	V
Output Low Voltage during verify	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	-	0.45	V
Output High Voltage during verify	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V

Notes (1) $\overline{\text{CS}}$ above are accessed through CS1-4. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) V_{CC} must be applied before V_{PP} and removed after V_{PP} .

(3) V_{PP} must not exceed 13.5V including overshoot.

(4) The transitions V_{IL} to 12.5V or 12.5V to V_{IL} are not allowed while $\overline{\text{CS}} = \text{Low}$.

(5) When programming the PUMA 2U4000, a $0.1\mu\text{F}$ capacitor is required across V_{PP} and GND to suppress noise transients which may damage the device.

(6) **CAUTION:** The PUMA 2U4000 must not be removed from or inserted into a socket while V_{PP} or V_{CC} are applied.

Operating Modes

This table shows the inputs required to control the operating modes of the EPROMs on the PUMA 2U4000.

Mode		\overline{CS}	\overline{OE}	\overline{PGM}	A0	A9	Vpp	Vcc	Outputs
Read		0	0	1	X	X	5V	5V	Data out
Output Disable		0	1	1	X	X	5V	5V	Floating
Standby		1	X	X	X	X	5V	5V	Floating
Program		0	1	0	X	X	12.5V	6V	Data in
Program Verify		0	0	1	X	X	12.5V	6V	Data out
Page Data Latch		1	0	1	X	X	12.5V	6V	Data in
Page Program		1	1	0	X	X	12.5V	6V	Floating
Program Inhibit		0	0	0	X	X	12.5V	6V	Floating
		0	1	1	X	X	12.5V	6V	
		1	0	0	X	X	12.5V	6V	
		1	1	1	X	X	12.5V	6V	
Identifier (NOTE 1)	Manufacturer	0	0	1	0	12V	X	5/6V	07 _{HEX}
	Device Code	0	0	1	1	12V	X	5/6V	38 _{HEX}

1 = V_{IH}0 = V_{IL}

X = Don't Care

Notes (1) A1 - A8 = A10 - A16 = V_{IL}

(2) \overline{CS} is accessed through $\overline{CS1-4}$, and \overline{PGM} is accessed through $\overline{PGM1-4}$. For correct operation, $\overline{CS1-4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation. $\overline{PGM1-4}$ must also be operated in the same manner.

AC Test Conditions

*Input pulse levels: GND to 3.0V

*Input rise and fall times: 5 ns

*Input and Output timing reference levels: 1.5V

*Output load: 1 TTL gate + 100pF

*V_{cc} = 5V ± 10%

*Module is tested in 32 bit mode.

Read Operation

Parameter	Symbol	-12		-15		Unit
		min	max	min	max	
Address to Output Delay	t_{ACC}	-	120	-	150	ns
Chip Select to Output Delay	t_{CS}	-	120	-	150	ns
Output Enable to Output Delay	t_{OE}	-	60	-	70	ns
OE or CS High to Output Float ⁽¹⁾	t_{DF}	0	50	0	60	ns
Output Hold from Address, CS or OE	t_{OH}	0	-	0	-	ns

Notes (1) t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.

Programming Operation

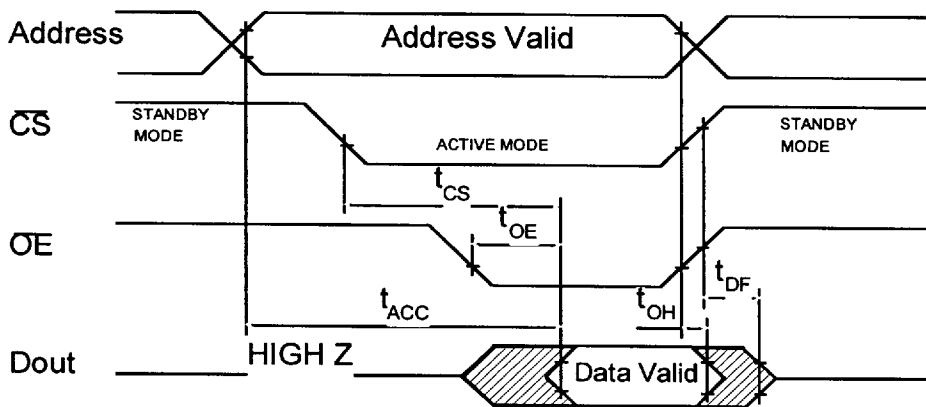
Parameter	Symbol	min	typ	max	Unit
Address Setup Time	t_{AS}	2	-	-	μ s
Output Enable Setup Time	t_{OES}	2	-	-	μ s
Output Enable Hold Time	t_{OEHL}	2	-	-	μ s
Data Setup Time	t_{DS}	2	-	-	μ s
Address Hold Time	t_{AH}	0	-	-	μ s
	t_{AHL}	2	-	-	μ s
Data Hold Time	t_{DH}	2	-	-	μ s
Output Enable High to Output Float Delay ⁽¹⁾	t_{DF}	0	-	130	ns
V_{PP} Setup Time	t_{VPS}	2	-	-	μ s
V_{CC} Setup Time	t_{VCS}	2	-	-	μ s
Program Initial Program Pulse Width ⁽²⁾	t_{PW}	0.19	0.2	0.21	ms
Program Overprogram Pulse Width ⁽³⁾	t_{OPW}	0.19	-	5.25	ms
Data Valid from Output Enable	t_{OE}	0	-	150	ns
Program Setup Time	t_{PGMS}	2	-	-	μ s
Chip Select Setup Time	t_{CES}	2	-	-	μ s
Chip Select Hold Time	t_{CSH}	2	-	-	μ s
Output Enable Pulse Width during Data Latch	t_{LW}	1	-	-	μ s

Notes (1) Defines the time at which the output achieves the open circuit condition and is no longer driven.

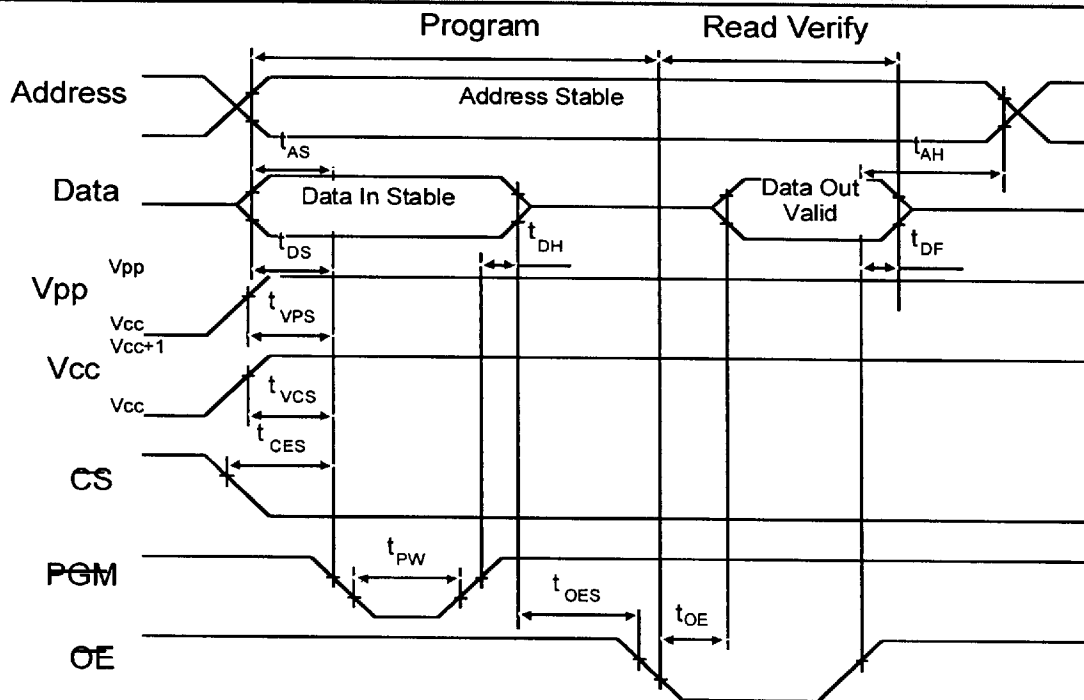
(2) Initial program pulse width tolerance is $0.2\text{ ms} \pm 5\%$.

(3) Length of this pulse may vary as a function of the iteration counter value n.

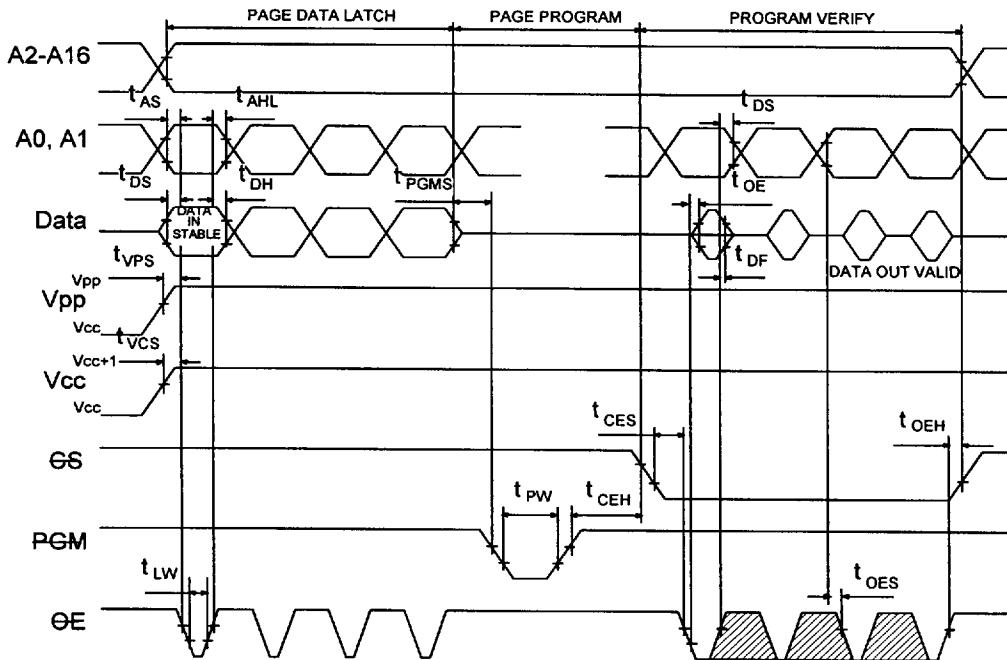
Read Cycle Timing Waveform



Single Byte Programming Timing Waveform



Page Mode Programming Timming Waveform



DEVICE OPERATION

High Performance Programming Algorithm

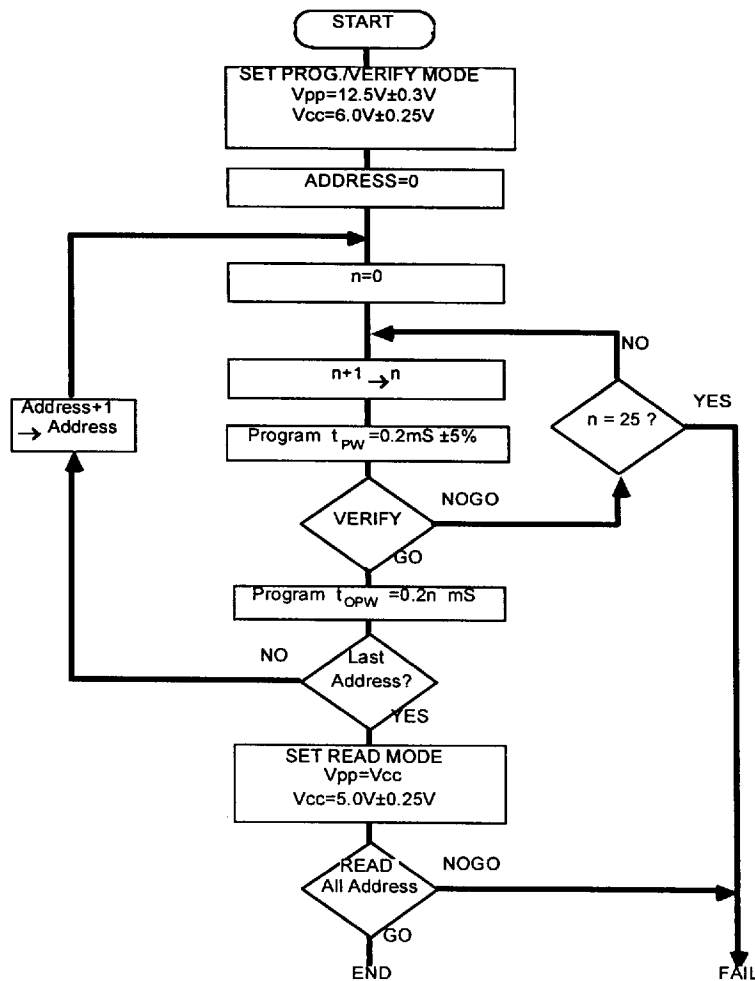
The PUMA 2U4000 can be programmed using either of the algorithms shown below. These allow faster programming times without stressing the device or causing deterioration in Data Retention Time. Two methods are described here, Single Byte and Page Mode; see the Truth Table on page 4 for selection of these modes.

Although each flow chart specifically refers to a single EPROM, all four devices on the PUMA can be programmed simultaneously in 32 bit mode, in pairs in 16 bit mode or singly in 8 bit mode.

Note that the parts used on this module are Hitachi 27C101A; this information, together with the device identifier code, should allow the correct programming algorithm to be selected automatically.

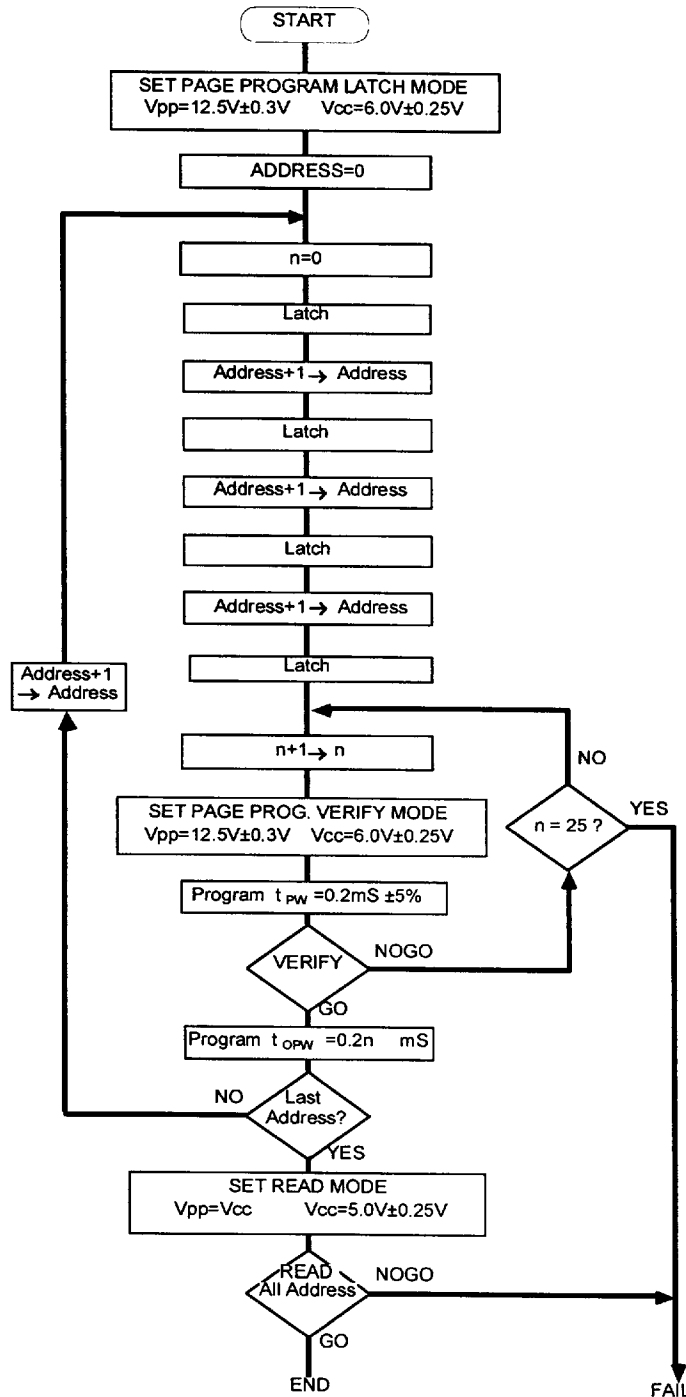
Single Byte

When the Program logic conditions are satisfied, the location is designated by A0 - A16, and the data to be programmed is applied 8 bits in parallel on D0 - D7. In this state, Byte programming is completed when PGM is at a low level.



Page Mode

Page Mode allows up to 16 bytes of data to be simultaneously programmed. The destination address for a Page Programming operation must reside on the same page i.e. A2 - A16 must not change. When the logic conditions in the Truth Table are satisfied, Page Mode Programming is activated. The four locations in the same page are designated by A0 - A1, and the data is applied in parallel on D0 - D7. In this state the data latch (4 bytes) is completed, and the data is programmed when OE is high. Programming is completed when PGM is low.



Programming Notes

Upon delivery, or after each erasure, the MUM8128W has all 1,048,576 bits in the ONE or HIGH state. ZEROs are loaded into the devices through the procedure of programming.

This mode is entered when 12.5V is applied to the V_{PP} pin, V_{CC} is raised to 6.0V, \overline{CS} and \overline{PGM} are at V_{IL} and \overline{OE} is at V_{IH} , as shown on the Table on page 2. Data may be applied in 8, 16 or 32 bits in parallel depending on how CS1-4 and PGM1-4 are controlled.

The algorithms reduce programming time by using 200 μ s pulses followed by byte verification to determine if the byte has been successfully programmed. If the data does not verify, up to 25 such pulses (n) can be applied, after which, if verification fails, programming stops. This process is repeated for each memory location within the PUMA 2U4000. After successful programming each memory location is given an overprogram pulse of n times 0.2 ms duration to ensure that all bits have an adequate margin.

The algorithms program at $V_{CC}=6.0V$ in order to ensure that each EPROM bit is programmed to a sufficiently high threshold voltage. After programming is complete, all bytes are compared with the original data with $V_{CC}=5.0V\pm 5\%$.

In order to overcome the voltage drop caused by the inductive effects of the printed circuit board on which the PUMA 2U4000 module is used, it is recommended that a 4.7 μ F electrolytic capacitor is used between V_{CC} and GND for every two PUMA modules. This capacitor should be placed close to the point where the power supply is routed to the UV EPROM array.

Device Identifier Mode

The device identifier mode allows the reading out of a binary code from an EPROM which identify its manufacturer and specific type. It is intended to be used to automatically match the device to be programmed with the correct algorithm. This mode operates over the 25°C \pm 5°C temperature range.

In order to activate this mode 12.0V \pm 0.5V must be placed onto address line A9, after which two identifier bytes may be read by toggling A0 from V_{IL} to V_{IH} . All other address lines are held at V_{IL} during this sequence.

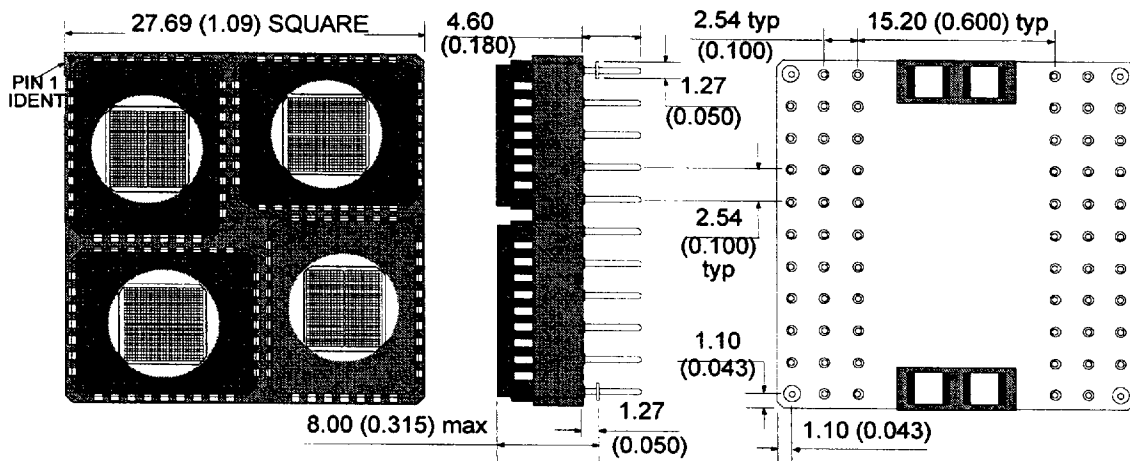
The manufacturer code is accessed with A0= V_{IL} and the device code with A0= V_{IH} ; the values for these codes are given in the Operating Mode Table on page 2. Note that all identifiers for manufacturer and device codes will possess odd parity, with D7 defined as the parity bit.

Erase

Complete erasure of the PUMA 2U4000 is performed by exposure to an ultraviolet light source giving a dosage of 15WS/cm². This dosage can be obtained by using an ultraviolet lamp with a wavelength of 2537 Å at a minimum intensity of 12,000 μ W/cm², for approximately 15 - 20 minutes. The MUM8128W should be directly under and about 1 inch from the light source.

Note that sunlight and fluorescent light may contain sufficient ultraviolet light to erase the programmed information. Although erasure times will be much longer at these levels, the transparent lids on this module should be covered with an opaque label to realise maximum system reliability.

Package Details Dimensions in mm (inches).



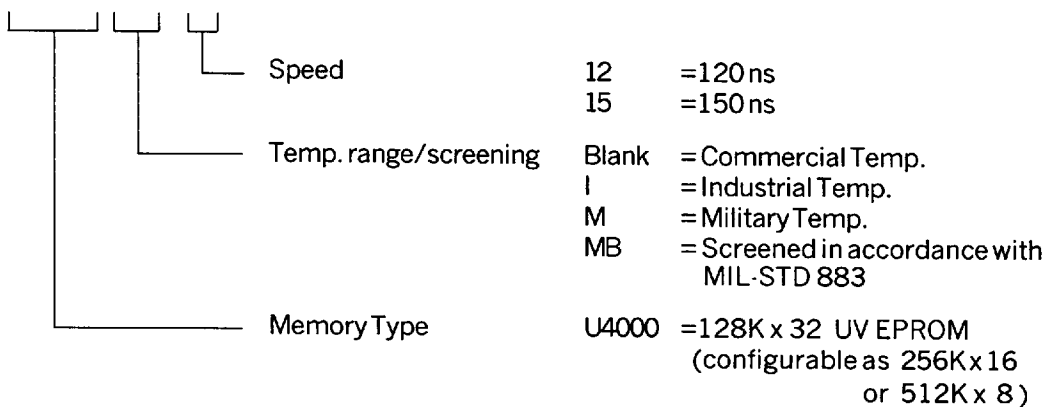
Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883 method 5004 Level B.

MB MODULE SCREENING FLOW		
SCREEN	TEST METHOD	LEVEL
Visual and Mechanical External visual Temperature cycle	2017 Condition B (or manufacturers equivalent) 1010 Condition C (10 Cycles, -65°C to +150°C)	100% 100%
Burn-In Pre Burn-in Electrical Burn-In	Per Applicable device Specifications at T _A = +25°C (optional) Method 1015, Condition D, T _A = +125°C	100% 100%
Final Electrical Tests Static (dc) Functional Switching (ac)	Per applicable Device Specification a) @ T _A = +25°C and power supply extremes b) @ temperature and power supply extremes a) @ T _A = +25°C and power supply extremes b) @ temperature and power supply extremes a) @ T _A = +25°C and power supply extremes b) @ temperature and power supply extremes	100% 100% 100% 100% 100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T _A = +25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per HMP or customer specification	

Ordering Information

PUMA 2U4000MB-12



■ 6353379 0002515 668 ■ 10