SIEMENS

ICs for Communications

Two/Four Channel Codec Filter for Terminal Applications SICOFI®-2/4-TE

PSB 2132 Version 1.4
PSB 2134 Version 1.4

Delta Sheet 1998-04-01

PSB 2132 **PSB 2134** **Revision History:**		**Current Version: 1998-04-01**
Previous Version:		None
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
		Abstract of Changes With the redesign of the SICOFI-2/4-TE all known erratas of version V1.2 were corrected according to the data sheet 09.97. **Effect of Changes** See detailed describtion as follows.

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Two/Four Channel Codec Filter for Terminal Applications SICOFI®-2/4-TE

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Delta Sheet for the Version 1.4

1 Interrupt Handling

If all the inputs assigned to channel-pair-1,2 (or 3,4) have been stable for two samples (i.e. for at least the debounce time), an interrupt on INT12 (or INT34) is generated. The status information will be read into the XR-registers with the rising edge of INT12 (or INT34). The status information of the assigned channel-pair-1,2 (or 3,4) will be updated after the next interrupt INT12 (or INT34) has occurred. The interrupt INT12 (or INT34) of assigned channel-pair-1,2 (or 3,4) is cleared, if the registers XR0-XR3 are read via a XOP command.

- The signaling inputs (SIx_x and SBx_x, if programmed as inputs) are sampled after the debounce time (refer to XR4)
- INT12 is assigned to and affected by the signaling inputs of channel-pair-1,2
- INT34 is assigned to and affected by the signaling inputs of channel-pair-3,4

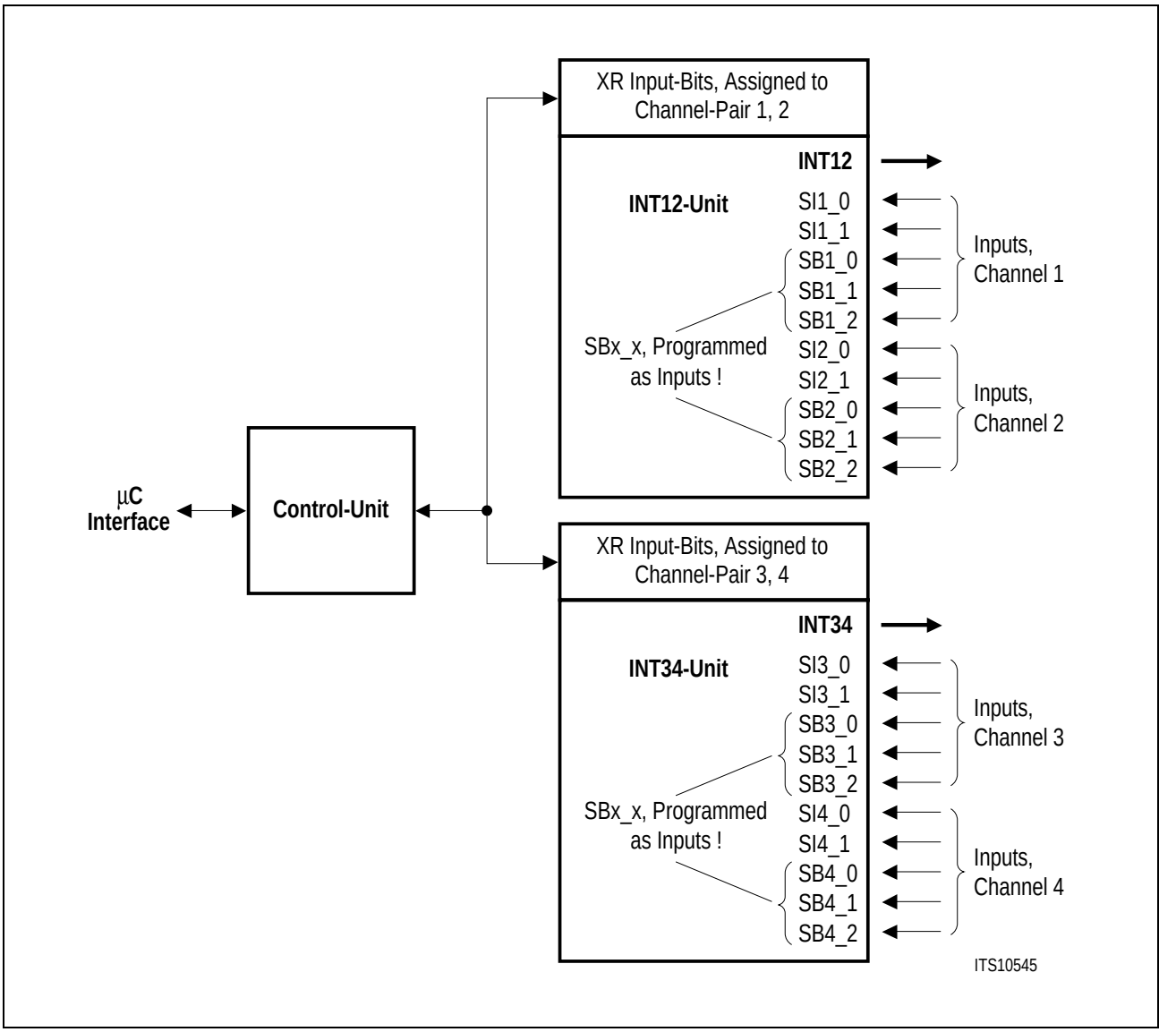

Figure 1

Example for Channel-pair-1,2

If one or more of the signaling input pins for channel-pair-1,2 (input pins and bi-directional pins programmed as inputs) change, and all these signaling inputs for channel-pair-1,2 are stable for at least the debounce time specified in Register XR4 INT12 will go from ‘0’ to ‘1’.

The assigned interrupt INT12 is cleared if the appropriate registers (XR0, XR1, XR2 and XR3, read with command XOP := $3B_H$) are read via the serial µC-interface.

Note: Pin INT34 provides the same functionality for channel-pair-3,4. Changes at the signaling inputs assigned to channel-pair-3,4 do not affect INT12 and vice versa!

The following example shows the interrupt functionality of channel-pair-1,2, SBx_x are programmed as outputs:

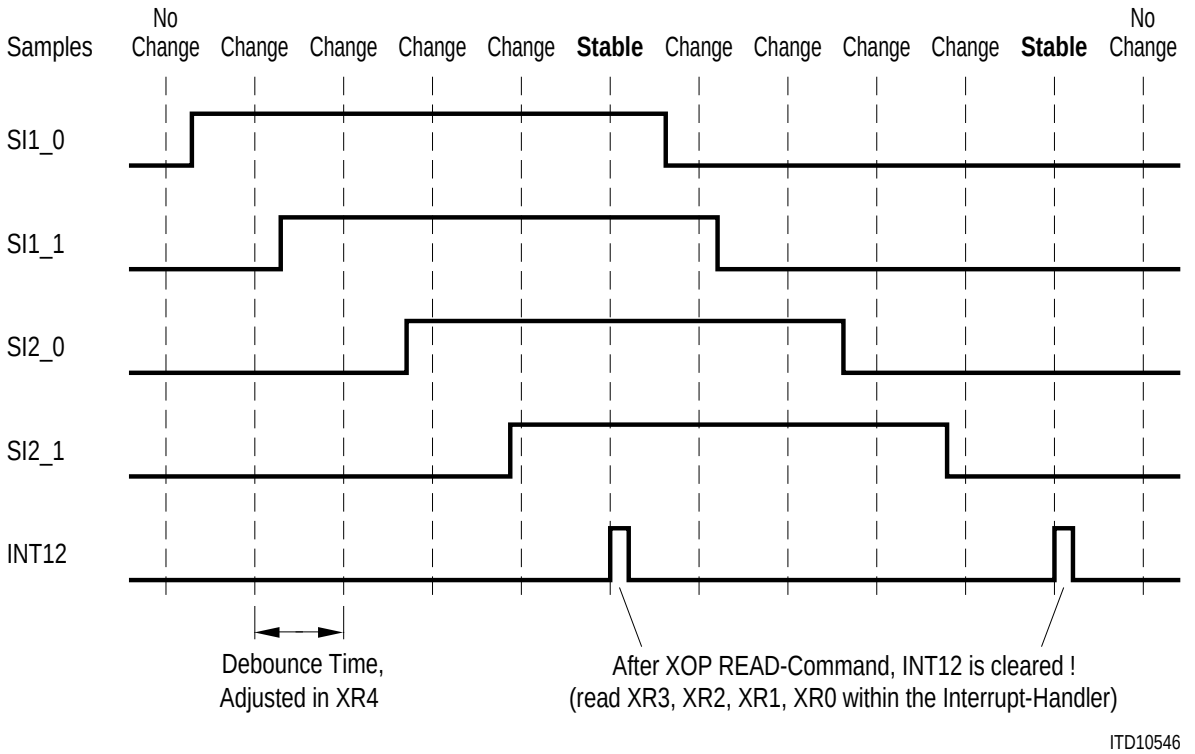

Figure 2

Example, Status Information in XR-Registers for Both Channel-pairs 1,2 and 3,4

The status information of the appropriate channel-pair-1,2 (or 3,4) will be read into the XR-registers with the rising edge of INT12 (or INT34) and remains valid until the next rising edge of INT12 (or INT34) updates the status information.

The assigned interrupt INT12 is cleared if the appropriate registers (XR0, XR1, XR2 and XR3, read with command XOP := $3B_H$) are read via the serial µC-interface.

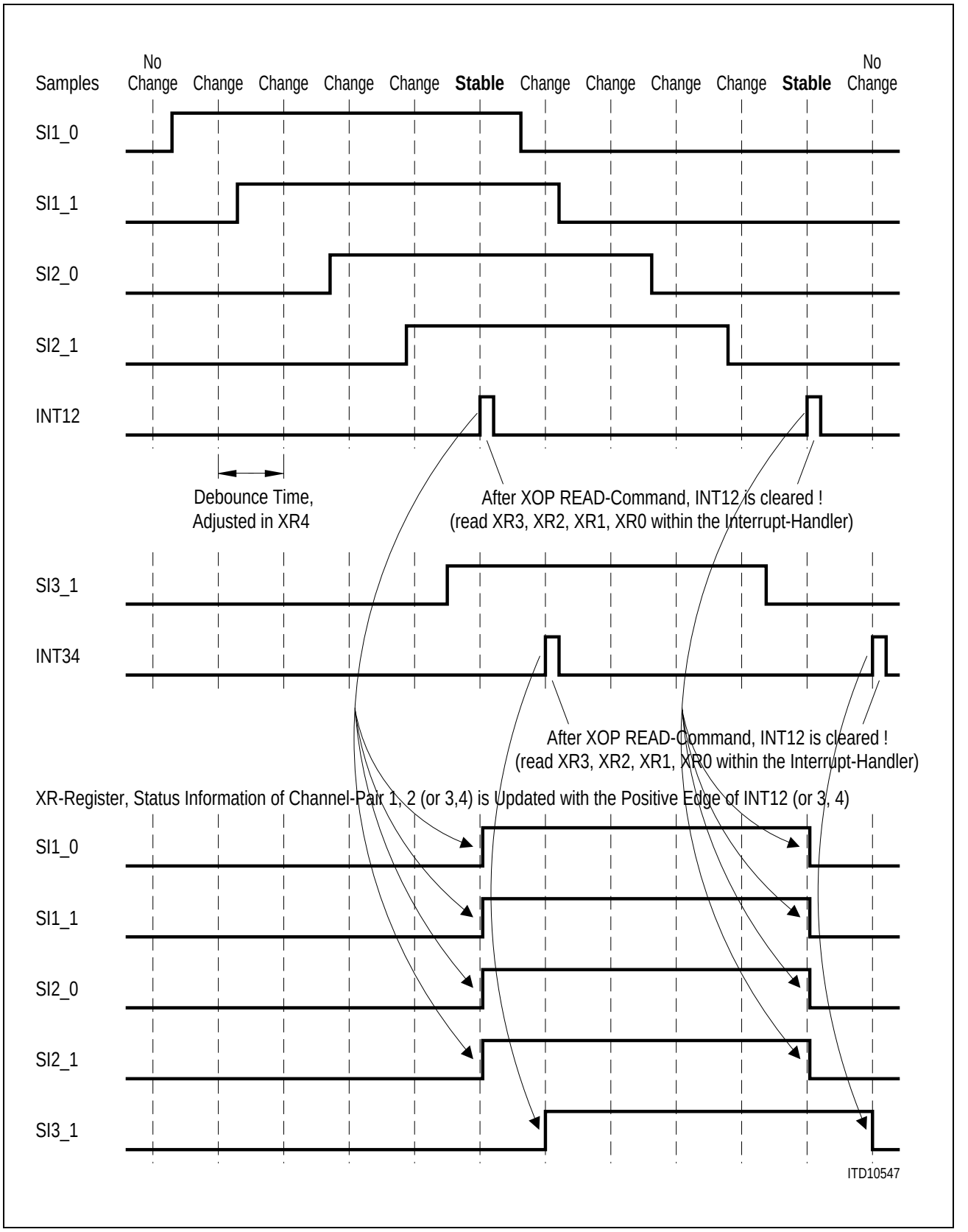
Samples
No Change
Change
Change
Change
Change
Change
Stable
Change
Change
Change
Change
Stable
No Change
SI1_0
SI1_1
SI2_0
SI2_1
INT12
Debounce Time, Adjusted in XR4
After XOP READ-Command, INT12 is cleared ! (read XR3, XR2, XR1, XR0 within the Interrupt-Handler)
SI3_1
INT34
After XOP READ-Command, INT12 is cleared ! (read XR3, XR2, XR1, XR0 within the Interrupt-Handler)
XR-Register, Status Information of Channel-Pair 1, 2 (or 3,4) is Updated with the Positive Edge of INT12 (or 3, 4)
SI1_0
SI1_1
SI2_0
SI2_1
SI3_1
ITD10547

Figure 3

2 XR4 Extended Register 4

Register XR4 provides two optional functions: debouncing of signaling input changes, and the configuration of the programmable output pin RGEN.

Bit	7	6	5	4	3	2	1	0
	N				T			

Signaling Debounce Interval N

To restrict the rate of changes on signaling input pins, deglitching of the status information from the SLIC may be applied.

An interrupt on pin INT12 (or INT34) will be generated, after all inputs of the assigned channel-pair-1,2 (or 3,4) have been stable for N milliseconds. New status information of the affected channel-pair-1,2 (or 3,4) will be read into registers XR0, XR1 and XR3 with the rising edge of the assigned interrupt INT12 (or INT34). The status information stays valid until the next interrupt INT12 (or INT34) occurs to update the XR-registers.

N is programmable in the range of 2 to 26 ms in steps of 2 ms. If N is programmed to “1111”, the debounce time is adjusted to 0.5 ms. The bit combination N = “1110” is reserved for future use.

With N = 0 the debouncing and the interrupt generation is disabled, the current signaling status can be read via the µC-interface (XOP-read command).

Table 1

Field N				Debounce Interval Time
0	0	0	0	Debounce and interrupt generation is disabled
0	0	0	1	Debounce period 2 ms
0	0	1	0	Debounce period 4 ms
.	.	.	.	.
.	.	.	.	.
1	1	0	1	Debounce period 26 ms
1	1	1	0	reserved
1	1	1	1	Debounce period 0.5 ms

Table 2 Configuration of RGEN

Field T				Frequency Applied to Pin RGEN
0	0	0	0	RGEN is set to 1 permanently
0	0	0	1	T is 2 ms
0	0	1	0	T is 4 ms
.	.	.	.	.
.	.	.	.	.
1	1	0	1	T is 26 ms
1	1	1	0	T is 28 ms
1	1	1	1	RGEN is set to 0 permanently

3 Signaling Interface

Due to the correction of the Interrupt Handling, it is necessary to apply a valid clock signal to the DCL pin. Polling the Signaling Interface is not possible without the DCL clock running.

4 XR5 Extended Register 5

Bit	7	6	5	4	3	2	1	0
	0	0	CR_DU	CR_DD	CHCLK		Version	

A crash occurs, if 2 or more channels are programmed to transmit (talk) in the same timeslot on the same highway. In this case a crash-bit will be set and transmission will be disabled for all affected channels. After correct timeslot programming (CR5 of the effected channels), the crash-bit will be cleared after XR5 was read.

The Version-Bitfield identifies the current chip version and has been changed to ‘01’ in version V1.4.