E2E0010-38-94

OKI Semiconductor

MSM6351/6351L

Built-in 8 or 5 bit Serial Port and LCD Driver 4-Bit Microcontroller

GENERAL DESCRIPTION

The MSM6351/6351L is a low-power microcontroller manufactured in silicon gate CMOS technology. Integrated into a single chip are ROM, RAM, five I/O ports, serial I/O port, time-base counter, LCD driver, three interrupts, crystal oscillator, and voltage tripler.

The MSM6351/6351L, which can drive LCD display with higher-count segments, is best suited to battery powered applications, such as watches and game machines.

The built-in 8-bit or 5-bit serial port provides a data communication capability with external machines.
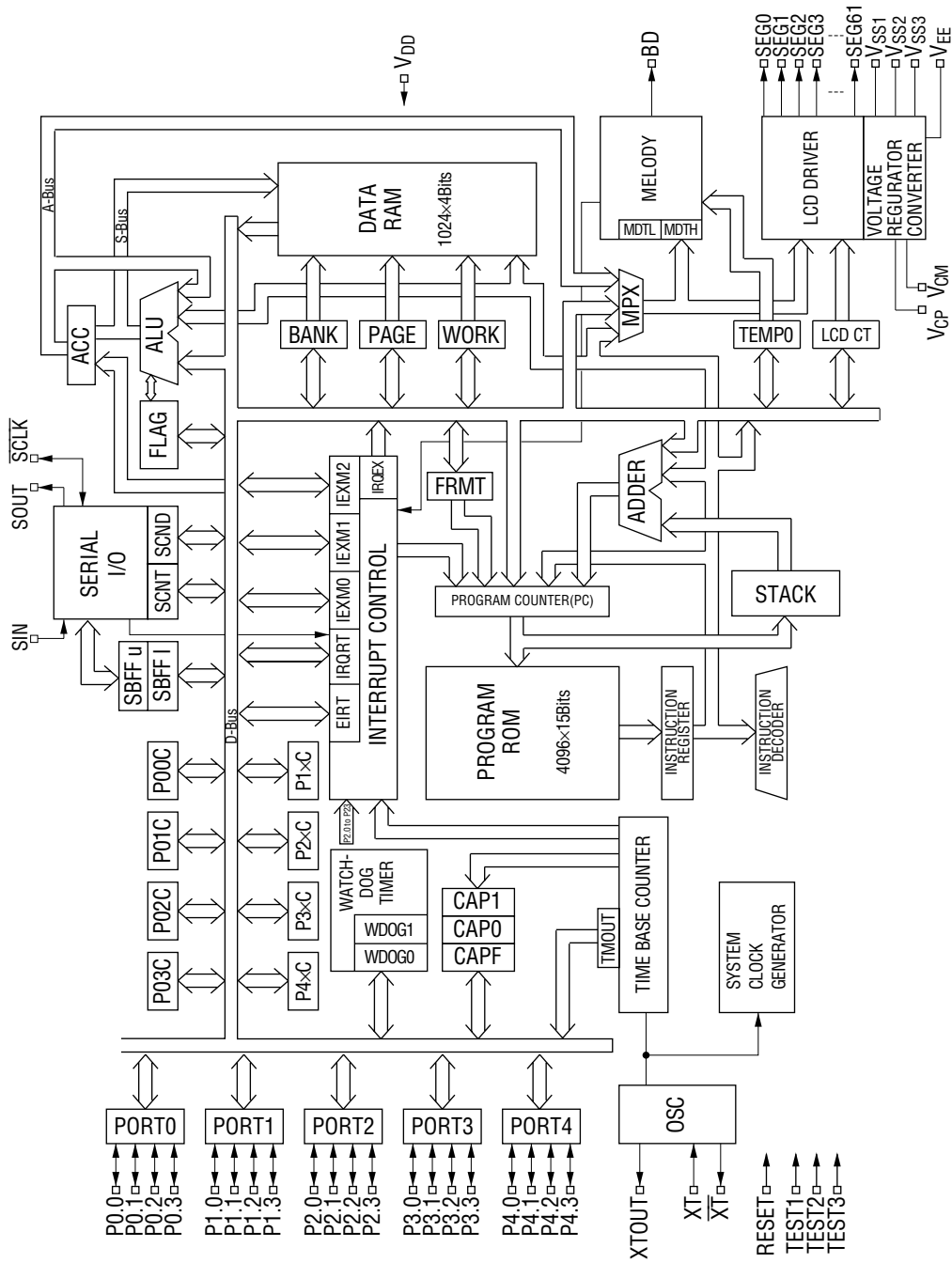
FEATURES

- Low power consumption
- Large capacity memory
- ROM   : 4096 words × 15 bits
- RAM   : 1024 words × 4 bits
- I/O port
      Input-output port   : 5 ports × 4 bits (input or output can be specified for each port)
- 62 LCD drivers (1/3 duty or 1/4 duty is selectable. Up to 232 segments can be displayed)
- Single 1.5 V power supply operation (MSM6351)
  Can be changed to 3.0 V specification by mask option (MSM6351L).
- Melody function
- Built-in watchdog timer
- Built-in 8-bit or 5-bit serial port (asynchronous or synchronous selectable)
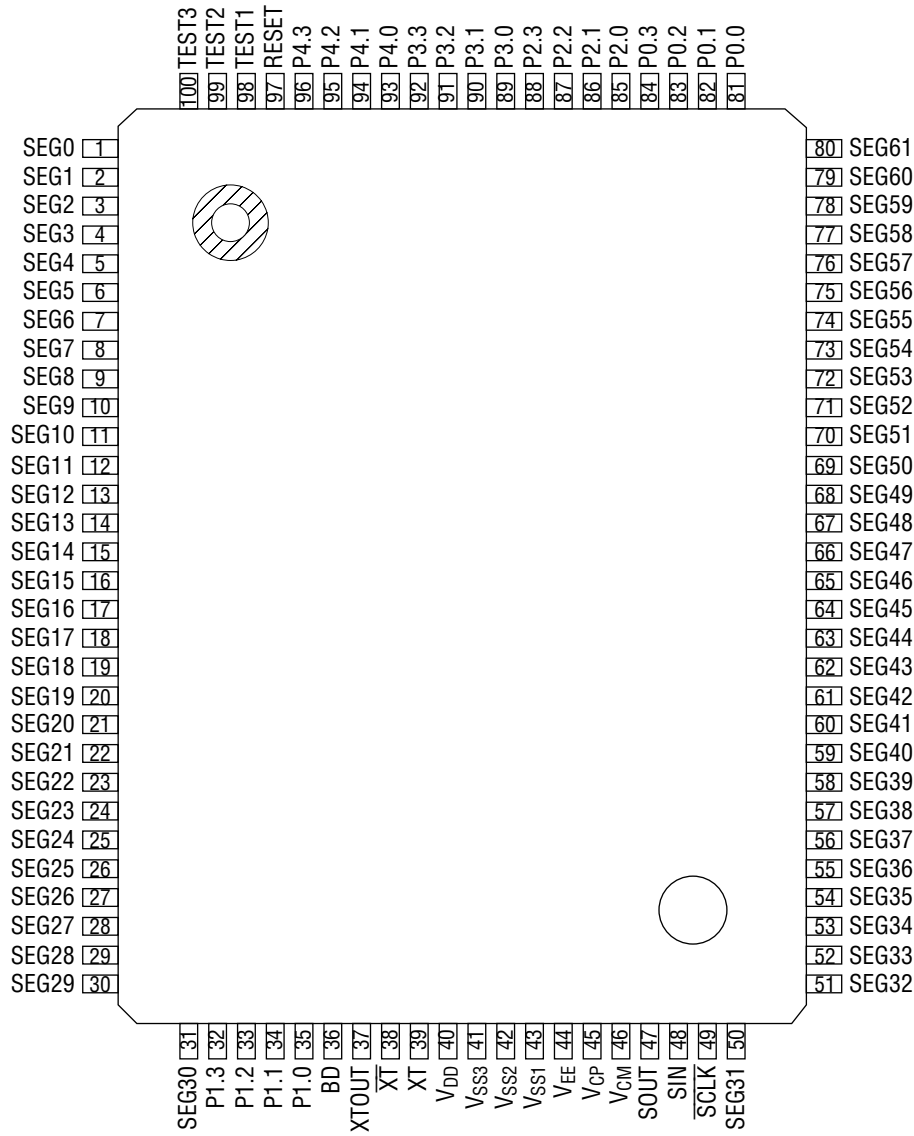- 32.768 kHz crystal oscillator
- Package options:
      100-pin plastic QFP (QFP100-P-1420-0.65-K)   (Product name :MSM6351-××GS-K/
                                                          MSM6351L-××GS-K)
      100-pin plastic QFP (QFP100-P-1420-0.65-L)   (Product name :MSM6351-××GS-L/
                                                          MSM6351L-××GS-L)
      100-pin plastic QFP (QFP100-P-1420-0.65-BK) (Product name :MSM6351-××GS-BK/
                                                          MSM6351L-××GS-BK)

      Chip

                                            ×× indicates a code number.

BLOCK DIAGRAM

V_{DD}

BD

SEG0 SEG1 SEG2 SEG3 --- SEG61 V_{SS1} V_{SS2} V_{SS3} V_{EE}

MELODY

LCD DRIVER

VOLTAGE REGURATOR CONVERTER

A-Bus

S-Bus

DATA RAM 1024×4Bits

MDTL MDTH

V_{CM}

V_{CP}

ACC

ALU

BANK PAGE WORK

MPX

TEMP0 LCD CT

FLAG

SCLK

SOUT

IEXM2

IRQEX

FRMT

ADDER

SERIAL I/O

SCNT SCND

IEXM1

STACK

SIN

SCNT

IEXM0

PROGRAM COUNTER(PC)

SBFF u SBFF l

EIRT IRQRT

INTERRUPT CONTROL

D-Bus

P00C P1×C

PROGRAM ROM 4096×15Bits

INSTRUCTION REGISTER

INSTRUCTION DECODER

P01C P2×C

P2.0 to P2.2

P02C P3×C

WATCH-DOG TIMER

CAP1

TIME BASE COUNTER

SYSTEM CLOCK GENERATOR

P03C P4×C

WDOG1

WDOG0

CAP0

CAPF

TMOUT

PORT0 PORT1 PORT2 PORT3 PORT4

OSC

P0.0 P0.1 P0.2 P0.3

P1.0 P1.1 P1.2 P1.3

P2.0 P2.1 P2.2 P2.3

P3.0 P3.1 P3.2 P3.3

P4.0 P4.1 P4.2 P4.3

XTOUT

XT $\overline{XT}$

RESET TEST1 TEST2 TEST3

PIN CONFIGURATION (TOP VIEW)

Top side pins (left to right): 100 TEST3, 99 TEST2, 98 TEST1, 97 RESET, 96 P4.3, 95 P4.2, 94 P4.1, 93 P4.0, 92 P3.3, 91 P3.2, 90 P3.1, 89 P3.0, 88 P2.3, 87 P2.2, 86 P2.1, 85 P2.0, 84 P0.3, 83 P0.2, 82 P0.1, 81 P0.0

Left side pins (top to bottom):

Pin	Signal
1	SEG0
2	SEG1
3	SEG2
4	SEG3
5	SEG4
6	SEG5
7	SEG6
8	SEG7
9	SEG8
10	SEG9
11	SEG10
12	SEG11
13	SEG12
14	SEG13
15	SEG14
16	SEG15
17	SEG16
18	SEG17
19	SEG18
20	SEG19
21	SEG20
22	SEG21
23	SEG22
24	SEG23
25	SEG24
26	SEG25
27	SEG26
28	SEG27
29	SEG28
30	SEG29

Right side pins (top to bottom):

Pin	Signal
80	SEG61
79	SEG60
78	SEG59
77	SEG58
76	SEG57
75	SEG56
74	SEG55
73	SEG54
72	SEG53
71	SEG52
70	SEG51
69	SEG50
68	SEG49
67	SEG48
66	SEG47
65	SEG46
64	SEG45
63	SEG44
62	SEG43
61	SEG42
60	SEG41
59	SEG40
58	SEG39
57	SEG38
56	SEG37
55	SEG36
54	SEG35
53	SEG34
52	SEG33
51	SEG32

Bottom side pins (left to right): 31 SEG30, 32 P1.3, 33 P1.2, 34 P1.1, 35 P1.0, 36 BD, 37 XTOUT, 38 $\overline{XT}$, 39 XT, 40 V_{DD}, 41 V_{SS3}, 42 V_{SS2}, 43 V_{SS1}, 44 V_{EE}, 45 V_{CP}, 46 V_{CM}, 47 SOUT, 48 SIN, 49 SCLK, 50 SEG31

100-Pin Plastic QFP

PIN DESCRIPTIONS

| Symbol	Type	Description				I/O Circuitry
P0.0	I/O	PORT0	• 4-bit I/O port 0 The input (*) /output, the existence (*) / absence of pull-down resistance, and the HALT function release enable/disable (*) condition can be selected for each bit.		Capture trigger signal	A
P0.1						
P0.2						
P0.3						
P1.0 to P1.3		PORT1	• 4-bit I/O port 1	The input (*) /output, the existence (*) / absence of pull-down resistance, and the HALT function release enable/disable (*) condition can be selected for each port.		
P2.0		PORT2	• 4-bit I/O port 2		External interrupt signal	
P2.1						
P2.2						
P2.3						
P3.0 to P3.3		PORT3	• 4-bit I/O port 3			
P4.0 to P4.3		PORT4	• 4-bit I/O port 4			
XTOUT	O	• Oscillator clock output. The oscillator clock is output when XTF (bit 3 of port P00C) is set to "1".				E
$\overline{XT}$	O	• Oscillator connection pins.				B
XT	I					
RESET	I	• Reset input. This is an input with a pull-down resistor. The system is reset when "1" is input.				C
TEST1	I	• Test input. This is an input with a pull-down resistor.				D
TEST2						
TEST3						
SIN	I	• Serial port data input.				F
SOUT	O	• Serial port data output. When the port is not in an output state, this pin is set at high-impedance level, except when HZOUT (bit 3 of port P2XC) =1 and transmitting data.				G
$\overline{SCLK}$	I/O	• Serial port clock input/output. The input/output (*) is switched by the serial port control register SCNT. In the output mode, the serial clock frequency can be selected from the demultiplied signal (1/1, 1/2 or 1/4 of the system clock).				H
BD	O	• Melody output (buzzer drive output).				I
SEG0 to SEG61	O	• LCD drive output with 1/3 bias and 1/3 duty, or 1/3 bias and 1/4 duty. The duty can be switched by LCD control register LCDCNT. A maximum of 177 segments can be displayed when using 1/3 duty and 232 when using 1/4 duty.				—

*   Means system reset conditions.

PIN DESCRIPTIONS (continued)

| Symbol	Description	I/O Circuitry
V_{DD}	• 0 V power supply pin	—
V_{SS1}	• −1.5 V power supply pin (for 1.5 V operation)	—
V_{SS2}	• −3.0 V power supply pin (for 3.0 V operation)	—
V_{SS3}	• −4.5 V power supply pin	—
V_{EE}	• Internal logic power supply pin	—
V_{CM}	• Internal voltage converter capacitor connecting pin	—
V_{CP}		

Circuitry on Input/Output Pins

A. Input/output port
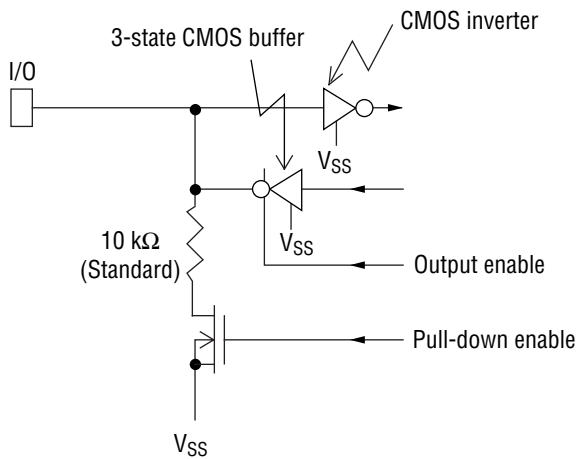
Note:

V_{SS}: $\begin{cases} \text{1.5 V operation} \rightarrow V_{SS1} \\ \text{3.0 V operation} \rightarrow V_{SS2} \end{cases}$

B. Oscillator
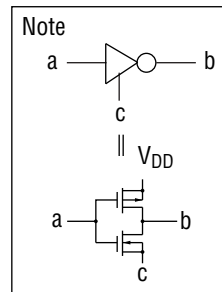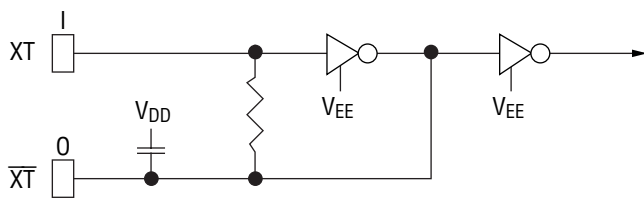
Circuitry on Input/Output Pins (continued)

C. RESET input
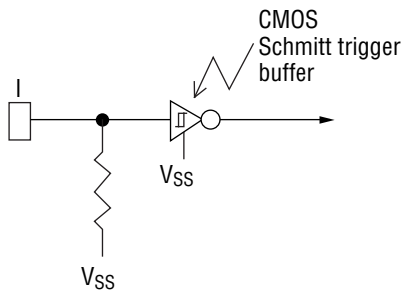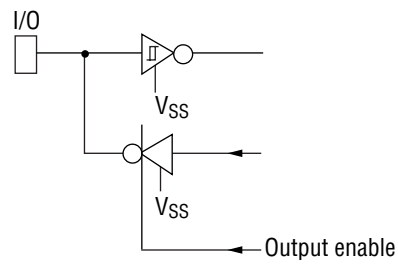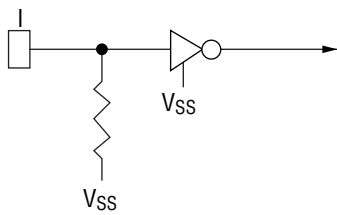
D. TEST input
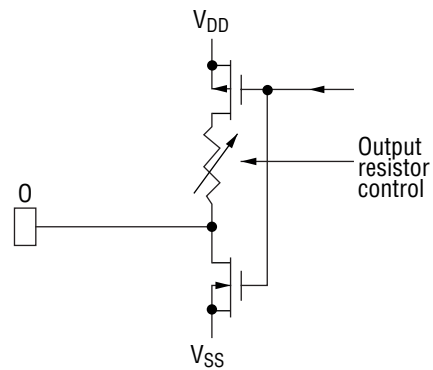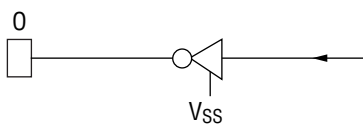
E. XTOUT output

F. SIN input

G. SOUT output

H. $\overline{\text{SCLK}}$ input/output
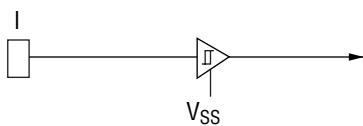
I. BD output
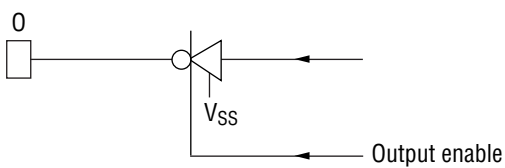
ABSOLUTE MAXIMUM RATINGS (MSM6351 (1.5 V Battery), BUF = "0")

V_{DD} = 0 V (V_{SS1} = Battery Voltage)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	—		−6.0 to +0.3	
Input Voltage	V_{IN}		V_{SS1} − 0.3 to V_{SS1} + 0.3	
Output Voltage *1	V_{O1}	Ta = 25°C	V_{SS1} − 0.3 to V_{SS1} + 0.3	V
Output Voltage *2	V_{O2}		−6.0 to +0.3	
Storage Temperature	T_{STG}	—	−55 to +125	°C

*1 Normal output
*2 LCD driver output

RECOMMENDED OPERATING CONDITIONS (MSM6351 (1.5 V Battery), BUF = "0")

V_{DD} = 0 V (V_{SS1} = Battery Voltage)

Parameter	Symbol	Condition	Range	Unit
Operating Voltage	V_{op}	BUF = "0"	−1.75 to −1.25	V
Operating Temperature	T_{op}	—	−20 to +70	°C
Operating Frequency	f_{OSC}	—	32.768	kHz

ELECTRICAL CHARACTERISTICS (MSM6351 (1.5 V Battery), BUF = "0")

V_{DD} = 0 V, V_{SS1} = −1.5 V (Battery Voltage), V_{SS2} = −3.0 V, V_{SS3} = −4.5 V, f_{OSC} = 32.768 kHz, C_X = 35 pF, Ta = 25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied Pin
Power Supply Current	I_{DD}	*1 *2	—	3.0	—	μA	—
Voltage for Oscillation Start	$-V_{OSC}$	Within 2 sec.	—	—	1.4	V	—
Output Current 1 ⟨ Common/Segment Output ⟩	$-I_{OH1}$	V_{OH} = −0.2 V	4	—	—	μA	SEG0 to SEG61
	$\lvert I_{OMH1} \rvert$	V_{OMH} = V_{SS1} ±0.2 V	4	—	—		
	$\lvert I_{OML1} \rvert$	V_{OML} = V_{SS2} ±0.2 V	4	—	—		
	$-I_{OL1}$	V_{OL} = −4.3 V	4	—	—		
Output Current 2	$-I_{OH2}$	V_O = −0.5 V	150	—	—	μA	PORT0 to PORT4 *3, SOUT, SCLK, XTOUT
	I_{OL2}	V_O = −1.0 V	150	—	—		
Output Current 3	$-I_{OH3}$	V_O = −0.5 V	7	—	—	μA	BD
	I_{OL3}	V_O = −1.0 V	20	—	—		
Input Current 1	$-I_{IH1}$	V_I = 0 V I/O input With pull-down resistor	75	150	300	μA	PORT0 to PORT4
Input Leakage Current	$\lvert I_{IL2} \rvert$	V_I = 0 V, −1.5 V I/O input Without pull-down resistor	—	—	1	μA	PORT0 to PORT4, SCLK, SIN, SOUT
Input Current 3	$-I_{IH3}$	V_I = 0 V With pull-down resistor	—	4	—	μA	RESET
Input Voltage	$-V_{IH}$	—	—	—	0.3	V	All input pins
	$-V_{IL}$	—	1.2	—	—		

*1   This value depends on program.

*2   BUF = "0"

*3   PORT0 = P0.0 to P0.3, PORT1 = P1.0 to P1.3, PORT2 = P2.0 to P2.3, PORT3 = P3.0 to P3.3, PORT4 = P4.0 to P4.3

ABSOLUTE MAXIMUM RATINGS (MSM6351L (3.0 V Battery), Halver used (BUF = "0"))

V_{DD} = 0 V (V_{SS2} = Battery Voltage)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	—		−6.0 to +0.3	
Input Voltage	V_{IN}		V_{SS2} − 0.3 to V_{SS2} + 0.3	
Output Voltage *1	V_{O1}	Ta = 25°C	V_{SS2} − 0.3 to V_{SS2} + 0.3	V
Output Voltage *2	V_{O2}		−6.0 to +0.3	
Storage Temperature	T_{STG}	—	−55 to +125	°C

*1 Normal output
*2 LCD driver output

RECOMMENDED OPERATING CONDITIONS

(MSM6351L (3.0 V Battery), Halver used (BUF = "0"))

V_{DD} = 0 V (V_{SS2} = Battery Voltage)

Parameter	Symbol	Condition	Range	Unit
Operating Voltage	V_{op}	Halver used (BUF = "0")	−3.5 to −2.6	V
Operating Temperature	T_{op}	—	−20 to +70	°C
Operating Frequency	f_{OSC}	—	32.768	kHz

ELECTRICAL CHARACTERISTICS (MSM6351L (3.0 V Battery), Halver used (BUF="0"))

$V_{DD} = 0$ V, $V_{SS1} = -1.5$ V, $V_{SS2} = -3.0$ V (Battery Voltage), $V_{SS3} = -4.5$ V, $f_{OSC} = 32.768$ kHz, $C_X = 35$ pF, Ta = 25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied Pin
Power Supply Current	I_{DD}	*1 *2	—	1.5	—	µA	—
Voltage for Oscillation Start	$-V_{OSC}$	Within 2 sec.	—	—	2.4	V	—
Output Current 1 < Common/Segment Output >	$-I_{OH1}$	$V_{OH} = -0.2$ V	4	—	—	µA	SEG0 to SEG61
	$|I_{OMH1}|$	$V_{OMH} = V_{SS1} \pm 0.2$ V	4	—	—		
	$|I_{OML1}|$	$V_{OML} = V_{SS2} \pm 0.2$ V	4	—	—		
	$-I_{OL1}$	$V_{OL} = -4.3$ V	4	—	—		
Output Current 2	$-I_{OH2}$	$V_O = -0.5$ V	500	—	—	µA	PORT0 to PORT4 *3, SOUT, $\overline{SCLK}$, XTOUT
	$-I_{OL2}$	$V_O = -2.5$ V	500	—	—		
Output Current 3	$-I_{OH3}$	$V_O = -0.5$ V	7	—	—	µA	BD
	$-I_{OL3}$	$V_O = -2.5$ V	20	—	—		
Input Current 1	$-I_{IH1}$	$V_I = 0$ V I/O input With pull-down resistor	150	300	600	µA	PORT0 to PORT4
Input Leakage Current	$|I_{IL2}|$	$V_I = 0$ V, -3 V I/O input Without pull-down resistor	—	—	1	µA	PORT0 to PORT4, $\overline{SCLK}$, SIN, SOUT
Input Current 3	$-I_{IH3}$	$V_I = 0$ V With pull-down resistor	—	25	—	µA	RESET
Input Voltage	$-V_{IH}$	—	—	—	0.5	V	All input pins
	$-V_{IL}$	—	2.5	—	—		

*1 This value depends on program.
*2 When 3 V battery with halver is used (BUF = "0")
*3 PORT0 = P0.0 to P0.3, PORT1 = P1.0 to P1.3, PORT2 = P2.0 to P2.3, PORT3 = P3.0 to P3.3,
PORT4 = P4.0 to P4.3

ABSOLUTE MAXIMUM RATINGS (MSM6351L (3.0 V Battery), Halver not used (BUF = "1"))

V_{DD} = 0 V (V_{SS2} = Battery Voltage)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	—		−6.0 to +0.3	
Input Voltage	V_{IN}	Ta = 25°C	V_{SS2} − 0.3 to +0.3	V
Output Voltage *1	V_{O1}		V_{SS2} − 0.3 to +0.3	
Output Voltage *2	V_{O2}		−6.0 to +0.3	
Storage Temperature	T_{STG}	—	−55 to +125	°C

*1 Normal output
*2 LCD driver output

RECOMMENDED OPERATING CONDITIONS

(MSM6351L (3.0 V Battery), Halver not used (BUF = "1"))

V_{DD} = 0 V (V_{SS2} = Battery Voltage)

Parameter	Symbol	Condition	Range	Unit
Operating Voltage	V_{op}	Halver not used (BUF = "1")	−3.5 to −2.2	V
Operating Temperature	T_{op}	—	−20 to +70	°C
Operating Frequency	f_{OSC}	—	32.768	kHz

ELECTRICAL CHARACTERISTICS (MSM6351L (3.0 V Battery), Halver not used (BUF="1"))

$V_{DD} = 0$ V, $V_{SS1} = -1.5$ V, $V_{SS2} = -3.0$ V (Battery Voltage), $V_{SS3} = -4.5$ V, $f_{OSC} = 32.768$ kHz, $C_X = 35$ pF, $Ta = 25°C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied Pin
Power Supply Current	I_{DD}	*1 *2	—	3.0	—	µA	—
Voltage for Oscillation Start	$-V_{OSC}$	Within 2 sec.	—	—	2.4	V	—
Output Current 1 Common/Segment Output	$-I_{OH1}$	$V_{OH} = -0.2$ V	4	—	—	µA	SEG0 to SEG61
	$\vert I_{OMH1} \vert$	$V_{OMH} = V_{SS1}$ ±0.2 V	4	—	—		
	$\vert I_{OML1} \vert$	$V_{OML} = V_{SS2}$ ±0.2 V	4	—	—		
	$-I_{OL1}$	$V_{OL} = -4.3$ V	4	—	—		
Output Current 2	$-I_{OH2}$	$V_O = -0.5$ V	500	—	—	µA	PORT0 to PORT4 *3, SOUT, SCLK, XTOUT
	$-I_{OL2}$	$V_O = -2.5$ V	500	—	—		
Output Current 3	$-I_{OH3}$	$V_O = -0.5$ V	7	—	—	µA	BD
	$-I_{OL3}$	$V_O = -2.5$ V	20	—	—		
Input Current 1	$-I_{IH1}$	$V_I = 0$ V I/O input With pull-down resistor	150	300	600	µA	PORT0 to PORT4
Input Leakage Current	$\vert I_{IL2} \vert$	$V_I = 0$ V, -3 V I/O input Without pull-down resistor	—	—	1	µA	PORT0 to PORT4, SCLK, SIN, SOUT
Input Current 3	$-I_{IH3}$	$V_I = 0$ V With pull-down resistor	—	25	—	µA	RESET
Input Voltage	$-V_{IH}$	—	—	—	0.5	V	All input pins
	$-V_{IL}$	—	2.5	—	—		

*1 This value depends on program.
*2 When halver is not used (BUF = "1")
*3 PORT0 = P0.0 to P0.3, PORT1 = P1.0 to P1.3, PORT2 = P2.0 to P2.3, PORT3 = P3.0 to P3.3, PORT4 = P4.0 to P4.3

INSTRUCTION LIST

	Mnemonic	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description	Machine cycle
Arithmetic operation instruction	ADD ACC, REG1	0	0	0	0	0	0	P	0	1	0	0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←(rP) + (ACC)	1
	ADD #i, REG1	0	0	1	1	0	0	P	i_3	i_2	i_1	i_0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←(rP) +i	1
	ADC REG1	0	0	0	0	0	0	P	0	1	0	1	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←decimal adj [(rP) + (ACC) + (C)]	1
	ADCN REG1	0	1	1	0	0	0	P	N_3	N_2	N_1	N_0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←N adjust [(rP) + (C)]	1
	SUB ACC, REG1	0	0	0	0	0	1	P	0	1	0	0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←(rP) + (ACC)	1
	SUB #i, REG1	0	0	1	1	0	1	P	i_3	i_2	i_1	i_0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←(rP) −i	1
	SBC REG1	0	0	0	0	0	1	P	0	1	0	1	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←decimal adj [(rP) − (ACC) − (C)]	1
	SBCN REG1	0	1	1	0	0	1	P	N_3	N_2	N_1	N_0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←N adjust [(rP) − (C)]	1
	CMP ACC, REG1	0	0	0	0	0	1	P	1	1	1	0	r_3	r_2	r_1	r_0	(Z), (C)←(rP) − (ACC)	1
	CMP #i, REG1	0	0	1	0	1	1	P	i_3	i_2	i_1	i_0	r_3	r_2	r_1	r_0	(Z), (C)←(rP) − i	1
	INC REG1	0	0	0	0	0	0	P	0	0	0	1	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←(rP) +1	1
	INCD REG2	1	0	0	0	b_1	b_0	0	P_3	P_2	P_1	P_0	r_3	r_2	r_1	r_0	(rPb), (ACC), (Z), (C)←(rPb) +1	1
	DEC REG1	0	0	0	0	0	1	P	0	0	0	1	r_3	r_2	r_1	r_0	(rP), (ACC), (Z), (C)←(rP) −1	1
	DECD REG2	1	0	0	1	b_1	b_0	0	P_3	P_2	P_1	P_0	r_3	r_2	r_1	r_0	(rPb), (ACC), (Z), (C)←(rPb) −1	1
Bit manipulation instruction	BIT ACC, REG1	0	0	0	0	0	0	P	1	1	1	0	r_3	r_2	r_1	r_0	(Z)←(r$\overline{P_3}$)∧(ACC3)∨(r$\overline{P_2}$)∧(ACC2)∨(r$\overline{P_1}$)∧(ACC1)∨(r$\overline{P_0}$)∧(ACC0)	1
	BIT #i, REG1	0	0	1	0	1	0	P	i_3	i_2	i_1	i_0	r_3	r_2	r_1	r_0	(Z)←(r$\overline{P_3}$)∧i_3∨(r$\overline{P_2}$)∧i_2∨(r$\overline{P_1}$)∧i_1∨(r$\overline{P_0}$)∧i_0	1
	BIS ACC, REG1	0	0	0	0	0	0	P	0	1	1	0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z)←(rP)∨(ACC)	1
	BIS #i, REG1	0	0	1	0	0	0	P	i_3	i_2	i_1	i_0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z)←(rP)∨i	1
	BIC ACC, REG1	0	0	0	0	0	1	P	0	1	1	0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z)←(rP)∧($\overline{ACC}$)	1
	BIC #1, REG1	0	0	1	0	0	1	P	i_3	i_2	i_1	i_0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z)←(rP)∧$\overline{i}$	1
	XOR ACC, REG1	0	0	0	0	0	0	P	0	1	1	1	r_3	r_2	r_1	r_0	(rP), (ACC), (Z)←(rP)⊻(ACC)	1
	XOR #1, REG1	0	0	1	1	1	1	P	i_3	i_2	i_1	i_0	r_3	r_2	r_1	r_0	(rP), (ACC), (Z)←(rP)⊻ i	1
Rotate instruction	ROR REG1	0	0	0	0	0	0	P	0	0	1	0	r_3	r_2	r_1	r_0	(Z), (ACC)←[→(C)→(rP)→]	1
	ROL REG1	0	0	0	0	0	1	P	0	0	1	0	r_3	r_2	r_1	r_0	(Z), (ACC)←[←(C)←(rP)←]	1
	ASR REG1	0	0	0	0	0	0	P	0	0	1	1	r_3	r_2	r_1	r_0	(Z), (ACC)←[0→(rP)→(C)]	1
	ASL REG1	0	0	0	0	0	1	P	0	0	1	1	r_3	r_2	r_1	r_0	(Z), (ACC)←[(C)←(rP)←0]	1
Flag operation instruction	CLG	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	(G)←0	1
	CLC	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	(C)←0	1
	CLZ	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	(Z)←0	1
	CLA	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	(Z), (C), (G)←0	1
	SEG	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	(G)←1	1
	SEC	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	(C)←1	1
	SEZ	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	(Z)←1	1
	SEA	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0	(Z), (C), (G)←1	1

INSTRUCTION LIST (continued)

	Mnemonic	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description	Machine cycle
Data transfer instruction	MOV ACC, REG1	0	0	0	0	0	0	P	1	1	1	1	r_3	r_2	r_1	r_0	$(rP) \leftarrow (ACC)$	1
	MOVD ACC, REG2	1	0	1	0	b_1	b_0	0	P_3	P_2	P_1	P_0	r_3	r_2	r_1	r_0	$(rPb) \leftarrow (ACC)$	1
	MOV #i, REG1	0	0	1	1	1	0	P	i_3	i_2	i_1	i_0	r_3	r_2	r_1	r_0	$(rP), (ACC), (Z) \leftarrow i$	1
	MOV REG1, ACC	0	0	0	0	0	1	P	1	1	1	1	r_3	r_2	r_1	r_0	$(ACC), (Z) \leftarrow (rP)$	1
	MOVD REG2, ACC	1	0	1	1	b_1	b_0	0	P_3	P_2	P_1	P_0	r_3	r_2	r_1	r_0	$(ACC), (Z) \leftarrow (rPb)$	1
	EXG REG1	0	0	0	0	0	1	P	0	0	0	0	r_3	r_2	r_1	r_0	$(rP) \leftrightarrow (ACC)$	1
	EXGD REG2	0	1	1	1	b_1	b_0	0	P_3	P_2	P_1	P_0	r_3	r_2	r_1	r_0	$(rPb) \leftrightarrow (ACC)$	1
Subroutine instruction	CALL adrs	1	1	1	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	$(STACK) \leftarrow (PC), (PC) \leftarrow a_{11}$ to a_0, $(SP) \leftarrow (SP)+1$	1
	RET	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	$(PC) \leftarrow (STACK)+1, (SP) \leftarrow (SP)-1$	1
	RTI	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	$(PC) \leftarrow (STACK)+1, (SP) \leftarrow (SP)-1$ (at INT routine)	1
Jump instruction	JMP adrs	1	1	0	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	$(PC) \leftarrow a_{11}$ to a_0	1
	AMP @ REG1	0	0	0	0	0	0	0	1	1	0	1	r_3	r_2	r_1	r_0	$(PC) \leftarrow (PC)+(rP)+1$	1
	JMPO @ REG1	0	0	0	0	0	1	0	1	1	0	1	r_3	r_2	r_1	r_0	$(PC) \leftarrow (PC)+7 \wedge (rP)+1$	1
	BGT n	0	0	0	0	1	1	P	0	0	1	n_4	n_3	n_2	n_1	n_0	if $(G)=1$ then $(PC) \leftarrow (PC)+N$ else $(PC) \leftarrow (PC)+1$	1
	BLE n	0	0	0	0	1	1	P	1	0	1	n_4	n_3	n_2	n_1	n_0	if $(G)=0$ then $(PC) \leftarrow (PC)+N$ else $(PC) \leftarrow (PC)+1$	1
	BCS n	0	0	0	0	1	1	P	0	0	0	n_4	n_3	n_2	n_1	n_0	if $(C)=1$ then $(PC) \leftarrow (PC)+N$ else $(PC) \leftarrow (PC)+1$	1
	BCC n	0	0	0	0	1	1	P	1	0	0	n_4	n_3	n_2	n_1	n_0	if $(C)=0$ then $(PC) \leftarrow (PC)+N$ else $(PC) \leftarrow (PC)+1$	1
	BEQ n (BZE n)	0	0	0	0	1	1	P	0	1	0	n_4	n_3	n_2	n_1	n_0	if $(Z)=1$ then $(PC) \leftarrow (PC)+N$ else $(PC) \leftarrow (PC)+1$	1
	BNE n (BNZ n)	0	0	0	0	1	1	P	1	1	0	n_4	n_3	n_2	n_1	n_0	if $(Z)=0$ then $(PC) \leftarrow (PC)+N$ else $(PC) \leftarrow (PC)+1$	1
	BGE n	0	0	0	0	1	1	P	0	1	1	n_4	n_3	n_2	n_1	n_0	if {$(G)=1$ or $(Z)=1$} then $(PC) \leftarrow (PC)+N$ else $(PC) \leftarrow (PC)+1$	1
	BLT n	0	0	0	0	1	1	P	1	1	1	n_4	n_3	n_2	n_1	n_0	if {$(G)=0$ and $(Z)=0$} then $(PC) \leftarrow (PC)+N$ else $(PC) \leftarrow (PC)+1$	1
Melody start	MSA adrs *	0	0	0	0	1	0	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	Specifies the first address of note data. ($E00_H$~FFF_H)	2
Display instruction	DSP dig, REG1 *	0	0	0	1	0	0	P	dig_3	dig_2	dig_1	dig_0	r_3	r_2	r_1	r_0	digit (Low Part) $\leftarrow (rP), (ACC)$	1
	DSPH dig, REG1 *	0	0	0	1	0	1	P	dig_3	dig_2	dig_1	dig_0	r_3	r_2	r_1	r_0	digit (High Part) $\leftarrow (rP), (ACC)$	1
	DSPF dig, REG1 *	0	0	0	1	1	0	P	dig_3	dig_2	dig_1	dig_0	r_3	r_2	r_1	r_0	digit (Low Part) $\leftarrow (rP)$ via Table	2
	DSPF dig, REG1 *	0	0	0	1	1	1	P	dig_3	dig_2	dig_1	dig_0	r_3	r_2	r_1	r_0	digit (Low Part) $\leftarrow (rP)$ via Table	2
Input/output instruction	OUT REG1, PORT	0	1	0	1	0	y_4	P	y_3	y_2	y_1	y_0	r_3	r_2	r_1	r_0	$(PORTy) \leftarrow (rP)$	1
	OUT #i, PORT	0	1	0	1	1	y_4	P	y_3	y_2	y_1	y_0	i_3	i_2	i_1	i_0	$(PORTy) \leftarrow i$	1
	INP PORT, REG1	0	1	0	0	0	y_4	P	y_3	y_2	y_1	y_0	r_3	r_2	r_1	r_0	$(rP), (ACC) \leftarrow (PORTy)$	1
CPU control instruction	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NO Operation	1
	HALT	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	HALT CPU	1

When P=0 in bit 8, N=n+1; when P=1, N=−n.

PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-K

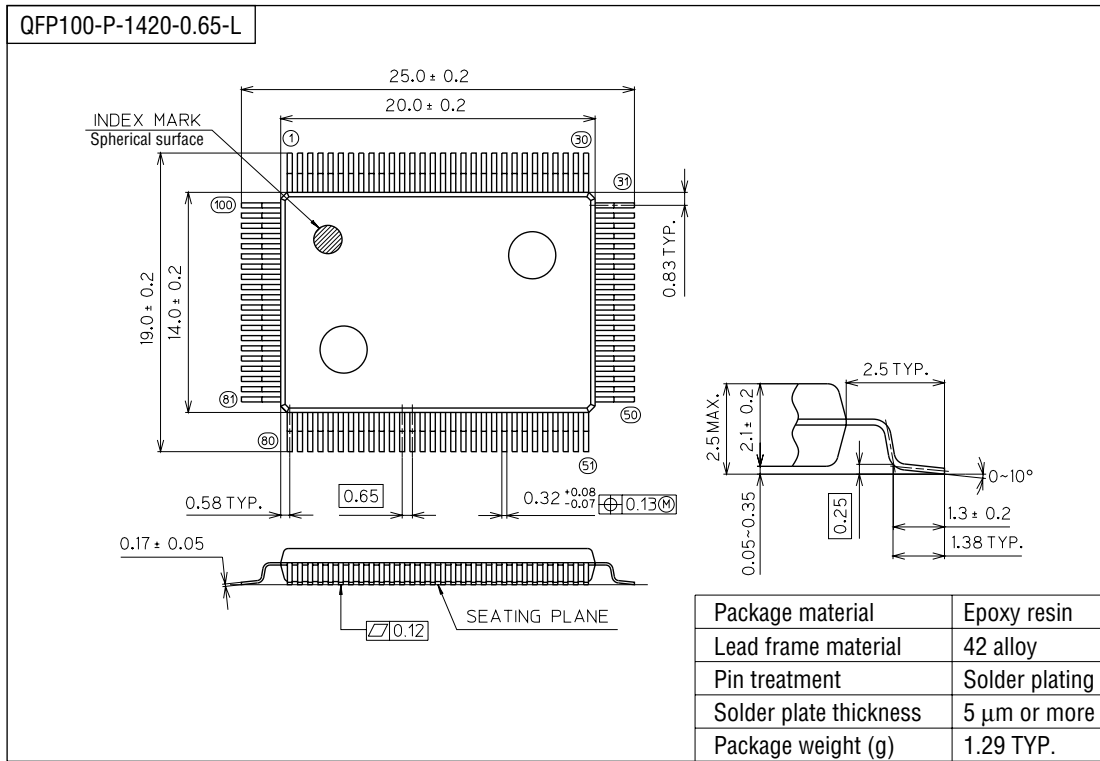| Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).
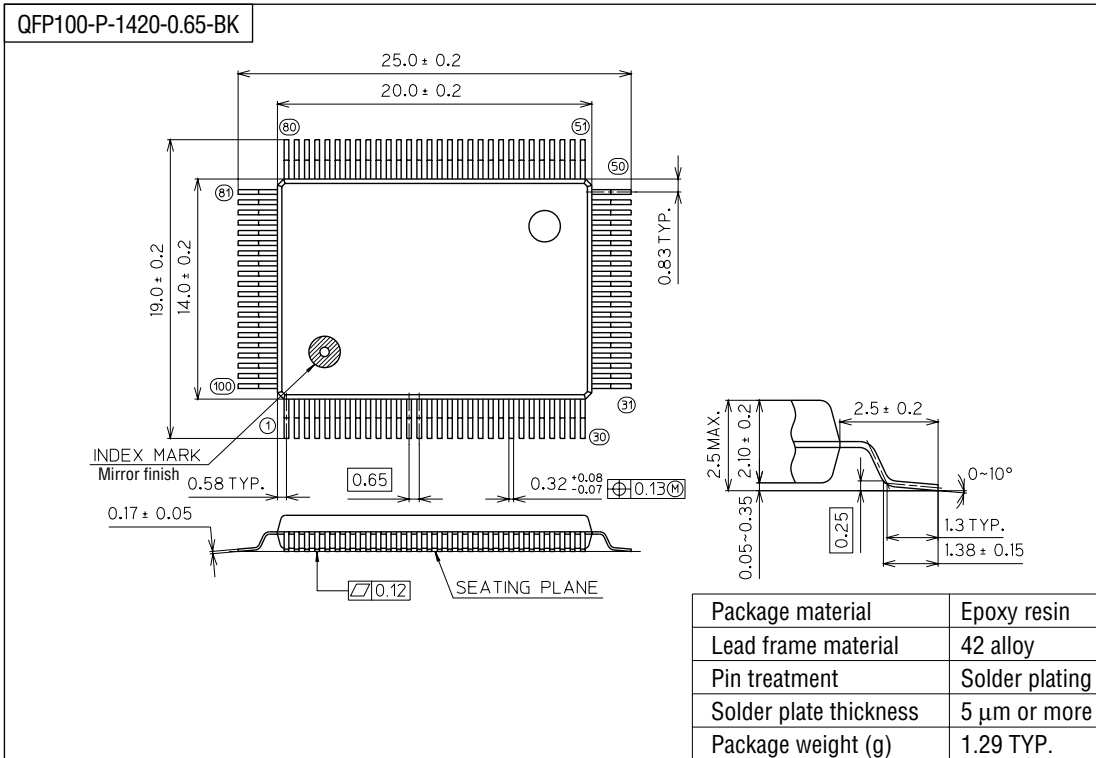
(Unit : mm)

QFP100-P-1420-0.65-L

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP100-P-1420-0.65-BK

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).