MOTOROLA

Advance Information

Critical Conduction GreenLine™ SMPS Controller

MC33364

CRITICAL CONDUCTION GREENLINE™ SMPS CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

The MC33364 series are variable frequency SMPS controllers that operate in the critical conduction mode. They are optimized for low power, high density power supplies requiring minimum board area, reduced component count, and low power dissipation. Each narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

Each MC33364 features an on–board reference, UVLO function, a watchdog timer to initiate output switching, a zero current detector to ensure critical conduction operation, a current sensing comparator, leading edge blanking, and a CMOS driver. Protection features include the ability to shut down switching, and cycle–by–cycle current limiting.

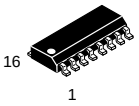
The MC33364D1 is available in a surface mount SO–8 package. It has an internal 126 kHz frequency clamp. For loads which have a low power operating condition, the frequency clamp limits the maximum operating frequency, preventing excessive switching losses and EMI radiation.

The MC33364D2 is available in the SO–8 package without an internal frequency clamp.

The MC33364D is available in the SO–16 package. It has an internal 126 kHz frequency clamp which is pinned out, so that the designer can adjust the clamp frequency by connecting appropriate values of resistance.

- Lossless Off–Line Startup
- Leading Edge Blanking for Noise Immunity
- Watchdog Timer to Initiate Switching
- Minimum Number of Support Components
- Shutdown Capability
- Over Temperature Protection
- Optional Frequency Clamp

D1, D2 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



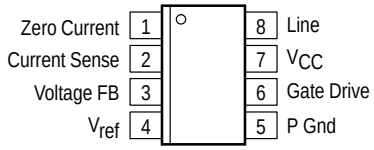
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33364D1	T_J = –25° to +125°C	SO–8
MC33364D2		SO–8
MC33364D		SO–16

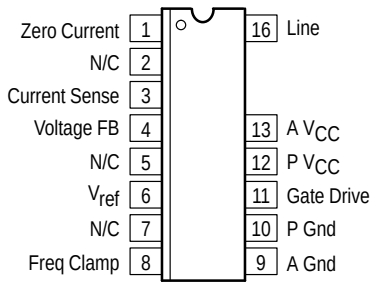
PIN CONNECTIONS

MC33364D1
MC33364D2



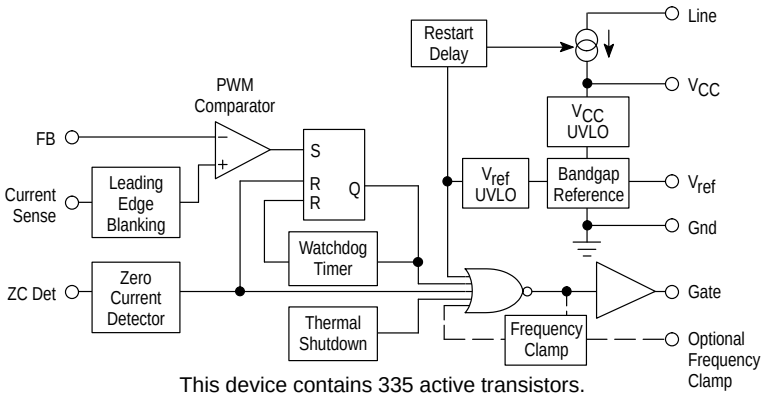
(Top View)

MC33364D



(Top View)

Representative Block Diagram



This device contains 335 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Transient)	V_{CC}	20	V
Power Supply Voltage (Operating)	V_{CC}	16	V
Line Voltage	V_{Line}	700	V
Current Sense, Compensation, Voltage Feedback, Restart Delay and Zero Current Input Voltage	V_{in1}	–1.0 to +10	V
Zero Current Detect Input	I_{in}	±5.0	mA
Restart Diode Current	I_{in}	5.0	mA
Power Dissipation and Thermal Characteristics D1 and D2 Suffix, Plastic Package Case 751 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air D Suffix, Plastic Package Case 751B–05 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 450 178 550 145	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +125	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_J = –25 to 125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REFERENCE					
Reference Output Voltage (I_{Out} = 0 mA, T_J = 25°C)	V_{ref}	4.90	5.05	5.20	V
Line Regulation (V_{CC} = 10 V to 20 V)	Reg_{line}	–	2.0	50	mV
Load Regulation (I_{Out} = 0 mA to 5.0 mA)	Reg_{load}	–	0.3	50	mV
Maximum V_{ref} Output Current	I_O	–	5	–	mA
Reference Undervoltage Lockout Threshold	V_{th}	–	4.5	–	V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	0.9	1.0	1.1	V
Hysteresis (V_{in} Decreasing)	V_H	–	200	–	mV
Input Clamp Voltage High State (I_{DET} = 3.0 mA) Low State (I_{DET} = –3.0 mA)	 V_{IH} V_{IL}	 9.0 –0.5	 10.33 –0.75	 12 –1.1	V
CURRENT SENSE COMPARATOR					
Input Bias Current (V_{CS} = 0 to 2.0 V)	I_{IB}	–0.5	0.02	0.5	μA
Built In Offset	V_{IO}	50	108	170	mV
Feedback Pin Input Range	V_{FB}	1.1	1.24	1.4	V
Feedback Pin to Output Delay	t_{DLY}	100	232	400	ns
DRIVE OUTPUT					
Source Resistance (Drive = 0 V, V_{Gate} = V_{CC} – 1.0 V) Sink Resistance (Drive = V_{CC}, V_{Gate} = 1.0 V)	R_{OH} R_{OL}	10 5	36 11	70 25	Ω Ω
Output Voltage Rise Time (25% – 75%) (C_L = 1.0 nF)	t_r	–	67	150	ns
Output Voltage Fall Time (75% – 25%) (C_L = 1.0 nF)	t_f	–	28	50	ns
Output Voltage in Undervoltage (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UV)}$	–	0.01	0.03	V

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_J = –25 to 125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
LEADING EDGE BLANKING					
Delay to Current Sense Comparator Input (V_{FB} = 2.0 V, V_{CS} = 0 V to 4.0 V step, C_L = 1.0 nF)	$t_{PHL(in/out)}$	–	250		ns
TIMER					
Watchdog Timer	t_{DLY}	200	410	700	µs
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	14	15	16	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	6.5	7.6	8.5	V
FREQUENCY CLAMP					
Internal FC Function (pin open)	f_{max}	90	126	160	kHz
Internal FC Function (pin grounded)	f_{max}	400	564	700	kHz
Frequency Clamp Input Threshold	$V_{th(FC)}$	–	2.0	–	V
Frequency Clamp Control Current Range	$I_{Control}$	30	70	110	µA
TOTAL DEVICE					
Line Startup Current (V_{Line} = 50 V) (V_{CC} = $V_{th(on)}$ – 1.0 V) Restart Delay Time	I_{Line} t_{DLY}	5.0	8.5 100	12	mA ms
Line Pin Leakage (V_{Line} = 575 V)	I_{Line}	0.5	32	70	µA
Line Startup Current (V_{CC} = 0 V, V_{Line} = 50 V)	I_{Line}	6.0	10	12	mA
V_{CC} Dynamic Operating Current (50 kHz, C_L = 1.0 nF) V_{CC} Static Operating Current (V_{CC} = 16 V, V_{ref} = 0)	I_{CC}	1.5 –	2.75 3.0	4.5 –	mA
V_{CC} Pin Leakage (V_{CC} = 11 V)	$I_{CC\ Lkg}$	300	544	800	µA

Figure 1. Drive Output Waveform

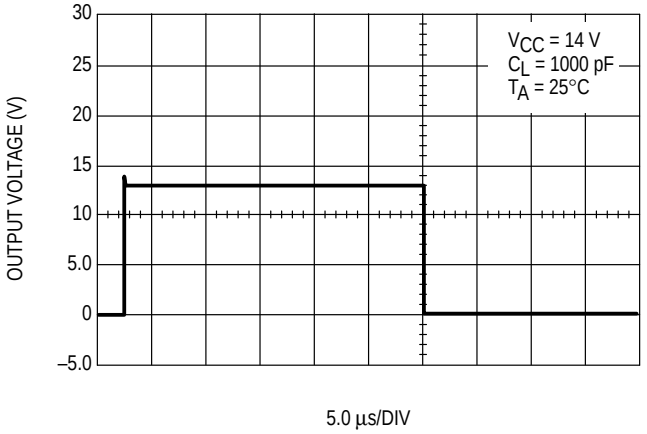


Figure 2. Watchdog Timer Delay versus Temperature

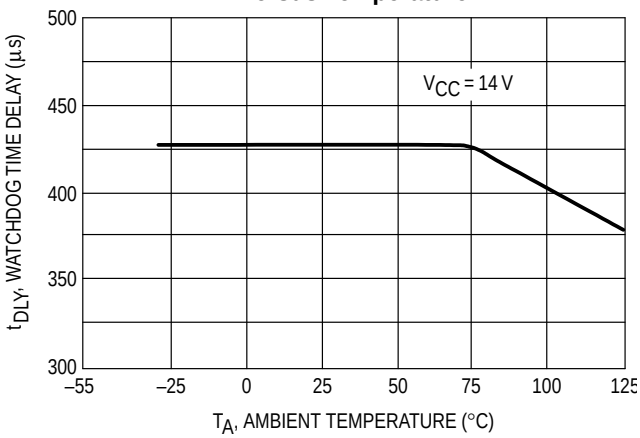


Figure 3. Reference Voltage versus Temperature

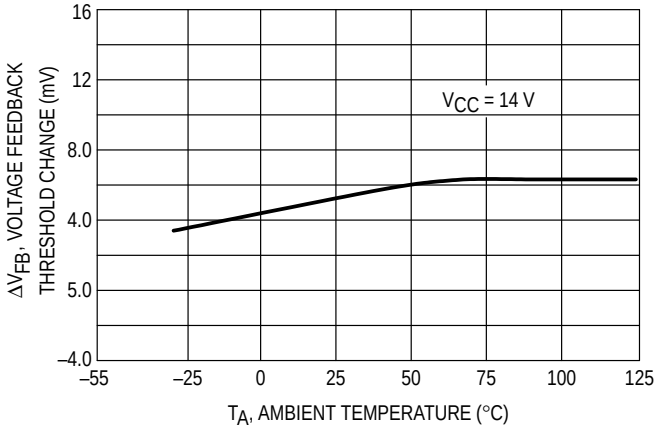


Figure 4. Supply Current versus Supply Voltage

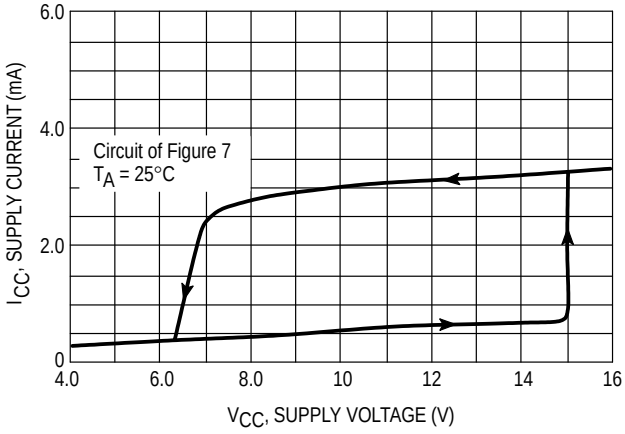


Figure 5. Transient Thermal Resistance

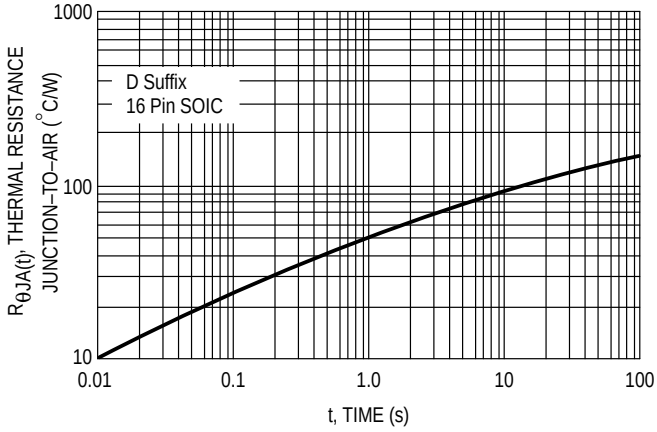
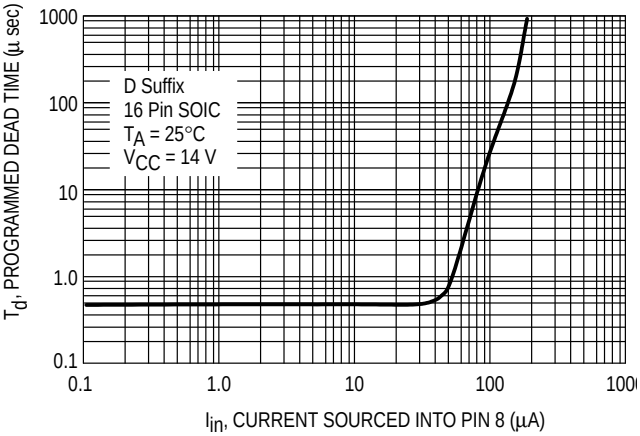


Figure 6. Dead Time versus Input Current

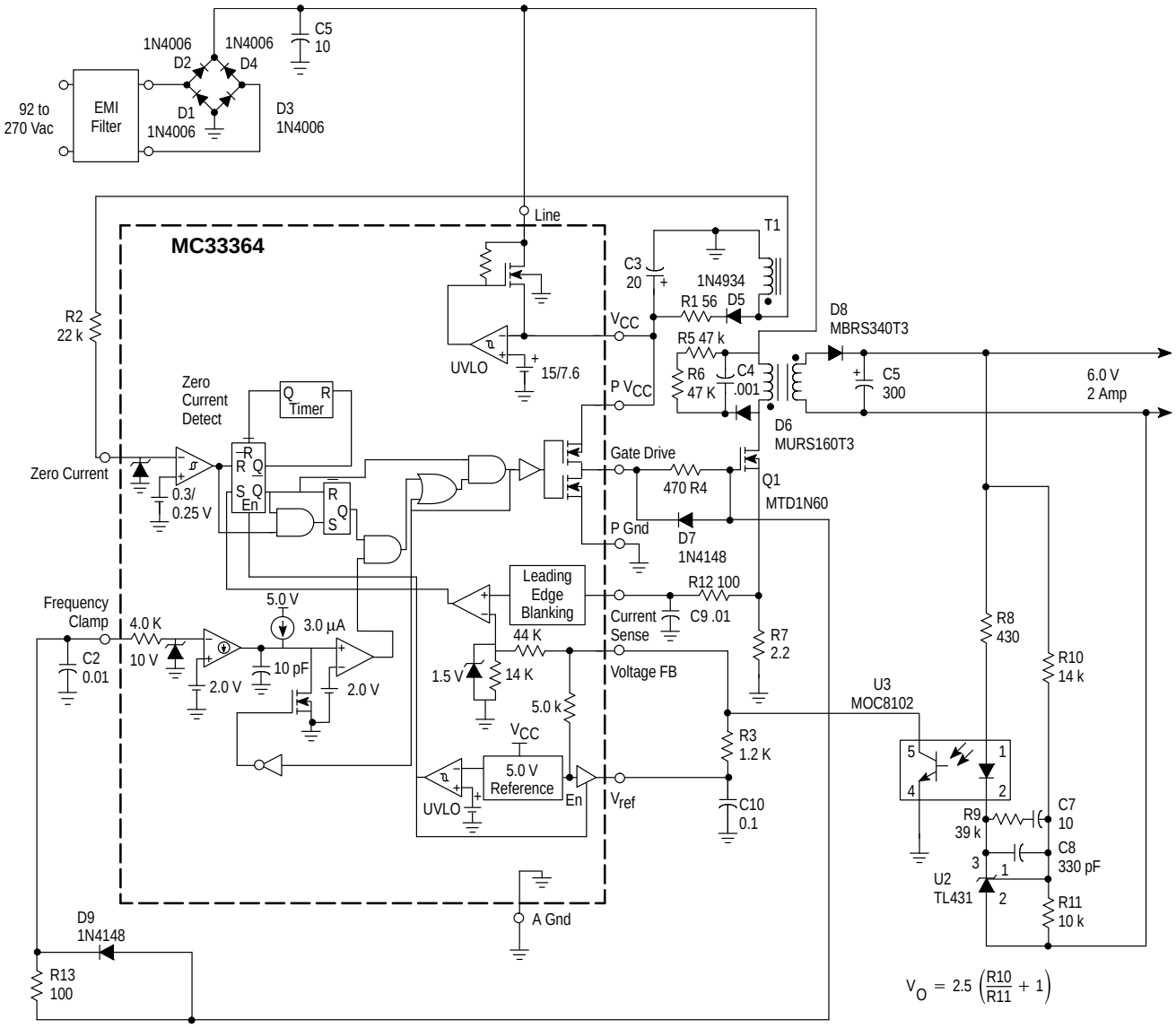


FUNCTIONAL DESCRIPTION

INTRODUCTION

With the goal of reducing the size and cost of off–line power supplies, there is an ever increasing demand for an economical method of obtaining a regulated galvanically isolated dc output voltage using a control which operates directly from the ac line. This data sheet describes a monolithic control IC that was specifically designed for power supply control with a minimal number of external components. It offers the designer a simple cost effective solution to obtain the benefits of off–line power regulation.

Figure 7. Functional Block Diagram



Operating Description

The MC33364 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. Referring to the block diagram in Figure 7, note that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Zero Current Detector

The MC33364 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the input threshold level. The Zero Current Detector initiates the next on–time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn–on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 0.25 V. To prevent false tripping, 50 mV of hysteresis is provided. The Zero Current Detector input is internally

protected by two clamps. The upper 0.7 V clamp prevents input overvoltage breakdown while the lower –0.7 V clamp prevents substrate injection. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps to 5.0 mA or less.

Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor in series with the source of output switch. This voltage is monitored by the Current Sense Input and compared to the divided down feedback voltage. The internal feedback voltage divider is limited to 1.5 V maximum. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.5\ V}{R_{Sense}}$$

The Current Sense Input to Drive Output propagation delay is typically 232 nS.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 410 microseconds after the inductor current reaches zero.

Undervoltage Lockout

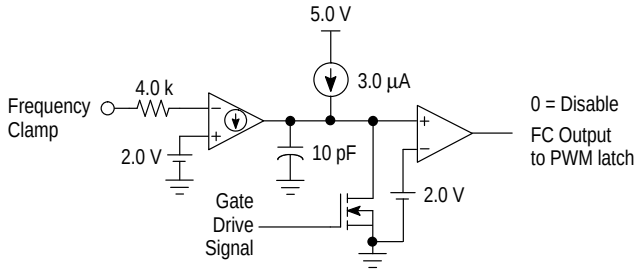
The MC33364 has a 5.0 V internal reference brought out to Pin 6 (D Suffix) or Pin 4 (D1 and D2 Suffixes) and capable of sourcing 10 mA typically. It also contains an Under Voltage Lockout (UVLO) circuit which suppresses the Gate output at Pin 11 if the V_{CC} supply voltage drops below 7.6 V typical.

Restart Delay

A restart delay function is provided to allow hiccup mode fault protection in case of a short circuit condition and to prevent the SMPS from repeatedly trying to restart after the input line voltage has been removed. When power is first applied, the V_{CC} bypass capacitor is charged through a constant current source. The Restart Delay turns off the high voltage startup MOSFET when V_{CC} reaches the startup threshold level. The Restart Delay turns on the high voltage MOSFET after V_{CC} has dropped below 4.5 V.

If the SMPS output is short circuited, the transformer winding, which provides the V_{CC} voltage to the MC33364, will be unable to sustain V_{CC}. The restart delay prevents the high voltage startup transistor within the IC from maintaining the voltage on the V_{CC} pin bootstrap capacitor. After V_{CC} drops below the UVLO threshold in the SMPS, the SMPS switching transistors are held off for the time programmed by the restart delay circuit. In this manner, the SMPS switching transistor is operated at a very low duty cyle, preventing destruction. If the short circuit fault is removed, the power supply system will turn on by itself in a normal startup mode after the restart delay has timed out

Figure 8. Frequency Clamp Circuit



Output Switching Frequency Clamp

In normal operation, the MC33364 operates the flyback transformer primary inductance in the critical mode. That is, the inductor current ramps to a peak value, ramps down to zero, then immediately begins ramping positive again. The peak current is programmed by the current sense resistance value. If the output load is reduced from full load to a standby load or no load condition, the switching frequency can increase to hundreds of kilohertz. Because regulatory agency EMI limits for allowed conducted current decreases as the switching frequency increases beyond 150 kHz, this may be an undesireable operating condition. The Output Switching Frequency Clamp remedies this situation to minimize EMI generated in this operating region. The internal frequency clamp circuit in the MC33364D1 and MC33364D programs a minimum off time, forcing discontinuous mode operation and limiting the operating frequency to less than 126 kHz. The MC33364D2 does NOT contain a frequency clamp circuit. The Output Switching Frequency Clamp function in the MC33364D can be disabled by connecting the FC input, Pin 8, to ground. The clamp frequency can be set externally by sinking or sourcing a current into the pin of up to 100 microamperes.

Output

The IC contains a CMOS output driver specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ±1500 mA peak current with a typical rise and fall time of 50 nS with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull–down resistor. The totem–pole output has been optimized to minimize cross–conduction current during high speed operation.

Design Example

Design an off–line Flyback converter according to the following requirements:

Output Power:	12 W
Output:	6.0 V @ 2 Amperes
Input voltage range:	90 Vac – 270 Vac, 50/60 Hz

The operation for the circuit shown in Figure 9 is as follows: the rectifier bridge D1–D4 and the capacitor C1 convert the ac line voltage to dc. This voltage supplies the primary winding of the transformer T1 and the startup circuit

in U1 through Pin 8. The primary current loop is closed by the transformer's primary winding, the TMOS switch Q1 and the current sense resistor R7. The switch Q1 is driven from Pin 6 of U1 through the resistor R4 and the diode D7. The resistor R4 smooths the switch–on of Q1. The diode D7 ensures a fast switching–off. The resistors R5, R6, diode D6 and capacitor C4 create a clamping network that protects Q1 from spikes on the primary winding. The network consisting of capacitor C3, diode D5 and resistor R1 provides a V_{CC} supply voltage for U1 from the auxiliary winding of the transformer. The resistor R1 makes V_{CC} more stable and resistant to noise. The resistor R2 reduces the current flow through the internal clamping and protection zener diode of the Zero Crossing Detector (ZCD) within U1. C3 is the decoupling capacitor of the supply voltage. The resistor R3 provides bias current for the optoisolator's transistor. The diode D8 and the capacitor C5 rectify and filter the output voltage. The device U2 drives the primary side through the optoisolator to make the output voltage stable. The output voltage information is delivered to U2 by a resistive divider that consists of resistors R10 and R11. The resistor R9 and the capacitors C7, C8 provide frequency compensation of the feedback loop.

Since the critical conduction mode converter is a variable frequency system, the MC33364 has a built–in special block to reduce switching frequency in the no load condition. This block is named the "frequency clamp" block. MC33364 used in the design example has an internal frequency clamp set to 126 kHz. However, optional versions with a disabled or variable frequency clamp are available. The frequency clamp works as follows: the clamp controls the part of the switching cycle when the MOSFET switch is turned off. If this "off–time" (determined by the reset time of the transformer's core) is too short, then the frequency clamp does not allow the switch to turn–on again until the defined frequency clamp time is reached (i.e., the frequency clamp will insert a dead time).

There are several advantages of the MC33364's startup circuit. The startup circuit includes a special high voltage switch that controls the path between the rectified line voltage and the V_{CC} supply capacitor to charge that capacitor by a limited current when the power is applied to the input. After a few switching cycles the IC is supplied from the transformer's auxiliary winding. After V_{CC} reaches the undervoltage lockout threshold value, the startup switch is turned off by the undervoltage and the overvoltage control circuit. Because the power supply can be shorted on the output, causing the auxiliary voltage to be zero, the MC33364 will periodically start its startup block. This mode is named "hiccup mode". During this mode the temperature of the chip rises but remains protected by the thermal shutdown block. During the power supply's normal operation, the high voltage internal MOSFET is turned off, preventing wasted power, and thereby, allowing greater circuit efficiency.

Since a bridge rectifier is used, the resulting minimum and maximum dc input voltages can be calculated:

$$V_{in(min)}dc = \sqrt{2}\,xV_{in(min)}ac = \left(\sqrt{2}\right)(90\ Vac) = 127\ V$$

$$V_{in(\mu ax)}dc = \sqrt{2}\,xV_{in(\mu ax)}ac = \left(\sqrt{2}\right)(270\ Vac) = 382\ V$$

The maximum average input current is:

$$I_{in} = \frac{P_{out}}{\left[nV_{in(min)}\right]} = \frac{12\ W}{[0.8(127\ V)]} = 0.118\ A$$

where n = estimated circuit efficiency.

A TMOS switch with 600 V avalanche breakdown voltage is used. The voltage on the switch's drain consists of the input voltage and the flyback voltage of the transformer's primary winding. There is a ringing on the rising edge's top of the flyback voltage due to the leakage inductance of the transformer. This ringing is clamped by the RCD network. Design this clamped wave for an amplitude of 50 V. Add another 50 V to allow a safety margin for the MOSFET. Then a suitable value of the flyback voltage may be calculated:

$$V_{flbk} = V_{TMOS} - V_{in(max)} - 100\ V =$$
$$600\ V - 382\ V - 100\ V = 118\ V$$

Since this value is very close to the $V_{in(min)}$, set:

$$V_{flbk} = V_{in(min)} = 127\ V$$

The V_{flbk} value of the duty cycle is given by:

$$\partial max = \frac{V_{flbk}}{V_{flbk} + V_{in(min)}} = \frac{127\ V}{[127\ V + 127\ V]} = 0.5$$

The maximum input primary peak current:

$$I_{ppk} = \frac{2\ I_{in}}{[\partial max]} = \frac{0.2(0.118\ A)}{0.5} = 0.472\ A$$

Choose the desired minimum frequency $\mathbf{f_{min}}$ of operation to be **70 kHz**.

After reviewing the core sizing information provided by a core manufacturer, a EE core of size about 20 mm was chosen. Siemens' N67 magnetic material is used, which corresponds to a Philips 3C85 or TDK PC40 material.

The primary inductance value is given by:

$$L_p = \frac{\partial max\ V_{in(min)}}{\left(I_{ppk}\right)\left(f_{min}\right)} = \frac{0.5(127\ V)}{(0.472\ A)(70\ kHz)} = 1.92\ mH$$

The manufacturer recommends for that magnetic core a maximum operating flux density of:

$$B_{max} = 0.2\ T$$

The cross–sectional area A_c of the EF20 core is:

$$A_c = 33.5\ mm^2$$

The operating flux density is given by:

$$B_{max} = \frac{L_p I_{ppk}}{N_p A_c}$$

From this equation the number of turns of the primary winding can be derived:

$$n_p = \frac{L_p I_{ppk}}{B_{max} A_c}$$

The A_L factor is determined by:

$$A_L = \frac{L_p}{n^2_p} = \frac{L_p\left(B_{max}A_c\right)^2}{\left[L_p\left(I_{ppk}\right)^2\right]}$$

$$= \frac{(0.2\ T)\left(33.5\ E{-}6\ m^2\right)^2}{(.00192\ H)(0.472\ A)^2} = 105\ nH$$

From the manufacturer's catalogue recommendation the core with an A_L of 100 nH is selected. The desired number of turns of the primary winding is:

$$n_p = \left(\frac{L_p}{A_L}\right)^{1/2} = \left[\frac{(0.00192\ H)}{(100\ nH)}\right]^{1/2} = 139\ turns$$

The number of turns needed by the 6.0 V secondary is (assuming a Schottky rectifier is used):

$$n_S = \frac{\left(V_S + V_{fwd}\right)(1{-}\partial max)n_p}{\left[\partial max\left(V_{in(min)}\right)\right]}$$

$$= \frac{(6.0\ V + 0.3\ V)(1 - 0.5)139}{\left[0.5(127\ V)\right]} = 7\ turns$$

The auxiliary winding to power the control IC is 16 V and its number of turns is given by:

$$naux = \frac{(V_{aux} + V_{fwd})(1 - \partial max)n_p}{\left[\partial max(V_{in(min)})\right]}$$

$$= \frac{(16\ V + 0.9\ V)(1 - 0.5)139}{[0.5(127\ V)]} = 19\ turns$$

The approximate value of rectifier capacitance needed is:

$$C1 = \frac{t_{off}(I_{in})}{V_{ripple}} = \frac{(5\ m\ sec)(0.118\ A)}{50\ V} = 11.8\ \mu F$$

where the minimum ripple frequency is 2 times the 50 Hz line frequency and t_{off}, the discharge time of C1 during the haversine cycle, is assumed to be half the cycle period.

Because we have a variable frequency system, all the calculations for the value of the output filter capacitors will be done at the lowest frequency, since the ripple voltage will be greatest at this frequency. The approximate equation for the output capacitance value is given by:

$$C5 = \frac{I_{out}}{(f_{min})(V_{rip})} = \frac{2\ A}{(70\ kHz)(0.1\ V)} = 286\ \mu F$$

Determining the value of the current sense resistor (R7), one uses the peak current in the predesign consideration. Since within the IC there is a limitation of the voltage for the current sensing, which is set to 1.2 V, the design of the current sense resistor is simply given by:

$$R7 = \frac{V_{cs}}{I_{ppk}} = \frac{1.2\ V}{0.472\ A} = 2.54\ \Omega \approx 2.2\ \Omega$$

The error amplifier function is provided by a TL431 on the secondary, connected to the primary side via an optoisolator, the MOC8102.

The voltage of the optoisolator collector node sets the peak current flowing through the power switch during each cycle. This pin will be connected to the feedback pin of the MC33364, which will directly set the peak current.

Starting on the secondary side of the power supply, assign the sense current through the voltage–sensing resistor divider to be approximately 0.25 mA. One can immediately calculate the value of the lower and upper resistor:

$$R_{lower} = R11 = \frac{V_{ref}\ (TL431)}{I_{div}} = \frac{2.5\ V}{0.25\ mA} = 10\ k$$

$$R_{upper} = R10 = \frac{V_{out} - V_{ref}(TL431)}{I_{div}}$$

$$= \frac{6.0\ V - 2.5V}{0.25\ mA} = 14\ k$$

The value of the resistor that would provide the bias current through the optoisolator and the TL431 is set by the minimum operating current requirements of the TL431. This currernt is minimum 1.0 mA. Assign the maximum current through the branch to be 5 mA. That makes the bias resistor value equal to:

$$R_{bias} = R_S = \frac{V_{out} - [V_{ref}(TL431) + V_{LED}]}{I_{LED}}$$

$$= \frac{6.0\ V - [2.5V + 1.4V]}{5.0\ mA} = 420\ \Omega \approx 430\ \Omega$$

The MOC8102 has a typical current transfer ratio (CTR) of 100% with 25% tolerance. When the TL431 is full–on, 5 mA will be drawn from the transistor within the MOC8102. The transistor should be in saturated state at that time, so its collector resistor must be

$$R_{collector} = \frac{V_{ref} - V_{sat}}{I_{LED}} = \frac{5.0\ V - 0.3\ V}{5.0\ mA} = 940\ \Omega$$

Since a resistor of 5.0 k is internally connected from the reference voltage to the feedback pin of the MC33364, the external resistor can have a higher value

$$R_{ext} = R3 = \frac{(R_{int})(R_{collector})}{(R_{int}) - (R_{collector})} = \frac{(5.0\ k)(940)}{5.0\ k - 940}$$

$$= 1157\ \Omega \approx 1200\ \Omega$$

This completes the design of the voltage feedback circuit.

In no load condition there is only a current flowing through the optoisolator diode and the voltage sense divider on the secondary side.

The load at that condition is given by:

$$R_{noload} = \frac{V_{out}}{(I_{LED} + I_{div})}$$

$$= \frac{6.0\ V}{(5.0\ mA + 0.25\ mA)} = 1143\ \Omega$$

The output filter pole at no load is:

$$f_{pn} = \frac{1}{(\ 2\pi\ R_{noload}\ C_{out}\ )}$$

$$= \frac{1}{(2\pi)(1143)(300\ \mu F)} = 0.46\ Hz$$

In heavy load condition the I_{LED} and I_{div} is negligible. The heavy load resistance is given by:

$$R_{heavy} = \frac{V_{out}}{I_{out}} = \frac{6.0\ V}{2.0\ A} = 3.0\ \Omega$$

The output filter pole at heavy load of this output is

$$f_{pn} = \frac{1}{(2\pi\ R_{heavy} C_{out})} = \frac{1}{(2\pi)(3)(300\ \mu F)} = 177\ Hz$$

The gain exhibited by the open loop power supply at the high input voltage will be:

$$A = \frac{\left(V_{in\ max} - V_{out}\right)^2 Ns}{\left((V_{in\ max})(V_{error})(Np)\right)} = \frac{(382\ V - 6.0\ V)^2 (7)}{(382\ V)(1.2\ V)(139)}$$

$$= 15.53 = 23.82\ dB$$

The maximum recommended bandwidth is approximately:

$$f_c = \frac{fs\,min}{5} = \frac{70\ kHz}{5} = 14\ kHz$$

The gain needed by the error amplifier to achieve this bandwidth is calculated at the rated load because that yields the bandwidth condition, which is:

$$Gc = 20\ \log\left(\frac{f_c}{f_{ph}}\right) - A = 20\ \log\left(\frac{14\ kHz}{177}\right) - 23.82\ dB$$

$$= 14.14\ dB$$

The gain in absolute terms is:

$$A_c = 10^{(Gc/20)} = 10^{(14.14/20)} = 51$$

Now the compensation circuit elements can be calculated. The output resistance of the voltage sense divider is given by the parallel combination of resistors in the divider:

$$R_{in} = R_{upper} \parallel R_{lower} = 10\ k \parallel 14\ k = 5833\ \Omega$$

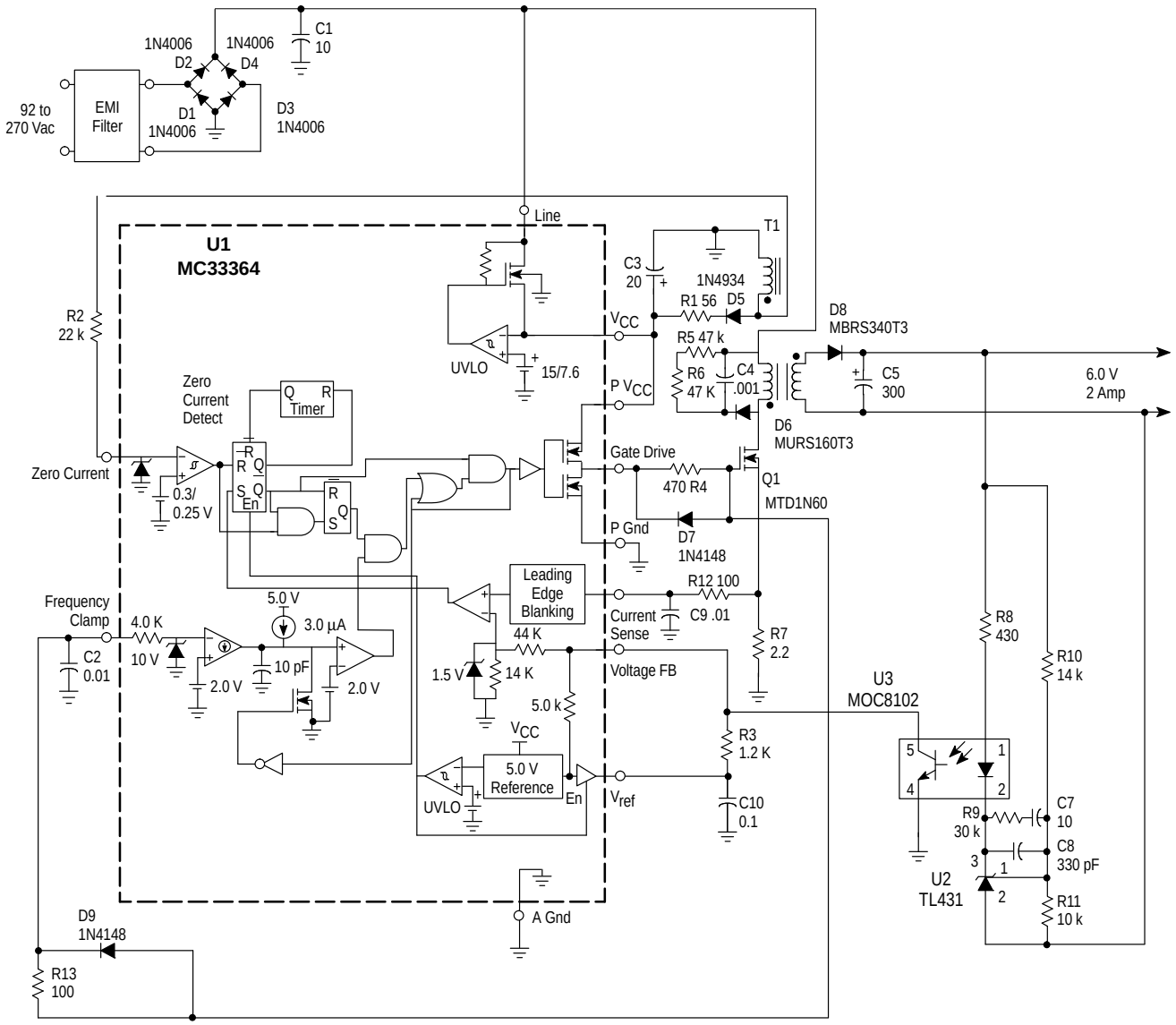
$$R9 = (Ac)\ (R_{in}) = 29.75\ k \approx 30\ k$$

$$C8 = \frac{1}{\left[2\pi\ (A_c)\ (R_{in})\ (f_c)\right]} = 382\ pF \approx 390\ pF$$

The compensation zero must be placed at or below the light load filter pole:

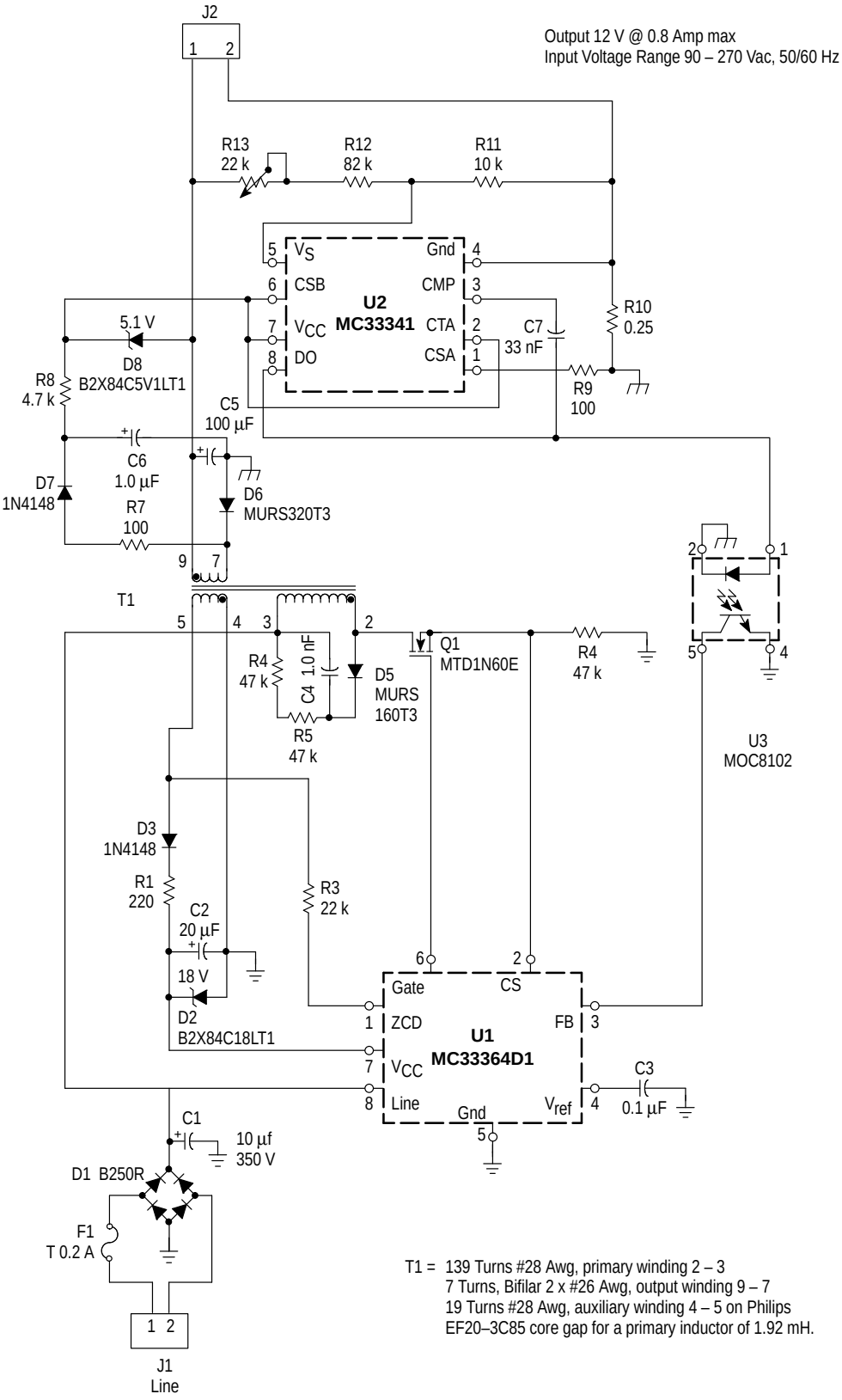
$$C7 = \frac{1}{\left[2\pi\ (R9)\ (f_{pn})\right]} = 11.63\ \mu F \approx 10\ \mu F$$

Figure 9. 12 W Power Supply



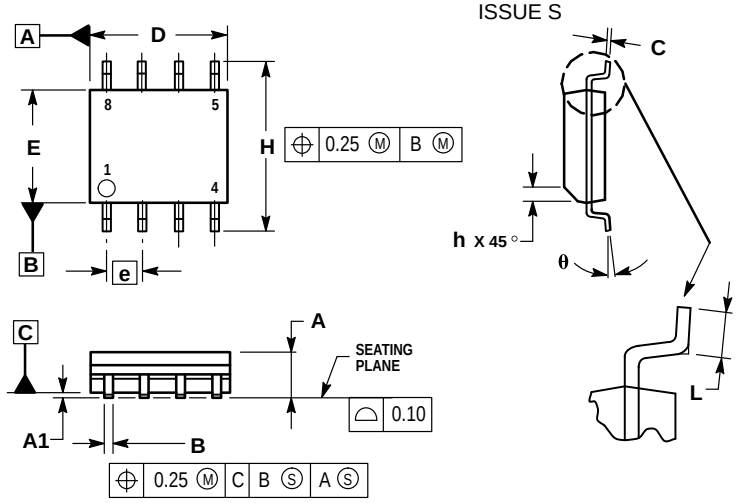
Line Regulation I_O = 930 mA	V_{in} = 90 to 270 Vac	Δ = 78 mV or ±6.5%
Line Regulation V_{in} = 115 Vrms	I_O = 110 to 1100 mA	Δ = 103 mV or ±8.6%
Output Ripple	V_{in} = 115 Vac, I_O = 1100 mA	600 mVpp
Efficiency	V_{in} = 115 Vac, I_O = 1100 mA	72.9%

Figure 10. Universal Input Battery Charger



OUTLINE DIMENSIONS

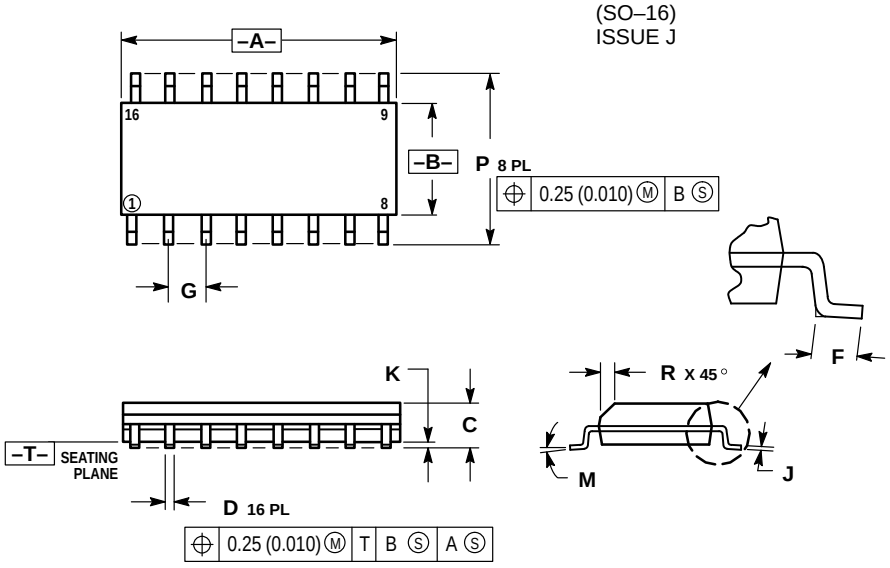
D1, D2 SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE S



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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