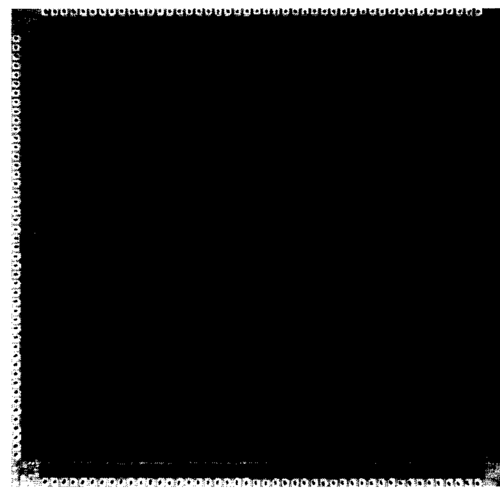
LSI LOGIC

LR3220
Read-Write Buffer
Preliminary

Introduction

The LR3220 Read-Write Buffer enhances the performance of MIPS architecture-based systems by buffering write and read operations. Using the Read-Write Buffer, the system can perform memory write operations at the cycle rate of the processor, instead of stalling the processor to write data to memory. On memory read operations, the system uses the Read-Write Buffer to pass the read address to main memory, and latch the read data from memory. The Read-Write Buffer generates parity, and then passes the data and parity to the processor. A single LR3220 provides six-deep write buffering and one level of read buffering for 32 bits of address and 32 bits of data. It operates at the system clock rate, and is available at 25 and 33.33 MHz to support the requirements of LR3000-based systems.



LR3220 Die

Features

- Combines the functionality of four LR3020 Write Buffers
- Minimizes additional loading on the address and data buses with on-chip data and address latches for read operations
- Supports big endian and little endian byte-order addressing
- Uses byte mask outputs to ease system design
- Performs block-mode conflict detection for block sizes of eight words or less
- Offers separate enable signals for all address and data buses
- Supports fast page-mode writes for 1MBit DRAM-based memory implementations
- Provides six-deep write buffering of data and addresses
- Supports two operating modes:
  1) LR3000 mode
     - compatible with the LR3000's staggered Address and Tag bus timing - decodes AccTyp [1:0] and AdrLo [1:0] inputs for byte ordering
  2) Harvard mode
     - uses synchronous address latching on the rising edge of the clock
     - uses byte mask inputs for byte ordering
- Offered in both 180-pin CPGA and compact 184-pin PQFP packages

Overview of Operation

Figure 1 shows an LR3220 in an LR3000-based system. Data and address transfers between the processor and the Read-Write Buffer occur synchronously at the cycle rate of the processor. The Read-Write Buffer and main memory controller exchange handshake signals to coordinate the transfer of data between the LR3220 and main memory. Refer to the LR3220/CPU Interface and LR3220/Main Memory Interface sections, below, for more specific information on these interfaces.

Figure 2 presents a functional block diagram of the LR3220. For write operations, the LR3220 latches the write address, data, and byte mask information from the processor, and decodes the byte mask bits if appropriate. The Read-Write Buffer FIFO has six ranks, to hold up to six address/data pairs while it waits to pass the data to main memory. For read operations, the Read-Write Buffer passes the read address from the processor to the memory controller, latches the read data from memory,

Overview of Operation (Continued)

generates parity, and passes the data and parity to the processor. Refer to the discussions on Modes of Operation, Conflict Resolution, Write Timing, and Read Timing, below, for more details on read and write operations.

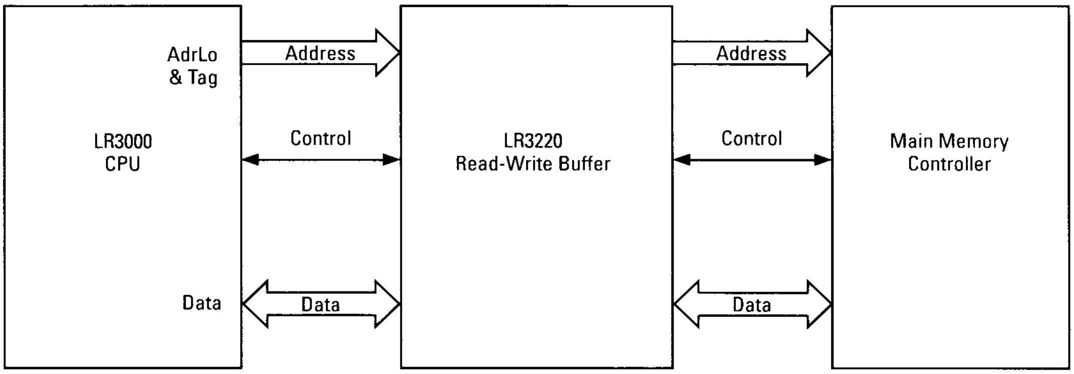


Figure 1. The LR3220 in an LR3000-based System

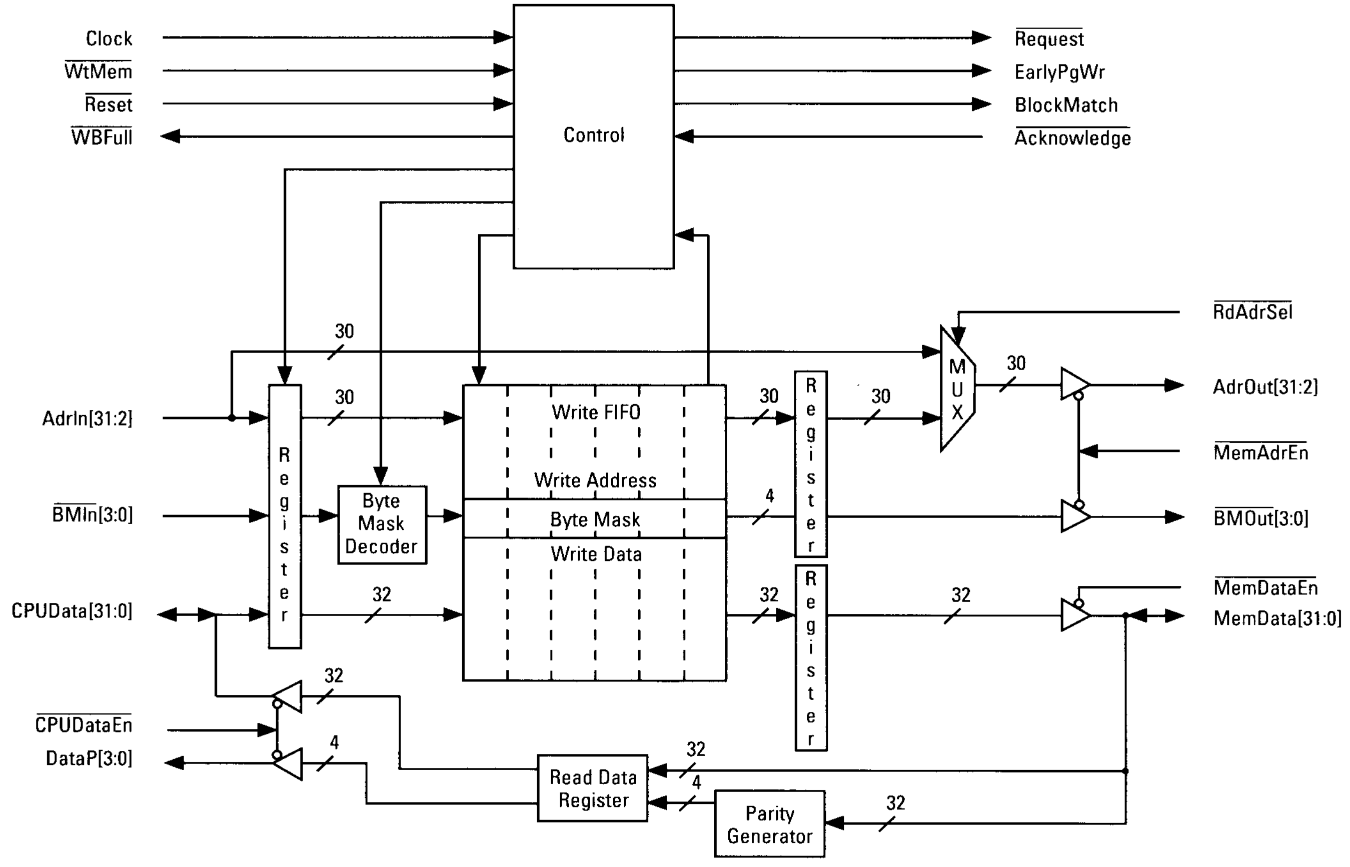


Figure 2. The LR3220 Functional Block Diagram

Modes of Operation

The LR3220 supports two operating modes, LR3000 mode and Harvard mode, selectable at reset. The modes differ in two ways: processor interface timing and byte mask bit interpretation, as explained below. Note that the selected mode only effects transfers between the LR3220 and the processor during write operations. Read transfers, and transfers between the LR3220 and main memory, are identical in both modes.

With regard to processor interface timing, in LR3000 mode the LR3220 latches AdrIn[15:2] and BMIn[1:0] into the input staging register on the falling edge of Clock, and AdrIn[31:16], BMIn[3:2], and CPUData on the rising edge of Clock, to correspond with the staggered timing on the LR3000's AdrLo, Tag, AccTyp, and Data buses. In Harvard mode, the Read-Write Buffer latches the AdrIn, BMIn, and CPUData buses on the rising edge of the Clock.

For byte mask bit interpretation, in LR3000 mode the Read-Write Buffer accepts AdrLo[1:0] and AccTyp[1:0] from the LR3000 on the byte mask input lines, BMIn[3:0]. The LR3220 then combines these bits with the appropriate endian byte ordering (big or little) determined during reset, translates them into the byte mask output bits, and stores them with the write data in the buffer ranks. In Harvard mode, the LR3220 stores BMIn[3:0] unmodified in the ranks, for use as the byte mask output bits. A later section of this data sheet, "Resetting the LR3220", discusses how to define the operating mode at reset time.

Pin Description

This section describes the LR3220 interface signals.

Clock

This signal from the processor synchronizes data transfers. In LR3000 mode, where Clock is an inverted version of the LR3000's SysOut signal, the Read-Write Buffer uses the trailing edge of the Clock to latch the contents of the AdrLo bus, and uses the leading edge to latch the contents of the Data and Tag buses. In Harvard mode, the leading edge of the Clock must latch the address, byte mask bits, and data. In both modes, the LR3220 uses the leading edge of Clock to latch data during memory read cycles.

CPUData[31:0]

These 32 bidirectional data lines connect the processor's data bus with the Read-Write Buffer.

DataP[3:0]

The LR3220 generates these four parity bits on read operations. In LR3000-based systems, these lines connect directly to the LR3000's DataP[3:0] signals. Note that the Read-Write Buffer does not store the parity; it generates it for read operations and ignores it on write operations.

AdrIn[31:2]

These 30 signals are the Read-Write Buffer's address inputs. In LR3000-based systems, the LR3000's AdrLo and Tag buses provide the LR3220 AdrIn[31:2] input signals.

BMIn[3:0]

The byte mask input signals define the byte ordering for the input data. In LR3000 mode, the LR3000's AdrLo[1:0] and AccTyp[1:0] outputs provide the byte-mask input, and the LR3220 decodes these signals and stores them as the byte mask. In Harvard mode, the Read-Write Buffer simply stores the byte mask inputs.

WtMem

The processor should assert this input whenever the processor performs a store operation. In LR3000-based systems, WtMem connects to the LR3000's MemWr output.

Request

When the LR3220 has an address/data pair available for a memory write, it asserts this signal to request a write operation to main memory. In an LR3000-based system, Request may also connect to the CpCond0 input of the LR3000. Because the LR3220 asserts Request only when it contains a valid address/data pair, system software can use Request to determine whether a previous write operation, for example a write to an I/O device, is complete before initiating a read to that device.

WBFull

The LR3220 asserts this signal when it cannot accept any more data; that is, when all six address/data registers in the buffer are occupied. If a processor attempts a write when WBFull is asserted, the LR3220 ignores it. For LR3000-based systems, WBFull connects to WrBusy. If the LR3000 needs to store data while WBFull is asserted, it performs a write busy stall until WBFull is deasserted.

AdrOut[31:2]

These 30 address lines are output from the LR3220 to the memory system address bus.

Pin Description (Continued)

MemData[31:0]
These 32 bidirectional data lines connect the LR3220 to the memory system data bus.

BMOut[3:0]
These byte mask output signals identify the valid data bytes for the memory system during memory write operations.

MemAdrEn
The memory system asserts this input to enable the Read-Write Buffer's AdrOut and BMOut bus outputs.

MemDataEn
The memory system asserts this input to enable the Read-Write Buffer's MemData bus outputs.

CPUDataEn
The processor uses this input to control the LR3220's CPUData and DataP buses. When the processor asserts this signal, the LR3220 sends read data and the generated parity to the processor. In LR3000-based systems, CPUDataEn connects to the LR3000's XEn signal.

RdAdrSel
This input selects between the read address and the current write address. When the main memory controller asserts RdAdrSel, the read address on the processor's address bus, which is available at the AdrIn[31:2] inputs of the LR3220, becomes available on the LR3220 AdrOut bus. When the main memory controller deasserts RdAdrSel, the current write address becomes available on AdrOut. In either case, the memory system must assert MemAdrEn to enable the AdrOut bus.

Acknowledge
The main memory system asserts this signal when it has captured the data presented by the LR3220. The LR3220 also uses this signal during reset to determine the operating mode of the Read-Write Buffer: big or little endian LR3000 mode, or Harvard mode, as illustrated in the reset timing diagram of Figure 18.

EarlyPgWr
For systems with a 1MBit DRAM-based memory implementation, this output signals to the memory controller that the next write operation is to the same memory page as the current write. To check the page address, the LR3220 compares the FIFO's next-write-address bits 31 through 12 with the current-write-address bits 31 through 12. If no write is currently active, EarlyPgWr signals whether or not a page write will occur during the next write cycle, regardless of how long ago the previous write occurred. EarlyPgWr is undefined during the cycle immediately preceding the first write operation after a reset.

BlockMatch
This output signals to the memory controller that the processor has requested a read operation at a memory location for which a write operation is pending. The LR3220 asserts this output when address input bits AdrIn[31:5] match address bits 31 through 5 of any valid address/data pair in the Read-Write Buffer.

Reset
This signal initializes the Read-Write Buffer to a known state and clears the contents of all of its registers.

LR3220/CPU Interface

Figure 3 illustrates the interface between the LR3000 CPU and the LR3220. A single LR3220 implements the full 32-bit, buffered interface. The AdrLo bus and Tag bus bits from the processor combine to form the 32-bit physical address (AdrIn[31:2] and BMIn[1:0]) for the LR3220. Thirty-two bits of data and two access type bits from the processor become the CPUData[31:0] and BMIn[3:2] inputs to the LR3220. On write operations, the LR3220 does not store or pass to main memory the processor's parity bits. On read operations, however, the Read-Write Buffer generates parity and passes it on to the processor.

Later sections in this datasheet provide an overview of the write timing for both the LR3000 and Harvard operating modes and a discussion of the input byte mask decoding for LR3000 mode.

In LR3000 mode, the LR3220 latches AdrLo[15:0], the 16 low-order address bits from the processor, on the trailing edge of the Clock signal. The 16 high-order address bits (Tag[31:16]), the data bits (D[31:0]), and the access type bits (AccTyp[1:0]) are latched on the rising edge of the Clock. AdrLo[1:0] and AccTyp[1:0] from the LR3000 are input on the BMIn[3:0] lines and are decoded by the LR3220 as defined in Table 1. This table shows how the byte masks are decoded, based both on these inputs and on the endian byte ordering specified at reset time.

LR3220/CPU Interface (Continued)

In Harvard mode, the LR3220 latches the complete AdrIn bus on the rising edge of Clock, along with the data and byte mask signals. The byte mask inputs are not decoded, but they indicate which bytes are valid. The LR3220 stores the BMIn[3:0] inputs with the address/data pairs, and then passes them to memory during the write operation.

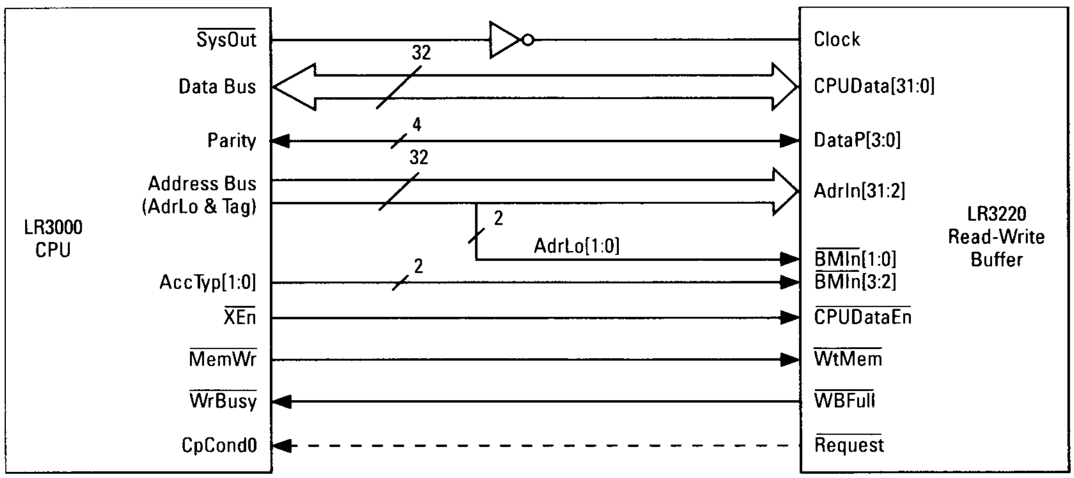


Figure 3. LR3000 to LR3220 Interface

Table 1. Byte Mask Decoding in LR3000 Mode

Byte Mask Inputs				Byte Mask Outputs							
3	2	1	0	3	2	1	0	3	2	1	0
(AccTyp[1:0])		(AdrLo[1:0])		(Big-Endian)[1] 31 … 0				(Little-Endian)[1] 31 … 0			
1 (word)	1	0	0	0	1	2	3	3	2	1	0
1	0	0	0	0	1	2	–	–	2	1	0
(tri-byte)		0	1	–	1	2	3	3	2	1	–
0	1	0	0	0	1	–	–	–	–	1	0
(halfword)		1	0	–	–	2	3	3	2	–	–
0	0	0	0	0	–	–	–	–	–	–	0
(byte)		0	1	–	1	–	–	–	–	1	–
		1	0	–	–	2	–	–	2	–	–
		1	1	–	–	–	3	3	–	–	–

Notes:
1. Determined at reset.
2. [shaded box] – Indicates $\overline{\text{BMOut}}$ asserted (LOW).

LR3220/Main Memory Interface

Figure 4 shows the signals which comprise the LR3220 interface to main memory. The interface is essentially decoupled from the LR3220/processor interface and is identical in both LR3000 and Harvard modes. The handshaking signals between the LR3220 and main memory have no direct connection with the LR3220/processor interface.

The byte mask outputs, $\overline{\text{BMOut}}$[3:0], indicate which bytes of the 32-bit MemData bus are involved in the current transfer, to simplify external hardware design. Specifically, they indicate whether the transfer is a byte, half-word, tri-byte, or word transfer. The byte mask signals indicate valid data as follows:

$\overline{\text{BMOut3}}$ applies to MemData[31:24]
$\overline{\text{BMOut2}}$ applies to MemData[23:16]
$\overline{\text{BMOut1}}$ applies to MemData[15:8]
$\overline{\text{BMOut0}}$ applies to MemData[7:0]

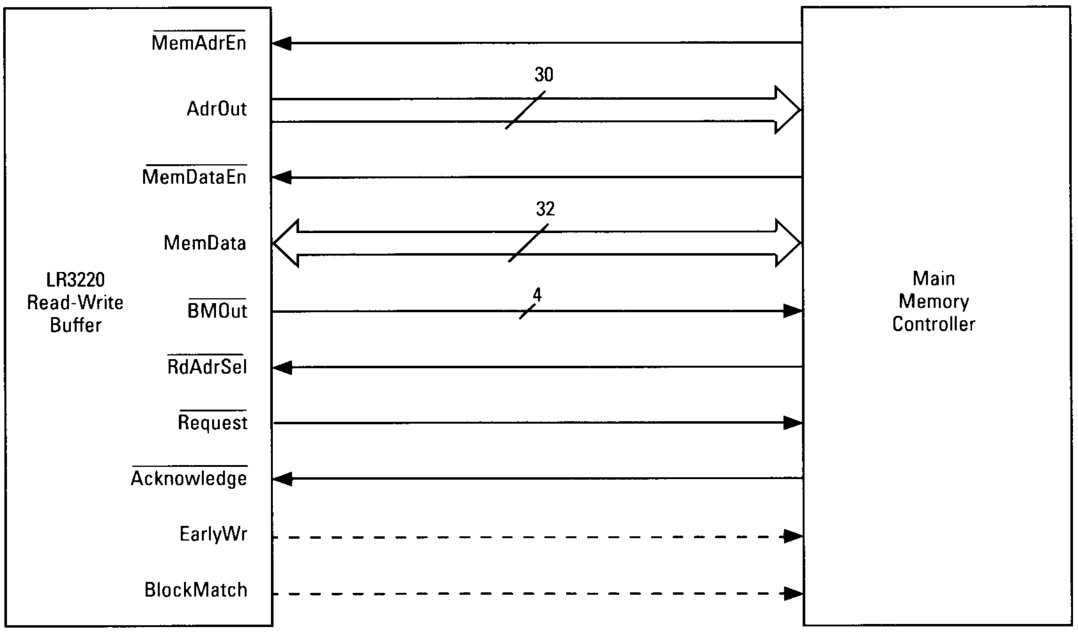


Figure 4. Main Memory to LR3220 Interface

Conflict Resolution

A conflict occurs when the processor requests a memory read operation from a memory location for which a write is pending; completing the read operation prior to the write would result in stale data being returned to the processor.

When the processor puts an address on the system address bus, the LR3220 checks for potential conflicts by comparing the 27 high-order address bits from the processor, available at AdrIn[31:5], with the corresponding address bits of the address/data pairs currently stored in the ranks. If these high-order address bits match, then the two addresses are aligned within the same eight-word block in memory and the LR3220 asserts BlockMatch to signal the potential conflict to the memory controller. If the address bits do not match, then there is no conflict.

When it detects a conflict, the memory controller should hold off the read operation until it has written the conflicting data to memory and the LR3220 has deasserted BlockMatch; then it can complete the memory read operation. Because the LR3220 performs address matching on eight-word-block boundaries, systems which support multiple-word transfers can use BlockMatch to ensure that memory reads of up to eight-word blocks do not result in stale data being returned to the processor. Note that although the LR3220 asserts BlockMatch whenever an address match occurs, the memory controller should only sample BlockMatch during read operations to detect conflicts; no conflicts occur on write operations.

Write Timing

Transfers between the processor and the buffer occur synchronously at the cycle rate of the processor. As mentioned previously, in LR3000 mode the LR3220 uses the inverted SysOut signal from the LR3000 as the Clock to latch the address and data information into the buffer's six address/data ranks.

Figure 5 illustrates the relative write timing in LR3000 mode. On the trailing edge of the Clock, the LR3220 latches the low-order address bits (AdrIn[15:2] and BMIn[1:0]) into its input staging registers. On the rising edge of Clock, the LR3220 latches the high-order address and byte mask bits (AdrIn[31:16] and BMIn[3:2]) and the contents of the data bus into the input staging registers. When the processor asserts WtMem, the assembled address/data pair in the input staging registers is written into one of the LR3220's six address/data ranks.

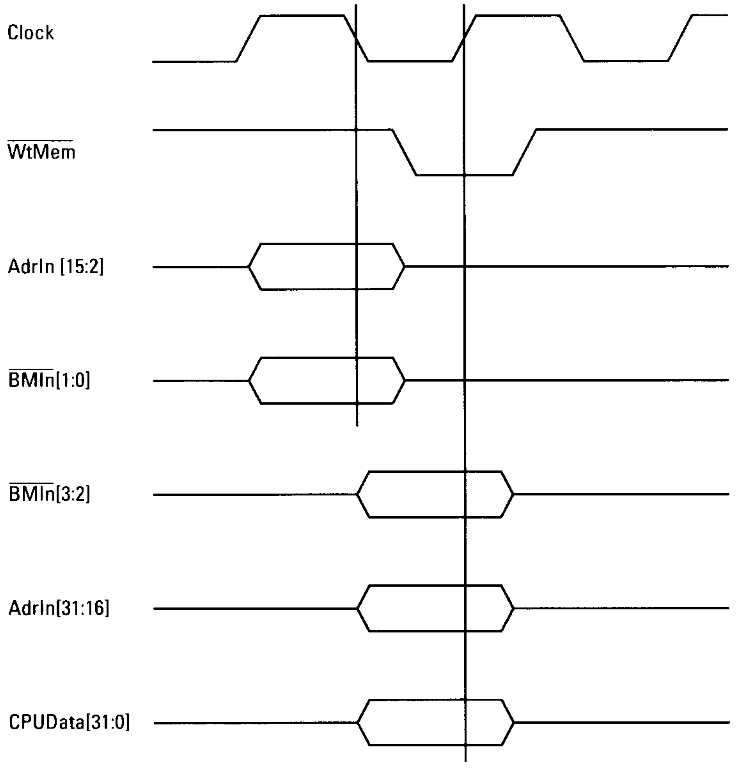


Figure 5. Processor to LR3220 Write Timing in LR3000 Mode

Figure 6 shows the relative write timing in Harvard mode. The LR3220 latches the address, data, and byte mask inputs on the rising edge of the Clock.

Figure 7 illustrates the data transfer timing from the LR3220 to the main memory system; this timing is identical for both the LR3000 and the Harvard operating modes. The sequence is as follows:

1. When the LR3220 has an address/data pair to transfer to the memory system, it asserts the Request signal.

2. When the memory system is ready to handle the address and byte mask, it asserts MemAdrEn to enable the LR3220's address and byte mask outputs onto the system address bus.

3. When the memory system is ready to handle the data, it asserts MemDataEn to enable the LR3220's data bus outputs onto the system data bus.

4. When the memory system no longer requires the Read-Write Buffer's current address and data outputs, it asserts the Acknowledge

Write Timing
(Continued)

signal. The LR3220 responds to this signal by discarding the address/data pair that was just output; that pair's rank is then available for re-use.

5. Next, the memory system can deassert MemAdrEn and MemDataEn to return the Read-Write Buffer's address and data outputs to a three-state condition. In the timing diagram shown in Figure 7, however, the Request signal remains asserted because another address/data write is pending. The memory system then reasserts the MemAdrEn and MemDataEn signals to enable the next address/data pair onto the system buses.

6. When the memory system has accepted the second address/data pair, it again asserts the Acknowledge signal. If the Read-Write Buffer has no other write operations pending, it responds by deasserting the Request signal. Note that the Read-Write Buffer's interface to main memory is not completely asynchronous. The buffer asserts the Request signal sychronous with the rising edge of the Clock, and the Acknowledge signal input from the memory system has a minimum setup and hold time relative to the Clock.

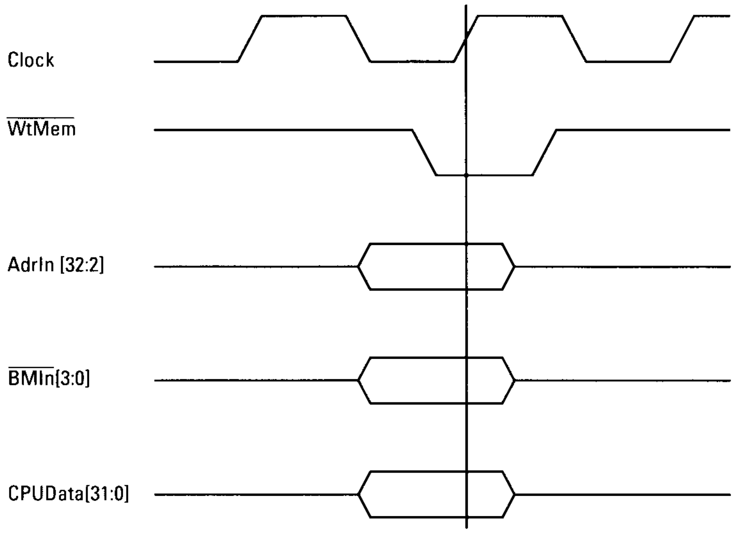


Figure 6. Processor to LR3220 Write Timing in Harvard Mode

Write Timing
(Continued)

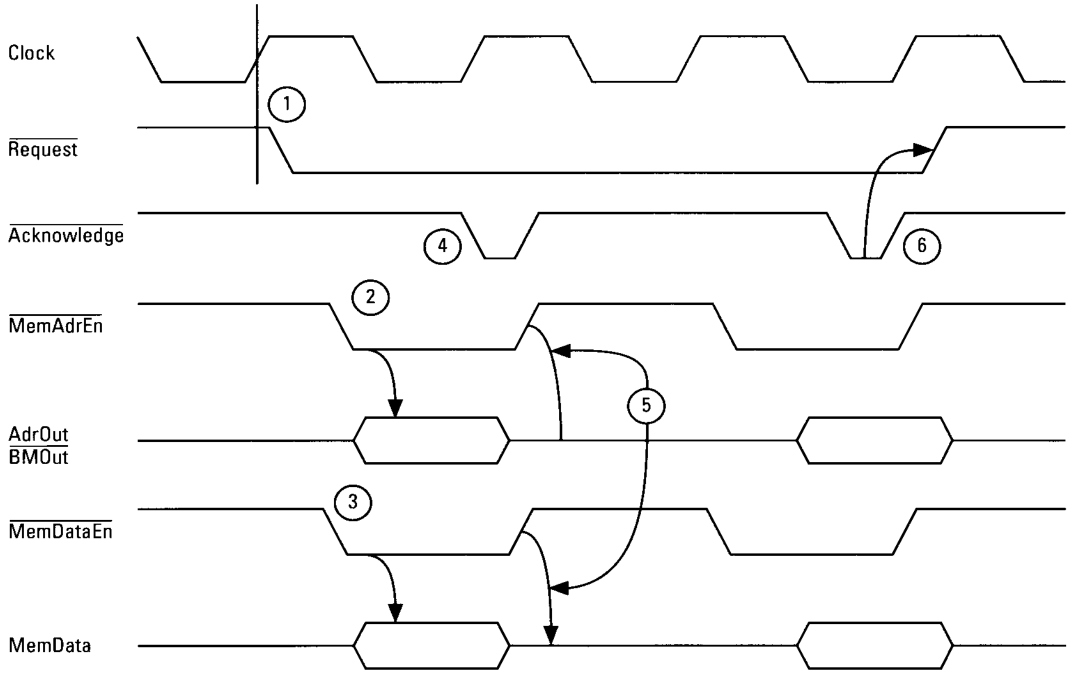


Figure 7. Main Memory Write Timing

Figure 8 illustrates the read address timing for the LR3220. After the processor initiates a read operation, the main memory controller asserts RdAdrSel. This signal transfers the read address, available at the LR3220's AdrIn inputs, to the LR3220's AdrOut bus outputs for access by the memory system. If MemAdrEn is not already asserted, then the main memory controller asserts this signal to enable the read address onto the memory address bus.

The memory system returns the read data on the Read-Write Buffer's MemData bus when MemDataEn is HIGH. The LR3220 generates even parity and strobes all 36 bits of data and parity into its internal read latch on the rising edge of the Clock. The data and parity are then available on the CPUData and DataP buses when the processor asserts the CPUDataEn signal. Note that MemDataEn should go HIGH at least one cycle before CPUDataEn goes LOW. Figure 9 shows the relative timing for read data transfers from the LR3220 to the CPU.

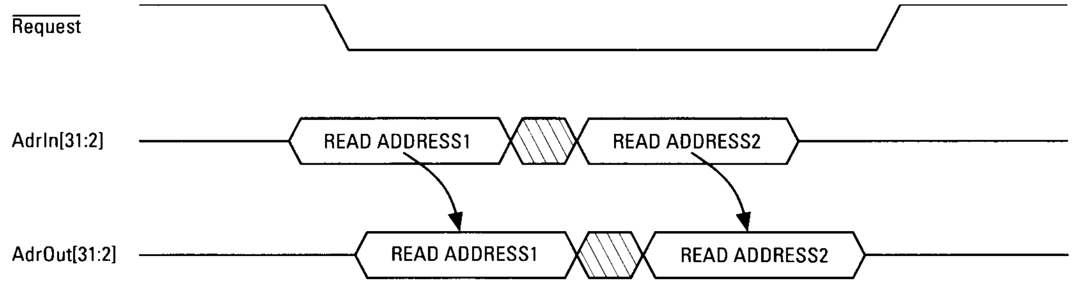


Figure 8. Read Address Timing

Read Timing (Continued)

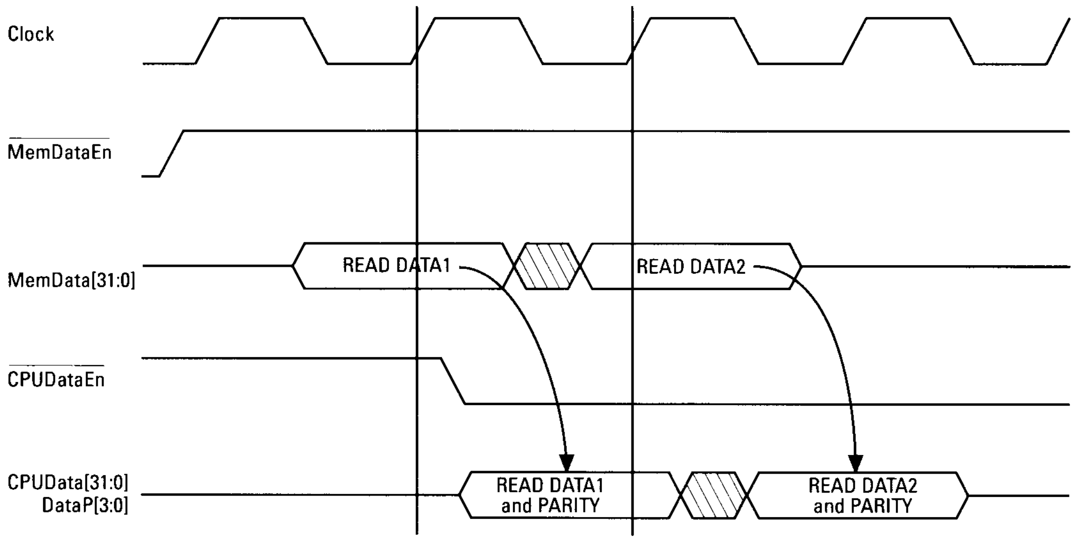


Figure 9. Read Data Timing

Resetting the LR3220

The Reset signal is the initialization input to the LR3220. Reset must be asserted for a minimum of four cycles to guarantee device initialization. The logic levels on the Acknowledge signal during the four cycles prior to the deassertion of Reset select the operating mode for the LR3220: Table 2 summarizes the mode selection. The Z cycle is the last cycle before the deassertion of Reset. W, X, and Y are the fourth, third, and second cycles, respectively, prior to the deassertion of Reset. Note that Acknowledge must be held HIGH during the W and X cycles to ensure compatibility with future versions of the Read-Write Buffer.

Table 2. Reset Mode Selection

Mode	W Cycle	X Cycle	Y Cycle	Z Cycle
LR3000, Little Endian	HIGH	HIGH	HIGH	HIGH
LR3000, Big Endian	HIGH	HIGH	HIGH	LOW
Harvard	HIGH	HIGH	LOW	LOW

Absolute Maximum Rating

Table 3 shows the absolute maximum ratings for the LR3220. Note that stresses beyond those listed in this table may cause permanent damage to the device. The values in Table 3 are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions, below, is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Ratings	Symbol	Value	Units
Supply Voltage	VCC	-0.5 to +6.0	V
Input Voltage	VIN	-0.5 to VCC +0.5	V
Operating Temperature	TA	0 to 70	°C
Storage Temperature	TSTG	-40 to 125	°C

LR3220
Read-Write Buffer
Preliminary

Recommended Operating Conditions

Tables 4 and 5 illustrate the DC and AC electrical characteristics for the LR3220. Figures 10 through 18, which follow, are timing diagrams which illustrate the AC characteristics.

Table 4. DC Electrical Characteristics

Parameter	Description	Test Conditions	25 MHZ		33.33 MHZ		Units
			Min	Max	Min	Max	
VOH	Output High Voltage	VCC = Min, IOH = -4 mA	2.4		2.4		V
VOL	Output Low Voltage	VCC = Min, IOL = 4 mA		0.4		0.4	V
VIH	Input High Voltage	VIN = VDD or GND	2	VCC	2	VCC	V
VIL	Input Low Voltage	VOUT = VDD or GND	-0.5	0.8	-0.5	0.8	V
VIHC	Input High Voltage		3.5		3.5		V
VILC	Input Low Voltage			0.4		0.4	V
CIN	Input Capacitance			8		8	pF
COUT	Output Capacitance			8		8	pF
CINC	Input Capacitance			15		15	pF
COUTC	Output Capacitance			15		15	pF
IIN	Input Leakage		-10	10	-10	10	µA
IOZ	Output Leakage		-10	10	-10	10	µA
ICC	Supply Current			160		170	mA

Note: VIHC, VILC, CINC, and COUTC apply to $\overline{\text{CPUDataEn}}$ and Clock Only.

Recommended Operating Conditions
(Continued)

Table 5. AC Electrical Characteristics

Parameter	Description	25 MHZ Min	25 MHZ Max	33.33 MHZ Min	33.33 MHZ Max	Units
t1	$\overline{\text{WtMem}}$ to Clock rising setup	6		5		ns
t2	$\overline{\text{WtMem}}$ from Clock rising hold	0		0		ns
t3[2]	AdrIn(15:2)/$\overline{\text{BMIn}}$(1:0) to Clock falling setup	5		5		ns
t4[2]	AdrIn(15:2)/$\overline{\text{BMIn}}$(1:0) to Clock falling hold	1.5		1.5		ns
t5[3]	AdrIn(15:2)/$\overline{\text{BMIn}}$(1:0) to Clock rising setup	3		3		ns
t6[3]	AdrIn(15:2)/$\overline{\text{BMIn}}$(1:0) to Clock rising hold	2		2		ns
t7	AdrIn(31:16) to Clock rising setup	4		2		ns
t8	AdrIn(31:16) to Clock rising hold	1.5		1.5		ns
t9	$\overline{\text{BMIn}}$(3:2) to Clock rising setup	2		2		ns
t10	$\overline{\text{BMIn}}$(3:2) to Clock rising hold	4		4		ns
t11	CPUData(31:0) to Clock rising setup	4		2		ns
t12	CPUData(31:0) to Clock rising hold	1.5		1.5		ns
t13	$\overline{\text{Request}}$ valid from Clock rising		14		14	ns
t14	$\overline{\text{Acknowledge}}$ to Clock rising setup	8		7		ns
t15	$\overline{\text{Acknowledge}}$ to Clock rising hold	3		3		ns
t16	AdrOut(31:2) from Clock rising		22		20	ns
t17	$\overline{\text{BMOut}}$(3:0) from Clock rising		19		15	ns
t18	MemData(31:0) from Clock rising		22		20	ns
t19	EarlyPgWr from Clock rising		22		20	ns
t20	$\overline{\text{MemAdrEn}}$ low to AdrOut(31:2)/$\overline{\text{BMOut}}$(3:0) valid		20		18	ns
t21	$\overline{\text{MemAdrEn}}$ high to AdrOut(31:2)/$\overline{\text{BMOut}}$(3:0) 3-state		20		18	ns
t22	$\overline{\text{MemAdrEn}}$ low to MemData(31:0) valid		20		18	ns
t23	$\overline{\text{MemAdrEn}}$ high to MemData(31:0) 3-state		20		18	ns
t24	$\overline{\text{WBFull}}$ active from Clock rising		16		15	ns
t25	$\overline{\text{WBFull}}$ inactive from Clock rising		11.5		11.5	ns
t26	$\overline{\text{RdAdrSel}}$ low to read address valid		20		15	ns
t27	AdrIn(31:2) to AdrOut(31:2) valid		18		12	ns
t28	$\overline{\text{RdAdrSel}}$ high to write address valid		22		15	ns
t29	MemData(31:0) to Clock rising setup		12		8	ns
t30	MemData(31:0) to Clock rising hold		0		0	ns
t31	CPUData(31:0)/DataP(3:0) from Clock rising		11.5		10	ns
t32	$\overline{\text{CPUDataEn}}$ low to CPUData(31:0)/DataP(3:0) valid		11		6	ns
t33	$\overline{\text{CPUDataEn}}$ high to CPUData(31:0)/DataP(3:0) 3-state		7.5		7.5	ns
t34	BlockMatch valid from Clock rising		27		22	ns
t35	Reset to Clock rising setup	10		10		ns
t36	$\overline{\text{Reset}}$ from Clock rising hold	3		3		ns
t37	$\overline{\text{Reset}}$ pulse width	4		4		cycles

Notes:
1. Test conditions were 70°C, VCC = 4.75 V, output loading 50 pF TTL (except CPUData/DataP 65 pF TTL).
2. t3 and t4 are valid in LR3000 mode only.
3. t5 and t6 are valid in Harvard mode only.

Timing Information

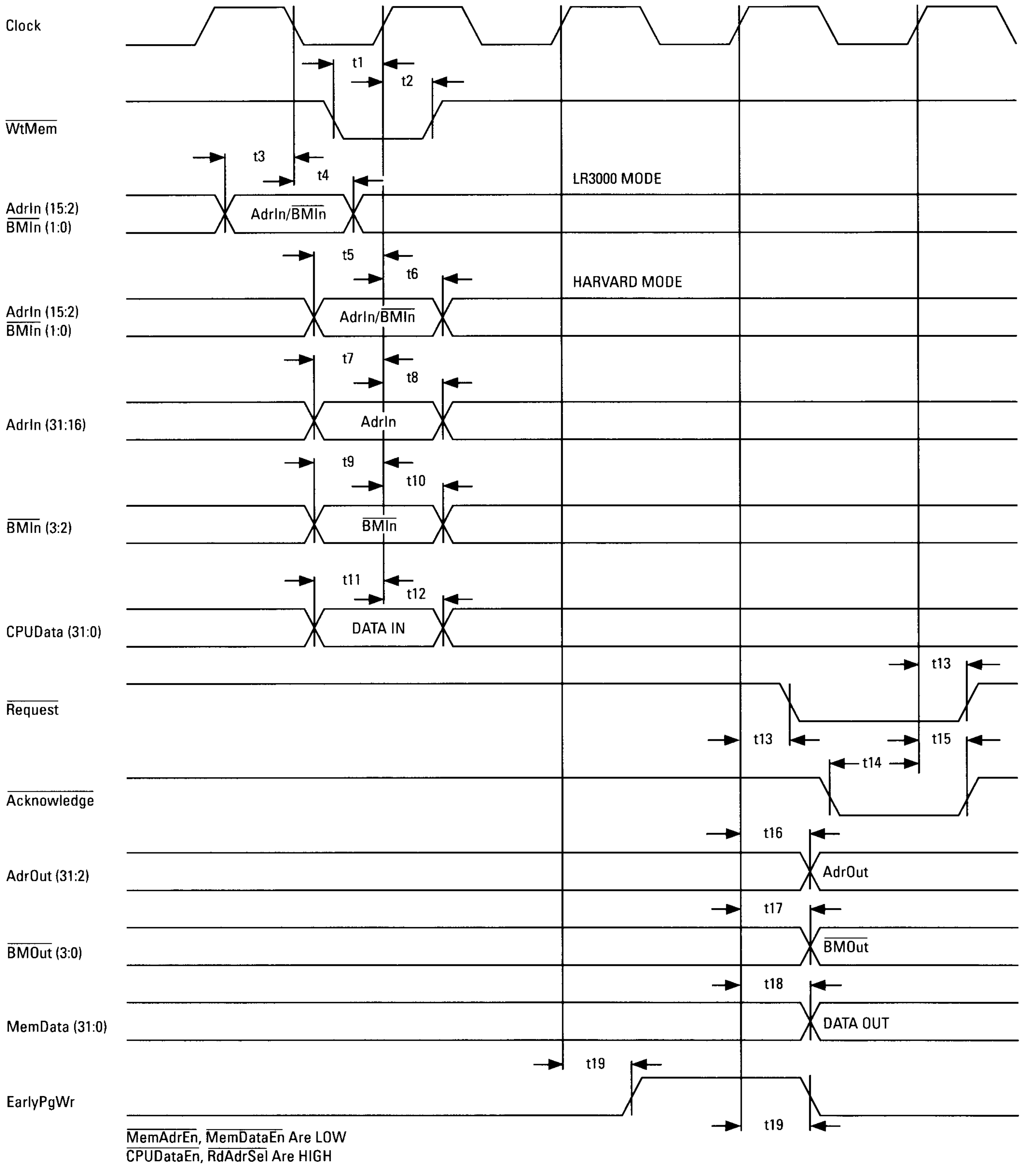


Figure 10. Memory Write Timing with Page Write

Timing Information
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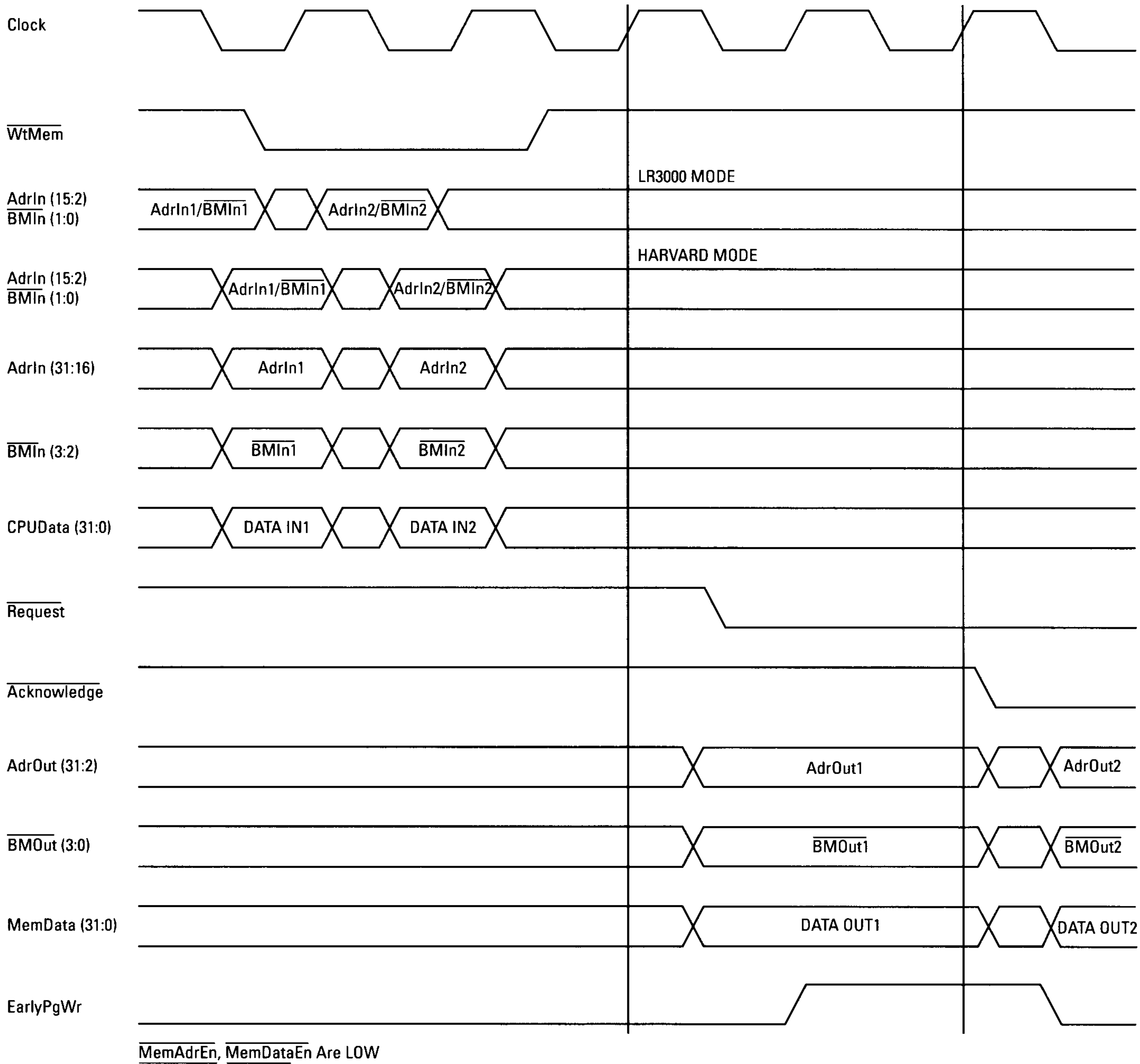


Figure 11. Back-to-Back Writes; Second Write is a Page Write

Timing Information
(Continued)

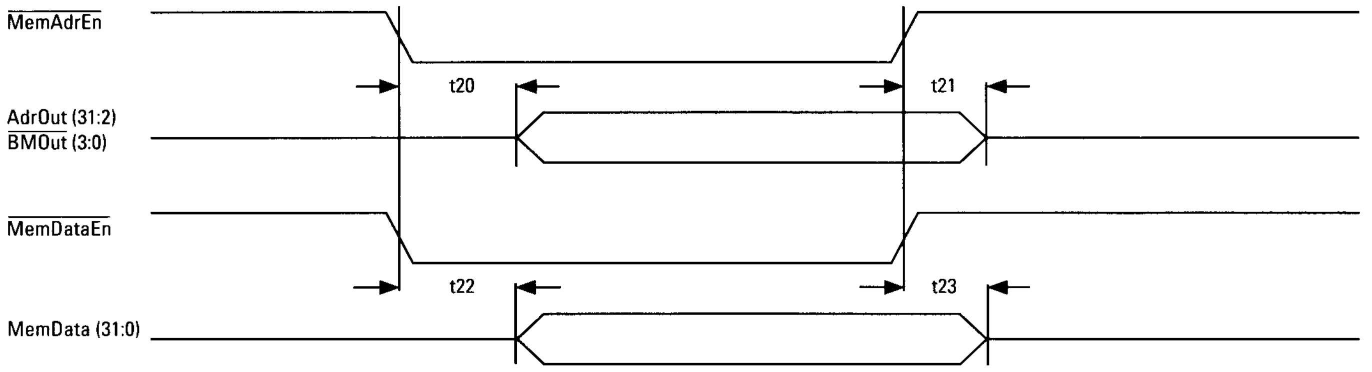


Figure 12. Main Memory 3-State Output Timing

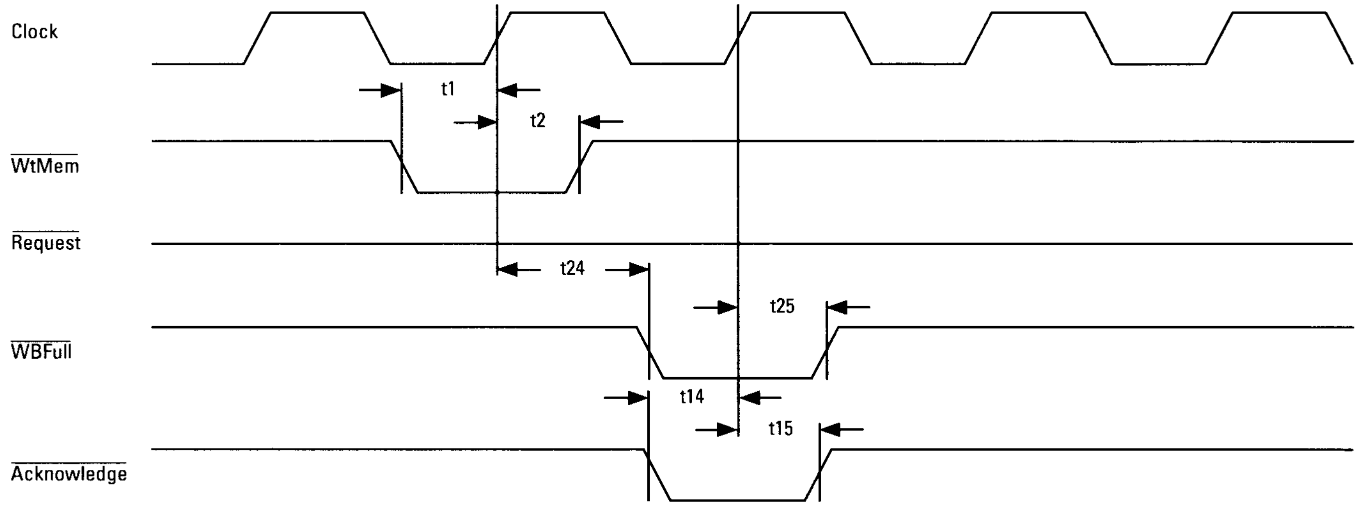


Figure 13. Write Buffer Full Timing

Timing Information
(Continued)

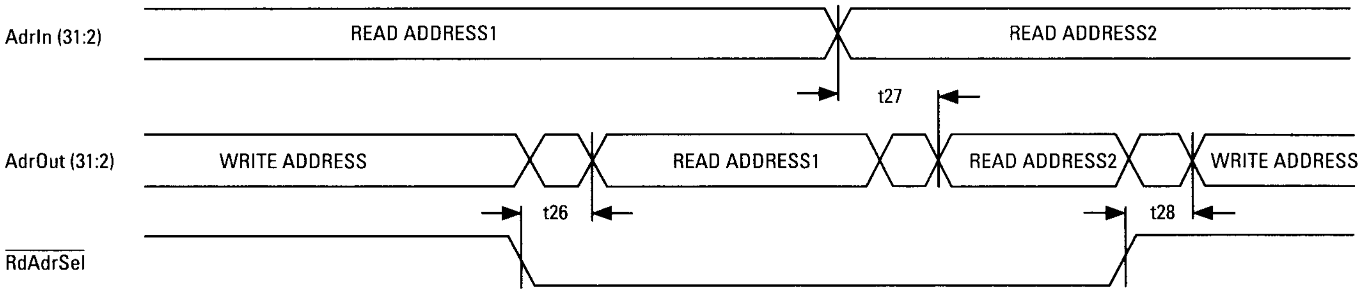


Figure 14. Read Address Output Timing

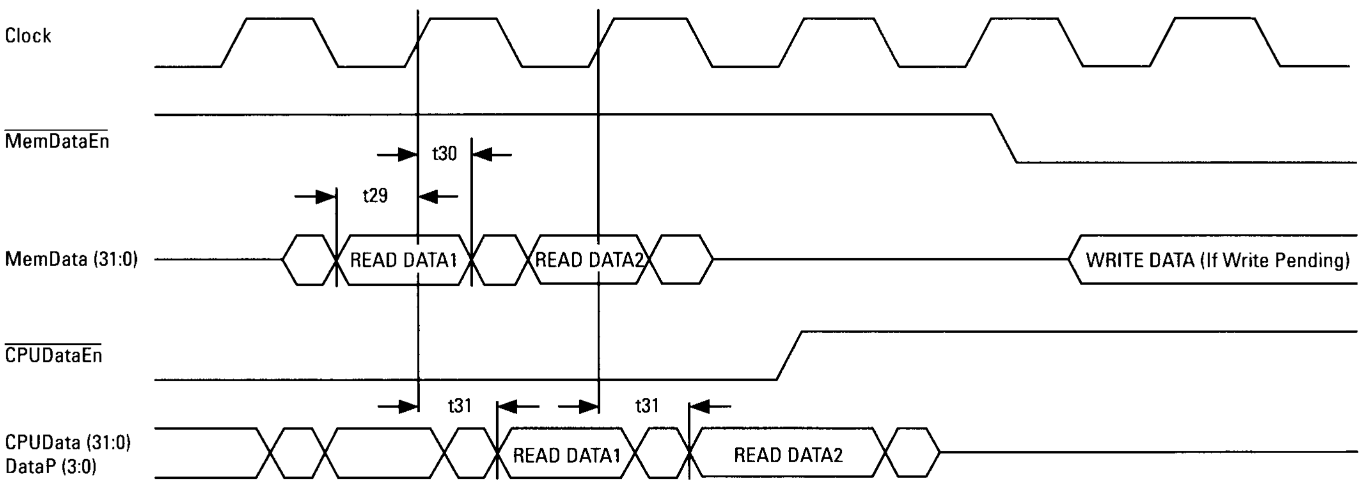


Figure 15. Read Data Input and Output Timing Relative to Clock

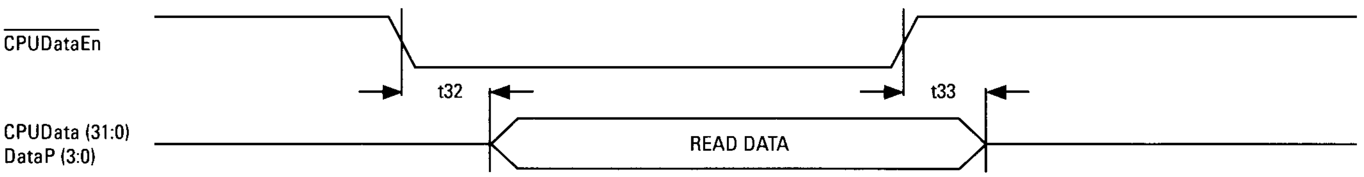


Figure 16. Read Data Output Timing Relative to CPUDataEn

Timing Information
(Continued)

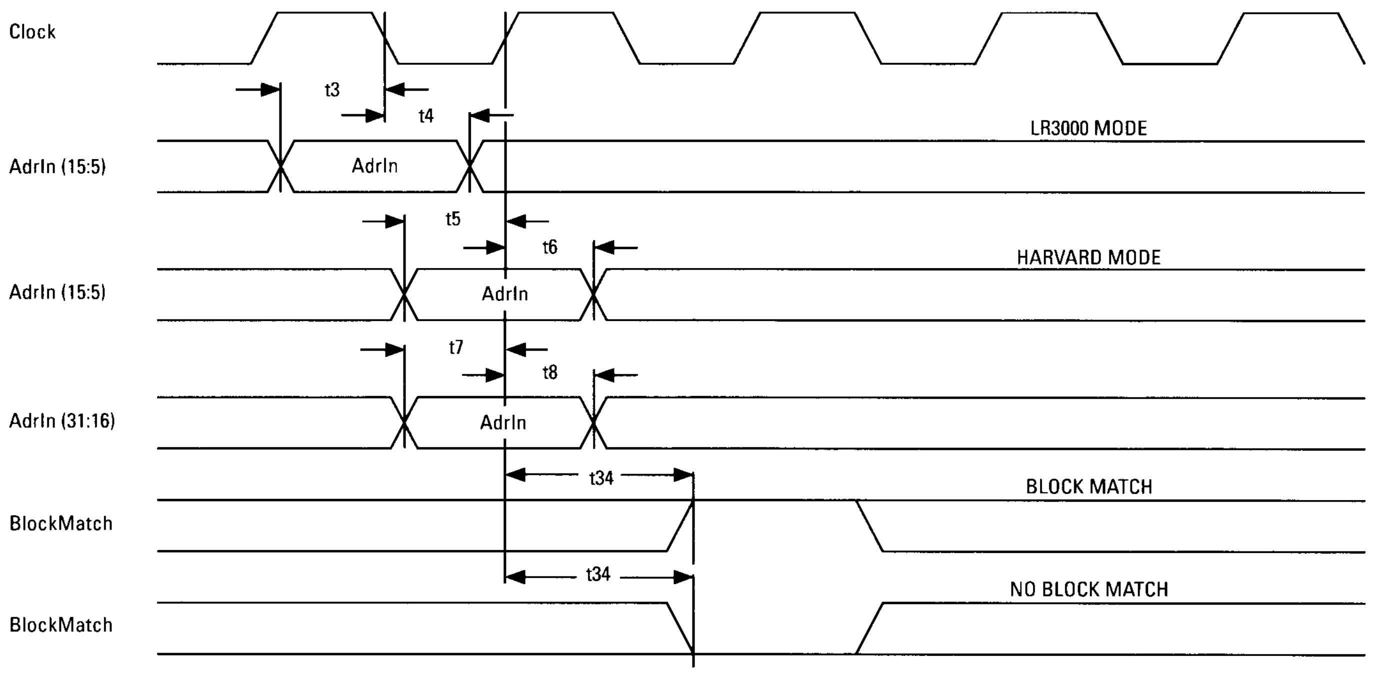


Figure 17. BlockMatch Timing

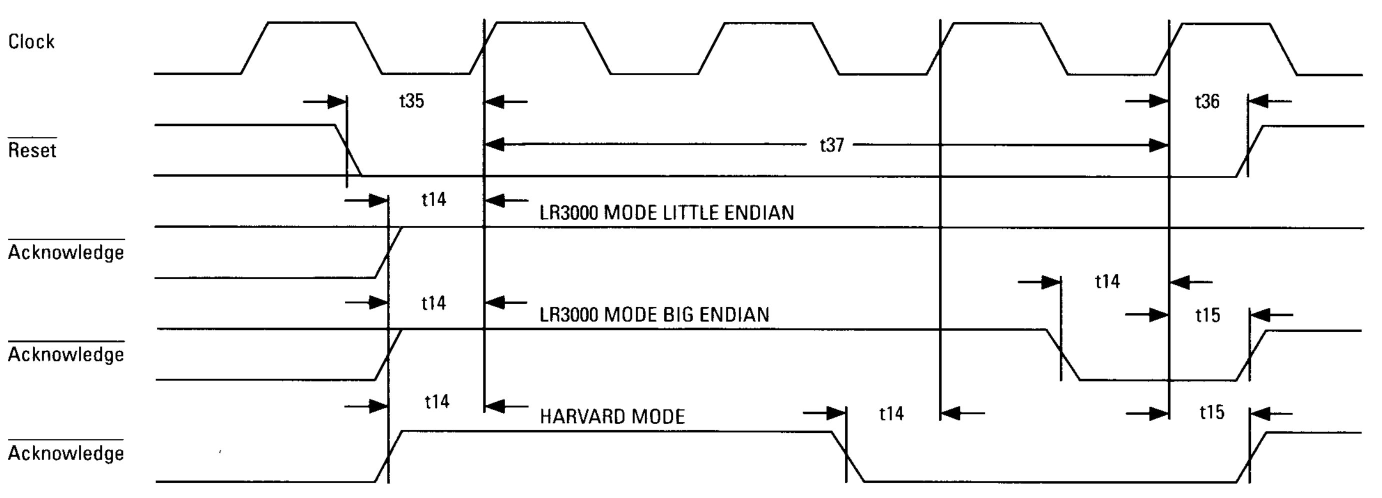


Figure 18. Reset and Configure Timing

Pinout and Package Information

Table 6. 180-Pin Ceramic Pin Grid Array (CPGA) Pin List

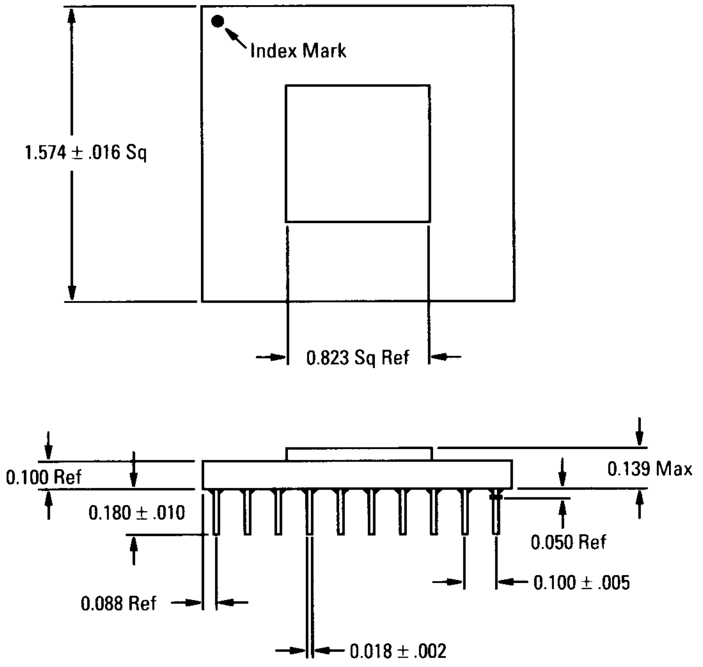
Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
Acknowledge	C11	AdrOut19	L2	CPUData23	E15	RdAdrSel	C7
AdrIn2	C4	AdrOut20	M2	CPUData24	D15	Request	P6
AdrIn3	C3	AdrOut21	N2	CPUData25	C15	Reset	D6
AdrIn4	B8	AdrOut22	P2	CPUData26	B15	WBFull	P7
AdrIn5	B7	AdrOut23	J1	CPUData27	A15	WtMem	C10
AdrIn6	B6	AdrOut24	M1	CPUData28	D11	VCC	A9
AdrIn7	B5	AdrOut25	N1	CPUData29	D10	VCC	B9
AdrIn8	B4	AdrOut26	P1	CPUData30	A13	VCC	D9
AdrIn9	B3	AdrOut27	R1	CPUData31	A12	VCC	E14
AdrIn10	B2	AdrOut28	M5	DataP0	A11	VCC	G12
AdrIn11	A8	AdrOut29	M6	DataP1	A10	VCC	J4
AdrIn12	A7	AdrOut30	M7	DataP2	B12	VCC	K1
AdrIn13	A6	AdrOut31	R2	DataP3	B11	VCC	M10
AdrIn14	A5	BlockMatch	P5	EarlyPgWr	P3	VCC	M14
AdrIn15	A4	BMIn0	C6	MemAdrEn	C8	VCC	P13
AdrIn16	A3	BMIn1	C5	MemDataEn	D5	GND	A14
AdrIn17	A2	BMIn2	C9	MemData0	N4	GND	B10
AdrIn18	A1	BMIn3	D8	MemData1	N5	GND	B13
AdrIn19	B1	BMOut0	R3	MemData2	N6	GND	D3
AdrIn20	C1	BMOut1	R4	MemData3	N7	GND	D4
AdrIn21	D1	BMOut2	R5	MemData4	M8	GND	E8
AdrIn22	E1	BMOut3	R6	MemData5	M9	GND	F13
AdrIn23	F1	Clock	D7	MemData6	M12	GND	F14
AdrIn24	G1	CPUDataEn	C12	MemData7	N8	GND	G15
AdrIn25	H1	CPUData0	K14	MemData8	N9	GND	H5
AdrIn26	C2	CPUData1	J14	MemData9	N10	GND	H11
AdrIn27	D2	CPUData2	H14	MemData10	N11	GND	J2
AdrIn28	E2	CPUData3	M13	MemData11	N12	GND	K13
AdrIn29	F2	CPUData4	L13	MemData12	P8	GND	L1
AdrIn30	G2	CPUData5	J13	MemData13	P9	GND	L8
AdrIn31	H2	CPUData6	H13	MemData14	P10	GND	L14
AdrOut2	E3	CPUData7	L12	MemData15	P11	GND	M11
AdrOut3	F3	CPUData8	K12	MemData16	P12	GND	N13
AdrOut4	G3	CPUData9	J12	MemData17	R8	GND	P14
AdrOut5	H3	CPUData10	H12	MemData18	R9	GND	P15
AdrOut6	E4	CPUData11	F12	MemData19	R10	GND	R7
AdrOut7	F4	CPUData12	E12	MemData20	R11	**reserved**	P4
AdrOut8	G4	CPUData13	D12	MemData21	R12		
AdrOut9	H4	CPUData14	G13	MemData22	R13		
AdrOut10	K4	CPUData15	E13	MemData23	R14		
AdrOut11	L4	CPUData16	D13	MemData24	R15		
AdrOut12	M4	CPUData17	C13	MemData25	N15		
AdrOut13	J3	CPUData18	G14	MemData26	M15		
AdrOut14	K3	CPUData19	D14	MemData27	L15		
AdrOut15	L3	CPUData20	C14	MemData28	K15		
AdrOut16	M3	CPUData21	B14	MemData29	J15		
AdrOut17	N3	CPUData22	F15	MemData30	H15		
AdrOut18	K2			MemData31	N14		

Pinout and Package Information (Continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	AdrIn 18	AdrIn 17	AdrIn 16	AdrIn 15	AdrIn 14	AdrIn 13	AdrIn 12	AdrIn 11	VCC	DataP 1	DataP 0	CPU Data31	CPU Data30	GND	CPU Data27
B	AdrIn 19	AdrIn 10	AdrIn 9	AdrIn 8	AdrIn 7	AdrIn 6	AdrIn 5	AdrIn 4	VCC	GND	DataP 3	DataP 2	GND	CPU Data21	CPU Data26
C	AdrIn 20	AdrIn 26	AdrIn 3	AdrIn 2	BMIn1	BMIn0	RdAdr Sel	Mem AdrEn	BMIn2	WtMem	Ac-knowl-edge	CPU DataEn	CPU Data17	CPU Data20	CPU Data25
D	AdrIn 21	AdrIn 27	GND	GND	Mem DataEn	Reset	Clock	BMIn3	VCC	CPU Data29	CPU Data28	CPU Data13	CPU Data16	CPU Data19	CPU Data24
E	AdrIn 22	AdrIn 28	AdrOut 2	AdrOut 6				GND				CPU Data12	CPU Data15	VCC	CPU Data23
F	AdrIn 23	AdrIn 29	AdrOut 3	AdrOut 7		Extra Pin						CPU Data11	GND	GND	CPU Data22
G	AdrIn 24	AdrIn 30	AdrOut 4	AdrOut 8								VCC	CPU Data14	CPU Data18	GND
H	AdrIn 25	AdrIn 31	AdrOut 5	AdrOut 9	GND			Top View			GND	CPU Data10	CPU Data6	CPU Data2	Mem Data30
J	AdrOut 23	GND	AdrOut 13	VCC								CPU Data9	CPU Data5	CPU Data1	Mem Data29
K	VCC	AdrOut 18	AdrOut 14	AdrOut 10								CPU Data8	GND	CPU Data0	Mem Data28
L	GND	AdrOut 19	AdrOut 15	AdrOut 11				GND				CPU Data7	CPU Data4	GND	Mem Data27
M	AdrOut 24	AdrOut 20	AdrOut 16	AdrOut 12	AdrOut 28	AdrOut 29	AdrOut 30	Mem Data4	Mem Data5	VCC	GND	Mem Data6	CPU Data3	VCC	Mem Data26
N	AdrOut 25	AdrOut 21	AdrOut 17	Mem Data0	Mem Data1	Mem Data2	Mem Data3	Mem Data7	Mem Data8	Mem Data9	Mem Data10	Mem Data11	GND	Mem Data31	Mem Data25
P	AdrOut 26	AdrOut 22	Early PgWr	Re-served	Block Match	Re-quest	WBFull	Mem Data12	Mem Data13	Mem Data14	Mem Data15	Mem Data16	VCC	GND	GND
R	AdrOut 27	AdrOut 31	BMOut 0	BMOut 1	BMOut 2	BMOut 3	GND	Mem Data17	Mem Data18	Mem Data19	Mem Data20	Mem Data21	Mem Data22	Mem Data23	Mem Data24

Figure 19. 180-Pin Ceramic Pin Grid Array (CPGA) Pin Diagram

Pinout and Package Information
(Continued)



Notes:
1. Ceramic packages meet Mil-Std-38510, Revision H.
2. Controlling dimension—inch.

Figure 20. 180-Pin Ceramic Pin Grid Array (CPGA) Mechanical Drawing

LR3220
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Preliminary

Pinout and Package Information
(Continued)

Table 7. 184-Pin Plastic Quad Flat Pack (PQFP) Pin List

Signal Name	Pin Number
Acknowledge	154
AdrIn2	168
AdrIn3	169
AdrIn4	170
AdrIn5	171
AdrIn6	172
AdrIn7	173
AdrIn8	174
AdrIn9	175
AdrIn10	176
AdrIn11	177
AdrIn12	178
AdrIn13	179
AdrIn14	180
AdrIn15	181
AdrIn16	182
AdrIn17	183
AdrIn18	184
AdrIn19	1
AdrIn20	2
AdrIn21	3
AdrIn22	4
AdrIn23	5
AdrIn24	6
AdrIn25	7
AdrIn26	8
AdrIn27	9
AdrIn28	10
AdrIn29	11
AdrIn30	12
AdrIn31	13
AdrOut2	15
AdrOut3	16
AdrOut4	17
AdrOut5	18
AdrOut6	19
AdrOut7	20
AdrOut8	21
AdrOut9	22
AdrOut10	26
AdrOut11	27
AdrOut12	28
AdrOut13	29
AdrOut14	30
AdrOut15	31
AdrOut16	23
AdrOut17	33
AdrOut18	35

Signal Name	Pin Number
AdrOut19	36
AdrOut20	37
AdrOut21	38
AdrOut22	39
AdrOut23	40
AdrOut24	43
AdrOut25	44
AdrOut26	45
AdrOut27	46
AdrOut28	47
AdrOut29	48
AdrOut30	49
AdrOut31	50
BlockMatch	58
BMIn0	166
BMIn1	167
BMIn2	156
BMIn3	157
BMOut0	51
BMOut1	52
BMOut2	53
BMOut3	54
Clock	158
CPUDataEn	153
CPUData0	103
CPUData1	104
CPUData2	105
CPUData3	106
CPUData4	107
CPUData5	109
CPUData6	110
CPUData7	111
CPUData8	112
CPUData9	113
CPUData10	114
CPUData11	118
CPUData12	119
CPUData13	120
CPUData14	121
CPUData15	123
CPUData16	124
CPUData17	125
CPUData18	126
CPUData19	129
CPUData20	130
CPUData21	131
CPUData22	133

Signal Name	Pin Number
CPUData23	134
CPUData24	135
CPUData25	136
CPUData26	137
CPUData27	138
CPUData28	139
CPUData29	140
CPUData30	143
CPUData31	144
DataP0	145
DataP1	146
DataP2	149
DataP3	150
EarlyPgWr	56
MemAdrEn	164
MemDataEn	160
MemData0	61
MemData1	62
MemData2	63
MemData3	64
MemData4	65
MemData5	66
MemData6	71
MemData7	72
MemData8	73
MemData9	74
MemData10	75
MemData11	76
MemData12	78
MemData13	79
MemData14	80
MemData15	81
MemData16	82
MemData17	85
MemData18	86
MemData19	87
MemData20	88
MemData21	89
MemData22	90
MemData23	91
MemData24	92
MemData25	94
MemData26	95
MemData27	96
MemData28	97
MemData29	98
MemData30	99
MemData31	100

Signal Name	Pin Number
RdAdrSel	165
Request	59
Reset	159
WBFull	60
WtMem	155
VCC	25
VCC	41
VCC	67
VCC	83
VCC	101
VCC	117
VCC	128
VCC	141
VCC	147
VCC	152
GND	14
GND	23
GND	24
GND	34
GND	42
GND	55
GND	68
GND	69
GND	70
GND	77
GND	84
GND	93
GND	102
GND	108
GND	115
GND	116
GND	122
GND	127
GND	132
GND	142
GND	148
GND	151
GND	161
GND	162
GND	163
reserved	57

Pinout and Package Information
(Continued)

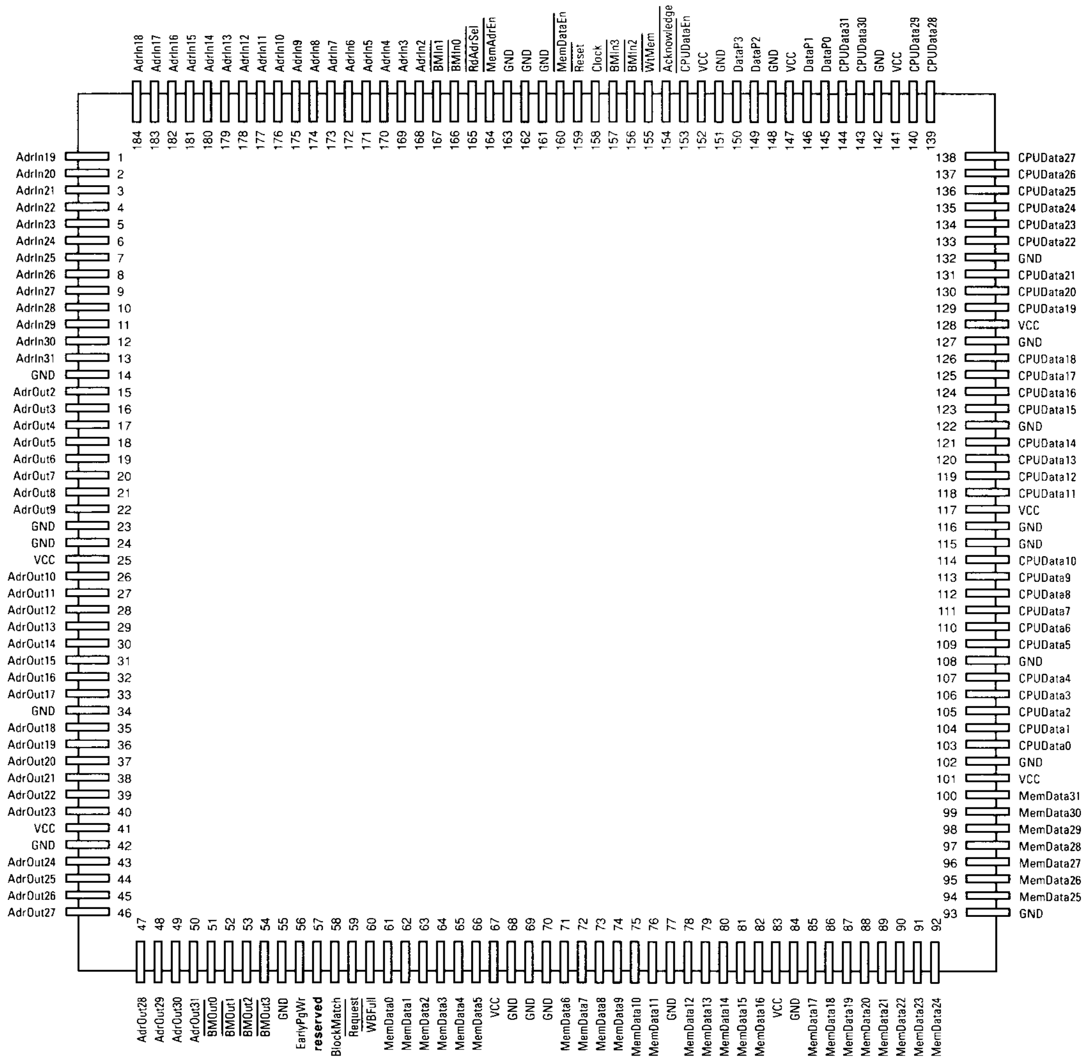
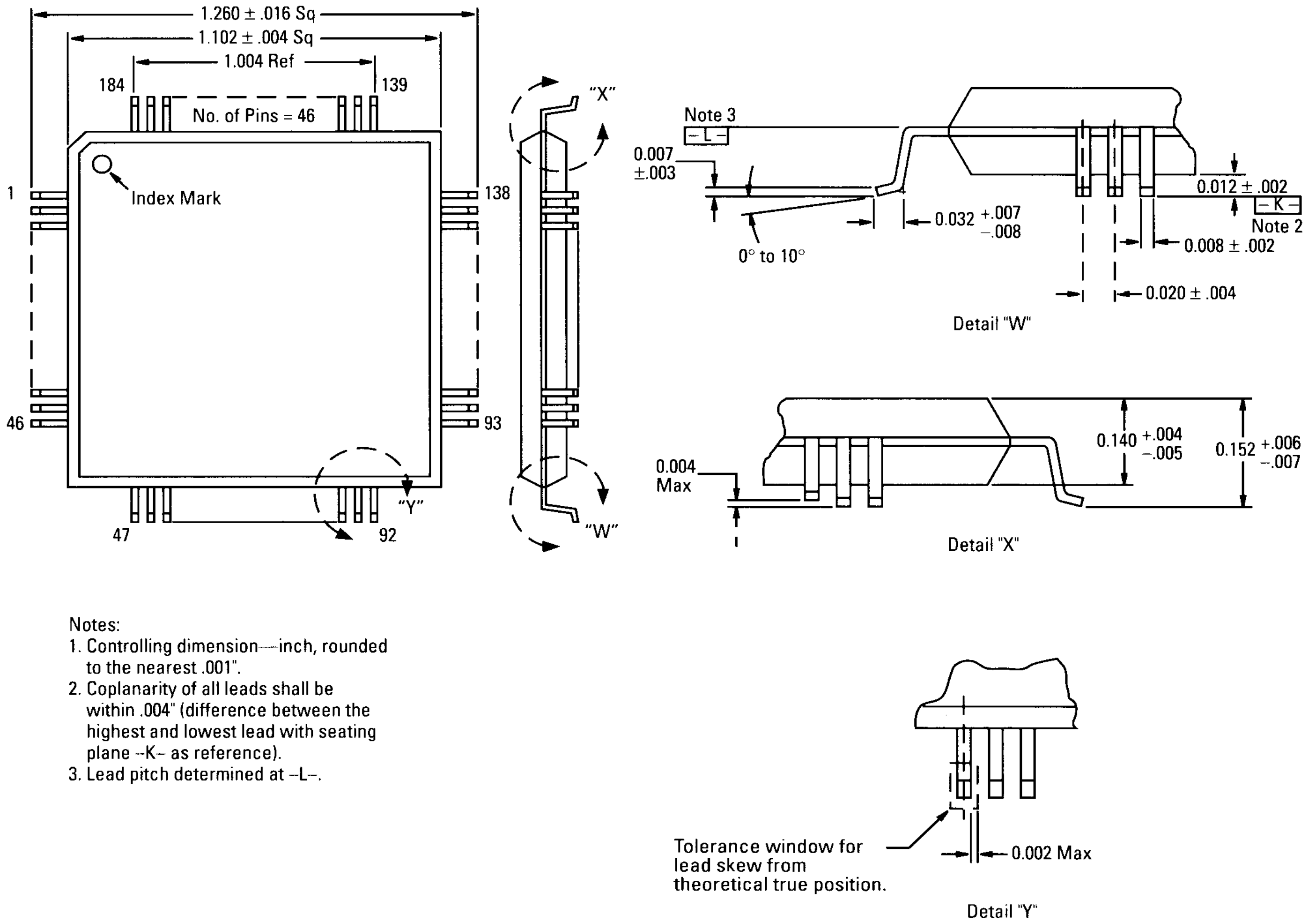


Figure 21. 184-Pin Plastic Quad Flat Pack (PQFP) Pin Diagram

Pinout and Package Information
(Continued)



Notes:
1. Controlling dimension—inch, rounded to the nearest .001".
2. Coplanarity of all leads shall be within .004" (difference between the highest and lowest lead with seating plane -K- as reference).
3. Lead pitch determined at -L-.

Figure 22. 184-Pin Plastic Quad Flat Pack (PQFP) Mechanical Drawing

Ordering Information

LR3220 Q C - 25

- 25: Operating Frequency:
  - 25 = 25 MHz
  - 33 = 33.33 MHz
- C: Temperature Range:
  - C = Commercial
  - M = Military
- Q: Package Code:
  - Q = 184-pin Plastic Quad Flat Pack (PQFP)
  - G = 180-pin Ceramic Pin Grid Array (CPGA)
- LR3220: Device Number

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LR3220 Read-Write Buffer
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