L64730 Discrete Cosine Transform Processor (DCT)

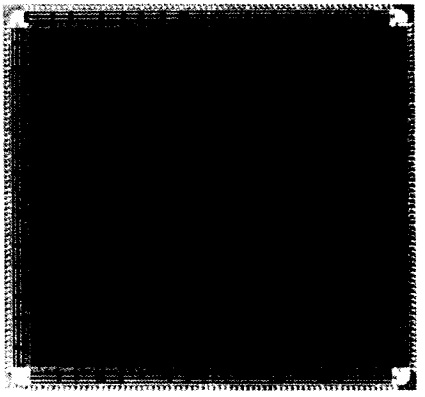
Description

The discrete cosine transform processor computes both the forward and inverse DCT over 8 x 8 data blocks and meets the proposed CCITT (Consultative Committee on International Telephones and Telegraphs) standard, H.261. Up to 12 bits of data precision is available for the input and output data. The output can also be rounded to 9 or 12 bits. The device supports data rates up to 40 MHz.

The cosine basis functions and control signals are generated internally; the user only supplies a signal indicating the beginning of the data block, the direction of the transform and the number of bits desired at the output.

The device can also perform the loop filtering specified in the CCITT standard. This operation is performed at the same rate as the DCT and inverse DCT.

The discrete cosine transform is ideal for image or video compression systems as the DCT coefficients can typically be coded with fewer bits of information than the original image. To ensure proper tracking between an encoder and decoder, the proposed CCITT standard has placed strict limits on the statistics of the errors encountered when computing the inverse DCT. This device complies fully with these requirements.



L64730 Chip

The device is available in 68-pin Grid Arrays or 100-pin PQFP (Plastic Quad Flat Pack) package.

Features

- 8 x 8 data block
- Handles continuous data streams
- Up to 12-bit input and output precision
- Computes forward and inverse transforms
- Multiple devices can be used for increased performance
- Compatible with proposed CCITT standard
- Performs the spatially variant loop filtering
- 20/30/40 MHz clock rates
- Simple external control
- 68-pin CPGA or PPGA (Ceramic or Plastic Pin Grid Array) or 100-pin PQFP (Plastic Quad Flat Pack) package

Pin Listing and Description (SIGNAL.0 is always the LSB)

DI.0-DI.11
Twelve-bit data input bus for either the original image (forward DCT or filter mode) or DCT coefficients (inverse DCT). Data has a two's complement normalized format and is input in a raster scan fashion.

DO.0-DO.11
Twelve-bit data output bus for either the reconstructed image (inverse DCT or filter mode) or DCT coefficients (forward DCT). Data has a two's complement normalized format.

AUX.0-AUX.11
Twelve-bit auxiliary input bus. In DCT mode, the value on this bus is subtracted from that on the DI bus before the transform is computed. In inverse DCT mode, the value on this bus is added to the processor output. In either case, the value on the AUX bus is ignored if the processor is in FILTER mode or the signal INTER is LOW.

INTER
When HIGH specifies that the device is in the inter-frame mode. The value on the AUX bus is only used in inter-frame mode when the device is computing the forward or inverse DCT.

SYNC
Indicates the beginning of a data block when HIGH. Should be LOW during all other input data cycles.

FN.0-FN.1
Function select pins. When FN.0 and FN.1 are both LOW, the inverse DCT is computed. The forward DCT is computed when both FN.0 and FN.1 are HIGH. The loop filtering is performed when FN.0 is HIGH and FN.1 is LOW.

RND9
The output is rounded to 9 bits when RND9 is HIGH and is rounded to 12 bits when RND9 is LOW.

CLIP
Clips negative values at the output to zero when HIGH. Has no effect when LOW.

CLK
System clock. Controls all system functions at LOW to HIGH transitions.

RESET
Internal controller active HIGH reset for testing. Should be LOW for normal operation.

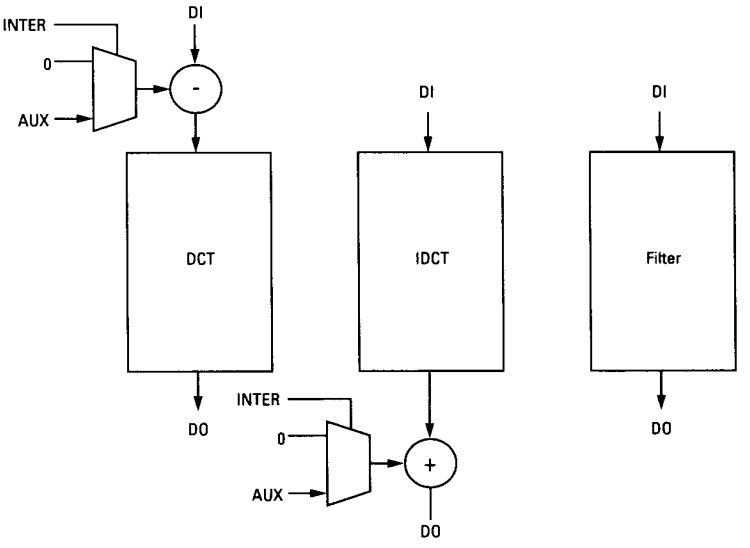
TESTO
LSI Logic test output. Should be left unconnected.

Pin Description Summary

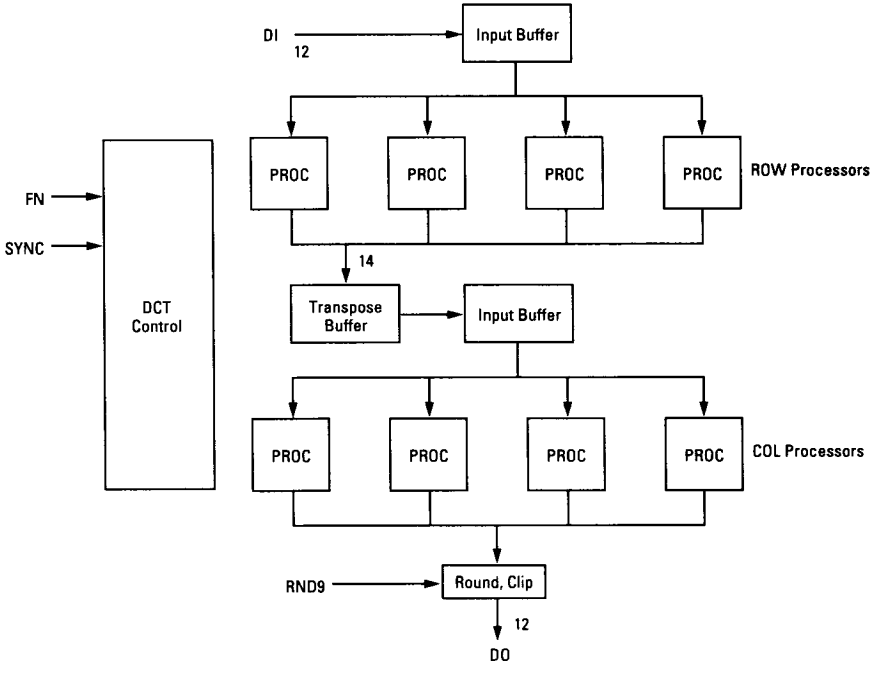
Pin	No. of Pins	I/O	Description
DI.0-DI.11	12	I	Data input bus
DO.0-DO.11	12	O	Data output bus
AUX.0-AUX.11	12	I	Auxilary input bus
INTER	1	I	Inter-frame mode flag
SYNC	1	I	Begin data block flag
FN.0-FN.1	2	I	Function select
RND9	1	I	Rounding flag
CLIP	1	I	Clip flag
CLK	1	I	Clock
RESET	1	I	Reset
TESTO	1	O	Test output-no connect

Block Diagrams

Discrete Cosine Transform Processor Operating Modes



Discrete Cosine Transform Processor Block Diagram



Functional Description

The DCT processor computes a separable transform: first 1-D transforms are computed over each of the 8 rows followed by 1-D transforms over each of the columns. Four processors compute the row DCTs while the other four processors compute the column DCTs. A buffer between the two sets of processors transposes the data.

Buffers at the input to each set of processors reformat the data from the raster scanned input format to that required by the processor arrays. The output of each group of processors is scaled and clipped if overflow occurs.

DCT Mode

When FN.0 and FN.1 are HIGH, the processor calculates the forward transform.

When FN.0 and FN.1 are LOW, the processor calculates the inverse transform. BD (u,v) and bd (x,y) are related by the equations shown in Table 1.

Table 1. DCT Mode

FN.0	FN.1	Transform	Equation
1	1	Forward	$BD(u,v) = \frac{1}{32} C(u) C(v) \sum_{x=0}^{7} \sum_{y=0}^{7} bd(x,y) \cos\left[\frac{\pi u(2x+1)}{16}\right] \cos\left[\frac{\pi v(2y+1)}{16}\right]$
0	0	Inverse	$bd(x,y) = 2 \sum_{u=0}^{7} \sum_{v=0}^{7} C(u)C(v) BD(u,v) \cos\left[\frac{\pi u(2x+1)}{16}\right] \cos\left[\frac{\pi v(2y+1)}{16}\right]$

Note:

$$C(i) = \begin{cases} \frac{1}{\sqrt{2}} & \text{if } i = 0 \\ 1 & \text{if } i \neq 0 \end{cases}$$

The constant scale factors, 1/32 and 2, are not identical to those used in the CCITT standard. The difference is due solely to the use of fractional data formats instead of an integer format. The input and output data is the same in both cases and the fractional format is used only to simplify the description of the device for inputs and outputs with different bit widths.

Loop Filter Mode

The loop filter operation (FN.0 HIGH and FN.1 LOW) is also a separable operation and can be performed in a manner similar to the DCT. The filter is block oriented, and different filter coefficients are used for different positions within the 8 x 8 data block. Figure 1 shows the four sets of coefficients at the left. The position within the 8 x 8 data block that each set of filter coefficients is used is shown in the right half of the diagram. Note that each coefficient is multiplied by the scale factor 1/16.

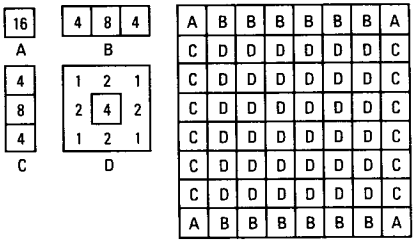


Figure 1. Loop Filter Coefficients

Inter Mode

When the pin, INTER, is HIGH, the value on the AUX bus is subtracted from the data on the DI bus (Forward DCT) or added to the result generated from the IDCT processor (Inverse DCT). If INTER is LOW or the device is in the filter mode, the data on AUX is internally set to zero so that the input and output data is not modified. This mode is useful when inter-frame prediction is used and the AUX bus carries the predicted value. For the forward DCT, the difference between the primary input (DI) and the predicted value (AUX) is coded.

It should be noted that overflow in the input adder is not detected. Normally, the data on both the DI and AUX buses will be positive and no overflow can occur. However, if the data on DI and AUX have different signs, the user should prevent overflow by shifting both values right one position.

Functional Description (Continued)

Output Rounding and Clipping

The output of processor is rounded to either 9 or 12 bits depending on the value of RND9. It should be noted that when the output is rounded to 9 bits, DO.0-DO.2 will contain useless information. Overflow is detected at both the output of the processor and at the output of the final adder for interframe processing. When either positive or negative overflow occurs at these points, the value at that point is replaced by the most positive or negative number, respectively.

Negative values at the output of the device can be set to zero by setting the CLIP pin HIGH. Normally, when performing the inverse DCT, the output (after interframe reconstruction if applicable) represents the reconstructed image and should contain only positive values. Setting CLIP HIGH will enforce this constraint. If CLIP is LOW, negative values pass to the output without change.

Setting the Operation Mode

There are five external signals which determine the operation of the device. The FN.0, FN.1, RND9, INTER and CLIP pins set the function of the device and the number of output bits desired. When the FN.0 or FN.1 signals make a transition, all partial results inside the device will be corrupted. To prevent the loss of data, the user should wait for 98 cycles after the last input value has been latched before changing the function.

I/O Data Ordering and Formats

The processor is block oriented and always operates on a single 8 x 8 data block. The data in the block is raster scanned to form the input data sequence, i.e., the points are input in the order bd(0,0), bd(1,0), bd(2,0), ... , bd(7,0), bd(0,1) ... bd(7,7). For the forward and inverse DCT, the output order is transposed and in a slightly irregular ordering: BD(0,0), BD(0,7), BD(0,1), BD(0,6), BD(0,2), BD(0,5), BD(0,3), BD(0,4), BD(1,0), BD(1,7), ... , BD(7,4). For the case of the loop filter, the output is transposed. Data on the AUX input is supplied in raster order for DCT operations and the same order as the output data in IDCT mode.

The data ordering is illustrated in Figure 2. The left part of the figure shows the order for the input data for all functions. The center of the figure shows the output order when filtering and the right of the figure shows the output order when performing forward or inverse DCTs. In each figure, the number given for each data element in the block is the relative cycle number in which that element will appear at the input or output.

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55
56	57	58	59	60	61	62	63

0	8	16	24	32	40	48	56
1	9	17	25	33	41	49	57
2	10	18	26	34	42	50	58
3	11	19	27	35	43	51	59
4	12	20	28	36	44	52	60
5	13	21	29	37	45	53	61
6	14	22	30	38	46	54	62
7	15	23	31	39	47	55	63

0	8	16	24	32	40	48	56
2	10	18	26	34	42	50	58
4	12	20	28	36	44	52	60
6	14	22	30	38	46	54	62
7	15	23	31	39	47	55	63
5	13	21	29	37	45	53	61
3	11	19	27	35	43	51	59
1	9	17	25	33	41	49	57

Figure 2. Data Ordering

The input and output data is always in a two's complement format. In addition, the data is always in a normalized (to the MSB) fractional format so that if fewer than 12 bits are used at the input or output, the LSBs and not the MSBs are ignored. This means that all inputs and outputs can be treated as fractional numbers between +1 and -1 with the binary point between bits DI.11 and DI.10 and between bits DO.11 and DO.10. Of course, the conversion between this normalized fractional representation and an integer notation is just a matter of shifting the binary point and in no way affects the results.

Data Interfaces

The device is ideally suited to processing 8-bit unsigned image data or 9-bit signed image data. The difference of two 8-bit image values is a 9-bit signed value and hence can be handled. When processing unsigned data, the input data to the DCT should have a zero sign bit appended. The output of the IDCT will be rounded and clipped (if CLIP is HIGH) to a 8-bit unsigned value (the useless sign bit can be ignored). For these cases, when performing the DCT, RND9 should be LOW and when the IDCT is being performed, RND9 should be HIGH.

CCITT H.261 Operation

For CCITT H.261 DCT operation, the 8-bit image data can be supplied on the DI bus and the prediction value on the AUX bus. A zero sign bit must be added to both values, forming 9-bit signed numbers. If the difference is computed externally, the 9-bit signed difference can be supplied on the DI bus and INTER set LOW to cause the AUX bus to be ignored. RND9 should be set LOW to get full 12-bit DCT coefficients at the DO output.

The 12-bit reconstructed DCT coefficients are supplied on the DI bus when performing the IDCT. If the addition for INTER mode at the output of the IDCT is performed within the device, the 8-bit unsigned predicted value is supplied on the AUX bus with an appended zero sign bit. If RND9 and CLIP are both HIGH, the 8-bit unsigned output will appear on the DO bus with a zero sign bit that can be ignored.

JPEG Operation

The JPEG standard requires that the 8-bit unsigned input data be offset by -0.5 (-128 in integer format) prior to the DCT processing. Operation in this mode is very similar to CCITT operation in INTER mode. However, the constant 0.5 (0.10000000000) is placed on the AUX bus in both forward and inverse DCT operation. In addition, because the input to the DCT processor is in the range ±0.5 instead of ±1, the 11-bit output of the DCT processor will appear on the 11 LSBs of the DO bus. The output for this case will always be sign extended.

The 11-bit signed reconstructed DCT coefficients should be sign extended to 12-bits and supplied on the DI bus for inverse DCT operation. The 8-bit unsigned pixel outputs will appear on the DO bus with an appended zero sign bit.

Table 2. Data Formats

Mode	FN.0	FN.1	INTER	RND9	CLIP	AUX.11-AUX.0	DI.11-DI.0	DO.11-DO.0
CCITT, Forward DCT inter mode	1	1	1	0	0	0.PPPPPPPP000	0.AAAAAAAA000	S.BBBBBBBBBB
CCITT, Forward DCT intra mode	1	1	0	0	0	-.----------	0.AAAAAAAA000	S.BBBBBBBBBB
CCITT, inverse DCT inter mode	0	0	1	1	1	0.PPPPPPP000	S.BBBBBBBBB	0.AAAAAAAA----
CCITT, inverse DCT intra mode	0	0	0	1	1	-.----------	S.BBBBBBBBB	0.AAAAAAAA----
JPEG,forward DCT	1	1	1	0	0	0.10000000000	0.AAAAAAAA000	S.SBBBBBBBB
JPEG, inverse DCT	0	0	1	1	1	0.10000000000	S.SBBBBBBBB	0.AAAAAAAA----
Forward DCT 9-bit signed data input	1	1	0	0	0	-.----------	S.AAAAAAAA000	S.BBBBBBBBB
Inverse DCT 9-bit signed data output	0	0	0	1	0	-.----------	S.BBBBBBBBB	S.AAAAAAAA----
Forward DCT 12-bit signed data input	1	1	0	0	0	-.----------	S.AAAAAAAAAA	S.BBBBBBBBB
Inverse DCT 12-bit signed data output	0	0	0	0	0	-.----------	S.BBBBBBBBB	S.AAAAAAAAAA
Loop filter	1	0	0	1	1	-.----------	0.AAAAAAAA000	0.AAAAAAAA----

S = Sign Bit, A = Image Data Bit, B = DCT Coefficient Bit, P = Predicted Image Data Bit, - = Undefined Bit

Performance

Error Performance

Table 3 shows the error performance of the device for various operating conditions. The input data in each case is random and for the inverse DCT was generated according to the proposed CCITT standard which requires the simulation of 60,000 blocks. The output of the device was compared to the forward or inverse transform of the input data or the filtered version of the input data when computed with double precision floating-point and rounded to the number of bits indicated. All error measures are referenced to the LSB of the output. The format for each entry is: measured_error/specified_max_error.

Table 3. L64730 Error Performance

DCT	No. Input Bits	No. Output Bits	Max Magnitude Error	Mean Error	Mean Sq Error	Max Pixel Mean Error	Max Pixel Mean Sq Error
Inv DCT	12	9	1/1	.008/.015	.018/.020	.010/.015	022/.060
For DCT	12	12	1/NA	.0013/NA	.077/NA	.0075/NA	.084/NA
Filter	9	9	0/NA	0/NA	0/NA	0/NA	0/NA
Filter	12	12	1/NA	.026/NA	.026/NA	.11/NA	.11/NA

Operation Speed

The performance of the DCT processor and the requirements on the external memory access time are given in Table 4. These figures apply to all three device operations.

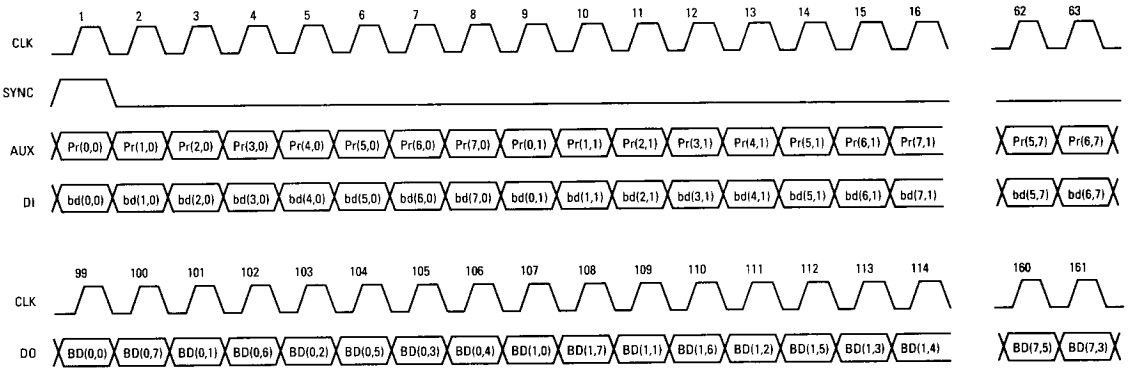
Table 4. Performance and Memory Access Requirements

n	Clock Freq (MHz)	Cycles	Execution Time (μsec)	External RAM Access Time (ns)
8	30	64	2.11	33
8	40	64	1.60	25

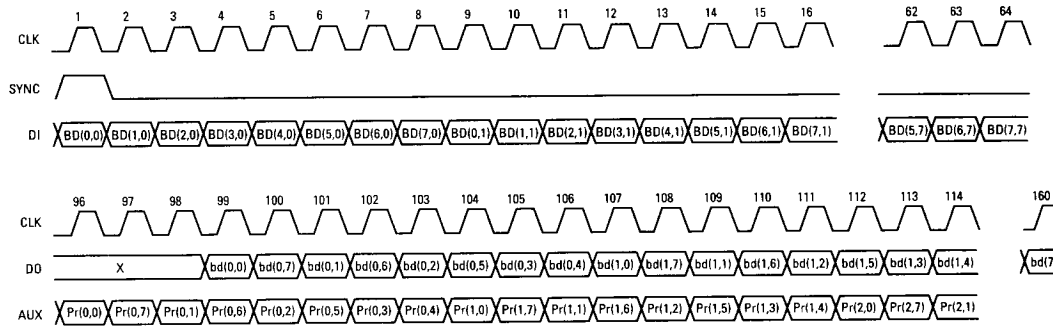
Although the execution time is only 64 cycles, there is a latency or delay of 98 cycles between the first input of a data block and the first output of the data block. In forward DCT mode, the INTER and AUX signals have the same latency as DI. In inverse DCT mode, INTER and AUX have a latency of only three cycles. Therefore, care must be taken to appropriately delay the data on the INTER and AUX pins.

Functional Waveforms

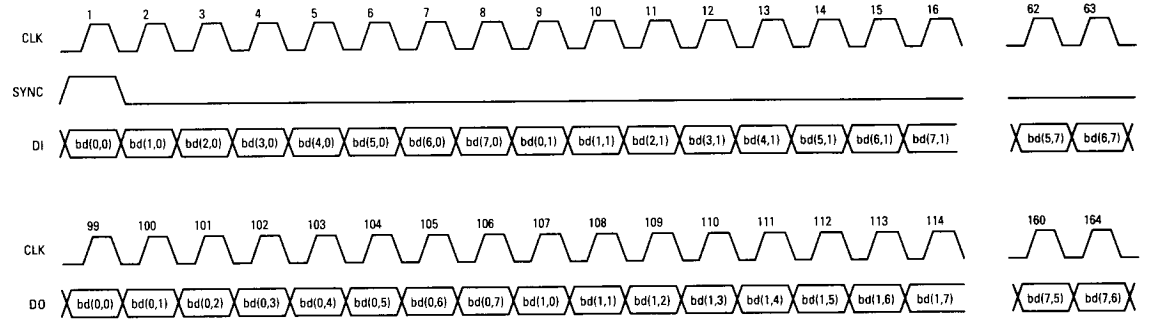
DCT Mode. If INTER is LOW, the data on AUX has no affect



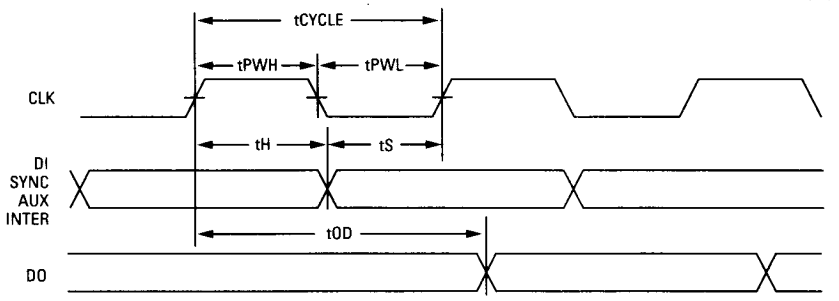
IDCT Mode. If INTER is LOW, the data on AUX has no affect



Filter Mode



AC Timing Waveform



AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64730-40		L64730-30		L64730-20	
		Min	Max	Min	Max	Min	Max
tCYCLE	CLK cycle time	25		33		50	
tPWH	Min CLK pulse width, HIGH	11		15		20	
tPWL	Min CLK pulse width, LOW	11		15		20	
tS	Input setup time to CLK	6		7		10	
tH	Input hold time to CLK	2		2		3	
tOD	DO output dealy from CLK		19*		22*		25*

Notes:
1. All times are in ns.
2. *Output loading = 50 pF.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Units
DC supply voltage	VDD	-0.3 to +7	V
Input votage	VIN	-0.3 to VDD +0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC supply voltage	VDD	+3 to +6	V
Operating ambient Temperature range Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges(1)

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIL	Low level input voltage				0.8	V
VIH	High level input voltage Commercial temperature range		2.0			V
IIN	Input current	VIN = VDD	-370		400	µA
VOH	High level output voltage	Comm and Mil IOH = -4 mA	2.4	4.5		V
VOL	Low level output voltage	Comm and Mil IOL = 4 mA		0.2	0.4	V
IOS	Output short circuit current(2)	VDD = Max, VO = VDD	30	75	140	mA
		VDD = Max, VO = 0V	-25	-70	-140	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS			10	mA
IDD	Operating supply current(3)	tCYCLE = 25 ns		400		mA
CIN	Input capacitance	Any input		2.5		pF
COUT	Output capacitance	Any output		2.0		pF

Notes:
1. Commercial temperature range is 0°C to +70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. For 40 MHz device.

L64730 Package Pin Information (68-Pin PGA, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A3	AUX.0	J10	DI.10	D1	DO.4	F1	VDD
B3	AUX.1	K11	DI.11	E2	DO.5	G10	VDD
A4	AUX.2	C10	DI.2	E1	DO.6	K1	VDD
B4	AUX.3	D11	DI.3	G1	DO.7	K10	VDD
A5	AUX.4	D10	DI.4	H2	DO.8	K2	VDD
B5	AUX.5	E11	DI.5	H1	DO.9	L10	VDD
A6	AUX.6	E10	DI.6	L7	FN.0	L6	VDD
B7	AUX.7	H11	DI.7	L8	FN.1	A10	VSS
A8	AUX.8	H10	DI.8	K3	INTER	A2	VSS
B8	AUX.9	J11	DI.9	L4	RESET	B6	VSS
A9	AUX.10	B1	DO.0	K4	RND9	F11	VSS
B9	AUX.11	C2	DO.1	K5	SYNC	F2	VSS
L3	CLIP	J2	DO.10	K9	TESTO	G11	VSS
F10	CLK	J1	DO.11	A7	VDD	K6	VSS
B11	DI.0	C1	DO.2	B10	VDD	L2	VSS
C11	DI.1	D2	DO.3	B2	VDD	L9	VSS

L64730 Package Pin Information (68-Pin PGA, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	VSS	B8	AUX.9	F1	VDD	K2	VDD
A3	AUX.0	B9	AUX.11	F2	VSS	K3	INTER
A4	AUX.2	B10	VDD	F10	CLK	K4	RND9
A5	AUX.4	B11	DI.0	F11	VSS	K5	SYNC
A6	AUX.6	C1	DO.2	G1	DO.7	K6	VSS
A7	VDD	C2	DO.1	G10	VDD	K9	TESTO
A8	AUX.8	C10	DI.2	G11	VSS	K10	VDD
A9	AUX.10	C11	DI.1	H1	DO.9	K11	DI.11
A10	VSS	D1	DO.4	H2	DO.8	L2	VSS
B1	DO.0	D2	DO.3	H10	DI.8	L3	CLIP
B2	VDD	D10	DI.4	H11	DI.7	L4	RESET
B3	AUX.1	D11	DI.3	J1	DO.11	L6	VDD
B4	AUX.3	E1	DO.6	J2	DO.10	L7	FN.0
B5	AUX.5	E2	DO.5	J10	DI.10	L8	FN.1
B6	VSS	E10	DI.6	J11	DI.9	L9	VSS
B7	AUX.7	E11	DI.5	K1	VDD	L10	VDD

Note: Pins G2, K7, K8 and L5 are no connects.

L64730 Package Pin Information (100-Pin PQFP, By Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS	25	VDD	57	DI.11	76	VDD
5	VDD	27	VDD	58	DI.10	78	VSS
6	DO.0	29	VSS	59	DI.9	81	AUX.11
7	DO.1	30	INTER	60	DI.8	82	AUX.10
8	DO.2	31	CLIP	61	DI.7	84	AUX.9
9	DO.3	32	RND9	62	VDD	85	AUX.8
10	DO.4	33	RESET	63	VSS	87	AUX.7
11	DO.5	36	SYNC	64	CLK	90	VDD
12	DO.6	40	VSS	65	VSS	91	VSS
13	VSS	42	VDD	66	DI.6	92	AUX.6
15	VDD	45	FN.0	68	DI.5	93	AUX.5
17	DO.7	47	FN.1	69	DI.4	94	AUX.4
18	DO.8	48	TESTO	70	DI.3	95	AUX.3
19	DO.9	50	VSS	71	DI.2	96	AUX.2
21	DO.10	54	VDD	72	DI.1	98	AUX.1
23	DO.11	55	VDD	73	DI.0	100	AUX.0

L64730 Package Pin Information (100-Pin PQFP, By Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
100	AUX.0	58	DI.10	10	DO.4	42	VDD
98	AUX.1	57	DI.11	11	DO.5	5	VDD
82	AUX.10	71	DI.2	12	DO.6	54	VDD
81	AUX.11	70	DI.3	17	DO.7	55	VDD
96	AUX.2	69	DI.4	18	DO.8	62	VDD
95	AUX.3	68	DI.5	19	DO.9	76	VDD
94	AUX.4	66	DI.6	45	FN.0	90	VDD
93	AUX.5	61	DI.7	47	FN.1	1	VSS
92	AUX.6	60	DI.8	30	INTER	13	VSS
87	AUX.7	59	DI.9	33	RESET	29	VSS
85	AUX.8	6	DO.0	32	RND9	40	VSS
84	AUX.9	7	DO.1	36	SYNC	50	VSS
31	CLIP	21	DO.10	48	TESTO	63	VSS
64	CLK	23	DO.11	15	VDD	65	VSS
73	DI.0	8	DO.2	25	VDD	78	VSS
72	DI.1	9	DO.3	27	VDD	91	VSS

Packaging

68-Pin Pin Grid Array: See NB Package in Package Selector Guide
100-Pin Plastic Quad Flat Pack: See PB Package in Package Selector Guide

Ordering Information

L64730 G C -XX

- **-XX** — Speed MHz
- **C** — Temperature Range/Flow Option
  - C = Commercial (0°C to 70°C)
  - M = Military (-55°C to + 125°C)
    Processed to MIL-STD-883C Level B
- **G** — Package Code
  - G = 68-Pin Ceramic Pin Grid Array
  - N = 68-Pin Plastic Pin Grid Array
  - Q = 100-Pin Plastic Quad Flat Pack
- **L64730** — Device Type
  Discrete Cosine Transform Processor