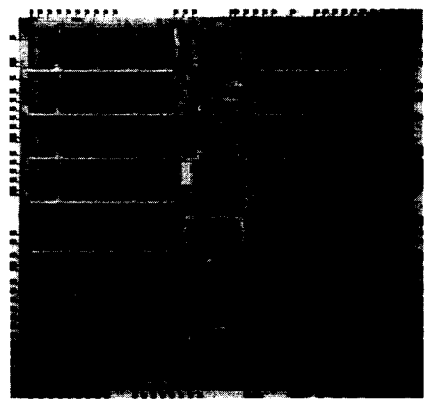
L64240
Multi-Bit Filter (MFIR)

LSI LOGIC

Description

The L64240 is a 64-tap high-speed transversal filter processor consisting of two 32-tap sections, with 8-bit wide coefficients and data. The processor can be configured as a 1-D (one-dimensional) filter for radar or other signal processing applications, or as a 2-D (two-dimensional) filter for image processing applications. The processor accepts 2-D data directly from a L64210/L64211 Variable-Length Video Shift Register or other video source. The coefficients can be changed to perform adaptive filtering and correlation. The window and/or precision of a 1-D or 2-D filter is expandable using more L64240 processors with minimal external logic.

The processor is ideally suited for real-time image processing applications such as video pattern matching, noise removal, inverse filtering, edge enhancement, and edge detection. The maximum window size is 8 x 8 for a single chip. Video output formatting circuitry is also available on-chip to alter gain, threshold and other parameters. Worst-case commercial grade data throughput of 20 MHz make the processor suitable for radar processing. Implemented in 1.5 micron drawn date length (0.9-micron effective channel length) low power HCMOS technology, the L64240 is available in 155-lead Ceramic Pin Grid Array Package.



L64240 Chip

Features

- Two 32-tap sections, each 8-bit data and coefficients
- One 32-tap section, each 16-bit data or coefficients
- Reconfigurable for 1-D and 2-D correlation/convolution
- Multiple processors can be used to extend data and/or coefficient precision up to 24 bits
- Multiple processors can achieve window sizes of over 1024 taps
- Two's complement or unsigned 8-bit input data and coefficient
- Output precision up to 40 bits for 1-D process ing, up to 24 bits for 2-D processing
- Double buffering of coefficients
- Format adjustment for video display
- On-chip barrel shifter for precision expansion
- Block floating-point format output
- Configurable as an IIR filter
- High speed operation

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

- Ability to perform Sobel edge extraction
- Available in 155-lead CPGA (Ceramic Pin Grid Array) package

Architecture

The L64240 Multi-Bit Filter is a stand-alone FIR (Finite Impulse Response) filter which can operate on either 1-D or 2-D data. It is easily reconfigurable to perform FIR filter operations with a variety of window sizes and shapes.

It operates at very high speeds and is useful in high-end applications such as radar signal processing, image processing, high speed data communications and other areas where performance and processing power are important.

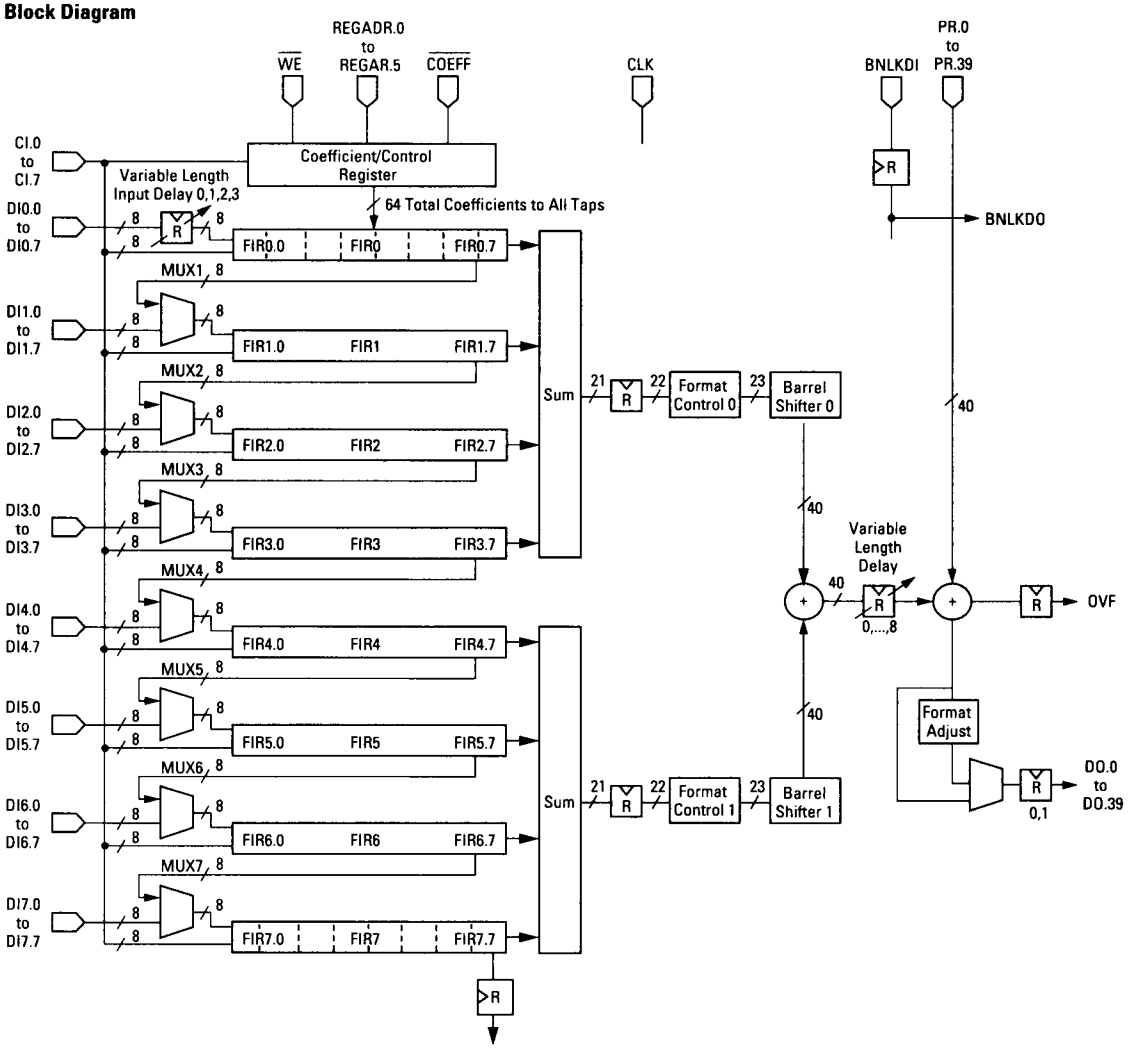
The L64240 performs convolution/correlation operations of the type:

$$1\text{-}D: y(n) = \sum_{l=0}^{L-1} h_l\, x(n-l)$$

$$2\text{-}D: y(n,m) = \sum_{l=0}^{L-1} \sum_{k=0}^{K-1} h_{l,k}\, x(n-l, m-k).$$

The device contains eight individual 8th order FIR filters (FIR0–FIR7).

Block Diagram



Architecture (Continued)

Each of the 64 taps accepts two's complement or unsigned 8-bit integer data and coefficients. The Multi-Bit Filter has eight separate input busses (DI0 through DI7), one for each of the FIR sections. By controlling the input source to each 8-tap FIR section, the Multi-Bit Filter can be configured as a 64th order 1-D FIR filter with 8-bit data and coefficients, a 32nd order 1-D FIR filter with 16-bit data or coefficients, or as a 2-D filter with a 2 x 32, 4 x 16 or 8 x 8 window. In addition, several Multi-Bit Filters can be cascaded to build higher order FIR filters and/or to process data and coefficients with larger widths.

All coefficients and most control signals are double-buffered. This allows the user to load a new set of coefficients and controls while processing continues on the current set. Thus, the processor does not require the insertion of new control inputs at the same speed as the data rate.

The outputs of the first four 8th order filters are summed together and the result is latched in a pipeline register. The sum of the last four 8th order FIR filters is latched in another pipeline register. The pipeline register outputs are sign-extended in the format control blocks and may be scaled in barrel shifter blocks. The barrel shifters provide the flexibility necessary to appropriately weight the ouput data in a multiprocessor system. The two barrel shifter outputs are summed to form the result of a 64th order FIR filter. Up to this stage no arithmetic overflow can occur regardless of the values of data, coefficients, and operating parameters.

This result is delayed by 0 to 8 cycles by the variable length output delay, to account for the latency which occurs in a multiprocessor system. The delayed result is added to the partial result bits (PR.0 to PR.39). This partial result represents an intermediate result in a multiprocessor system. As a stand-alone processor, the L64240 is normally used with the variable length output delay set for 0 or 1 delay, depending on the speed requirements, and the partial result input pins left unconnected, which automatically sets the PR bits to zero.

The sum of the filter output and the partial result may generate a positive or negative overflow, which is flagged. The format of the sum may be adjusted for video display. Among other functions, the format adjust block provides control to vary the contrast of the image or to generate binary images. When using the format adjust block, the partial result bits can be used to offset the filter output. The L64240 has an optional data output register. In FIR systems, the output register should be included in the data path. The L64240 can be configured as an IIR filter, in which case the output register is bypassed. A 40-bit output bus (DO) is available for a 1-D system and a 24-bit output bus is available in a 2-D system.

The Shift Register Output (SRO) is used to cascade 1-D filters in a multiprocessor system. In such a system the SRO output of one device can be connected to the DIO input of the next, effectively increasing the shift register length.

Pin Listing and Description

Note: For all buses, SIGNALY.X denotes the Xth bit of SIGNALY. The LSB of bus SIGNALY is SIGNALY.0

DI0-DI7
Eight individual data input buses, each 8 bits wide. When the L64240 is used as a 1-D filter with 8-bit wide data, only pins DI0.0 to DI0.7 are used. The remaining data input pins are either left unconnected or used for other functions, depending on the system configuration. When used as a 2-D filter processor with an 8 x 8 window, the L64240 operates with all 64 data input pins (DI0.0 to DI0.7, DI7.0 to DI7.7) active. DI0.0 to DI0.7, DI2.0 to DI2.7, and DI4.0 to DI4.7 are all input pins dedicated to DI data.

DI1.0 to DI1.7 are unidirectional input pins, which are shared with PR.0 to PR.7 inputs. DI3.0 to DI3.7 are bidirectional pins, which are shared with DO.0 to DO.7 outputs. DI5.0 to DI5.7 are bidirectional pins, which are shared with DO.8 to DO.15 outputs. DI6.0 to DI6.7 are unidirectional input pins, which are shared with PR.8 to PR.15 inputs. DI7.0 to DI7.7 are bidirectional pins, which are shared with SRO.0 to SRO.7 outputs. All unidirectional DI inputs default to LOW when left unconnected.

SR0.0 to SR0.7
Data output, which is DI0.0 to DI0.7 delayed by a minimum of 65 cycles and a maximum of 68 cycles, depending on the number of extra delays set in the variable input register. These signals come from data register of filter tap FIR7.7, delayed by an extra cycle in an output register. Typically, these signals would go to the DI0.0 to DI0.7 of another L64240 when operated as a 1-D processor with an expanded window. SR0.0 to SR0.7 are not used for window expansion in 2-D processing.

Pin Listing and Description (Continued)

CI.0 to CI.7
Coefficient/control input pins. An 8-bit coefficient can be loaded into any one of the 64 filter taps by choosing the address of the destination filter cell with REGADR.0 to REGADR.5, COEFF being LOW. CI.0 to CI.7 are used to input coefficents when decimal value of REGADR.0-REGADR.5 is less than 64. CI.0 to CI.7 are interpreted as control bits for setting various filter processes and output data format adjustment and gain parameters when REGADR.0 to REGADR.5 is between 0 and 5 inclusive and COEFF is HIGH. CI.0 to CI.7 are ignored when REGADR.0-REGADR.5 are greater than 5 during loading of control bits.

BNKLDI
Input signal, set HIGH to bank load new coefficients and certain decoded internal control signals from master to slave registers. While asynchronously loading coefficients/controls with respect to CLK, BNKLDI is held LOW until bank loading occurs. When loading coefficient/control synchronous to CLK, BNKLDI is held HIGH.

BNKLDO
Output pin, BNKLDI signal delayed by one CLK cycle. This may be used as BNKLDI for the next L64240 in a 1-D multiprocessor system.

WE
Write enable input, active LOW, for enabling the loading of coefficients and decoded control signals into the destination latches selected by REGADR.0 to REGADR.5 and COEFF.

REGADR.0 to REGADR.5
Inputs indicating the destination address of the coefficients or control signals where they are loaded into master latches when WE is LOW. When (REGADR.0-REGADR.5) are between 0 and 63 inclusive, and COEFF is LOW, CI.0 to CI.7 are interpreted as coefficients. When (REGADR.0-REGADR.5) are between 0 and 5 inclusive and COEFF is HIGH, the CI inputs are interpreted as control signals. When (REGADR.0-REGADR.5) > 5 and COEFF is HIGH, destination address is invalid.

CLK
System clock controls all positive edge-triggered master-slave flip-flops in the data path. When BNKLDI is HIGH, CLK enables the level-triggered slave latches of all coefficients and certain decoded control signal destinations.

DO.0 to DO.39
Multi-Bit Filter data output. The value of these signals is derived from the biased sum of all 64 taps and the partial result (PR.0 to PR.39), if any, from another L64240. The sum may be scaled and format adjusted (negative clipped, etc.) before being output via an optional output register.

The outputs DO.0 to DO.7 are bidirectional pins shared with input signals DI3.0 to DI3.7. The outputs DO.8 to DO.15 are bidirectional pins shared with input signals DI5.0 to DI5.7. DO.16 to DO.39 are dedicated output pins. All 40 DO bits may be used in a 1-D processing system. In the case of 2-D processing, only DO.16 to DO.39 are available.

RESET
Input pin. Held LOW during power on and initialization.

OVF
Positive or negative overflow flag. Outputs a HIGH if the addition of the output of the variable length delay and the external partial result (PR.0 to PR.39), if any, yields a two's complement result greater than 7FFFFFFFFF (base 16) or less than 8000000000 (base 16). This flag is generated prior to any format adjustment.

PR.0 to PR.39
Partial result inputs. During multiprocessor operation the 24 most significant bits (PR.16 to PR.39) come from the DO.16 to DO.39 outputs of the preceding processor. PR.0 to PR.15 can be used in 1-D processing. PR.0 to PR.15 cannot be used in the 2-D case. When any of PR.0 to PR.39 pins are left unconnected, the internal values of those signals are set to 0.

The partial results can be used to offset the filter output before format adjustment.

COEFF
Input pin. When LOW, specifies that CI.0 to CI.7 are coefficients. When HIGH, specifies that CI are control bits provided REGADR.0 to REGADR.5 are between 0 and 5 inclusive.

Pin Description Summary

Pin	No. of Pins	I/O	Description
DI0.0-DI0.7	8	I	Data input bus 0
DI1.0-DI1.7 Shared with PR.0-PR.7	8	I I	Data input bus [2-D] Partial result input (8 least significant bits [1-D])
DI2.0-DI2.7	8	I	Data input bus 2
DI3.0-DI3.7 Shared with D0.0-D0.7	8	I 0	Data input bus 3 [2-D] Filter output (8 least significant bits [1-D])
DI4.0-DI4.7	8	I	Data input bus 4
DI5.0-DI5.7 Shared with DO.8-DO.15	8	I 0	Data input bus 5 [2-D] Filter output [1-D]
DI6.0-DI6.7 Shared with PR.8-PR.15	8	I 1	Data input bus 6 [2-D] Partial result input [1-D]
DI7.0-DI7.7 Shared with SR0.0-SR0.7	8	I 0	Data input bus 7 [2-D] Delayed DI0.0-DI0.7 [1-D]
CI.0-CI.7	8	I	Coefficient/control input bus
PR.16-PR.39	24	I	Partial result input
D0.16-D0.39	24	0	Filter output
CLK	1	I	System clock
BNKLDI	1	I	Bank loads
BNKLDO	1	0	BNKLDI delayed one CLK cycle
$\overline{WE}$	1	I	Write enable for coefficient/control registers
REGADR.0-REGADR.5	6	I	Address of coefficient/control registers
OVF	1	0	Overflow flag
$\overline{COEFF}$	1	I	Indicates if CI are coefficient or control inputs
$\overline{RESET}$	1	I	Reset/initialize pin

Functional Overview

One-Dimensional Processing: The L64240 performs convolution/correlation of the form:

$$DO(n) = FA \quad PR(n-1) + 2^{-G} \cdot f \sum_{i=0}^{63} hi\ DIO(n - i - D1 - D2 - 3)$$

DO(n) is the time domain filter output of a 64th order FIR filter.

DIO(n - i) is the delayed data input (the data value of the ith filter tap at time n). The position of the ith filter tap (FIRy.x) in the L64240 block diagram can be found by:

$$i = 8y + x.$$

hi is the active coefficient in the ith filter cell, which in this case is assumed to be time invariant. The sum of the 64 products of data and coefficients in all the filter taps can be represented by:

$$\sum_{i=0}^{63} hi\ DIO(n - i).$$

Extra latency is introduced by certian factors. The data register in FIRO.0, the pipeline register before the format control and the output data register of the processor introduce a total delay of three cycles. D1 represents the variable length input delay (0 to 3 cycles). D2 represents the extra delay (0 to 8 cycles) in the variable length output delay block before partial result addition. Taking these factors into consideration gives the filter ouput term:

$$\sum_{i=0}^{63} hi\ (DIO(n - i - D1 - D2 - 3).$$

where f represents the optional absolute value operation (ABSVAL) performed in the format control blocks. 2^{-G} represents the data scale factor implemented in the barrel shifter blocks. PR(n – 1) is the partial result from the previous processor in a multiprocessor system. PR (n – 1) can be regarded as the sum of all the filter taps preceding FIRO.0. FA represents the format adjustment functions performed on the sum of the partial result and the delayed, scaled sum of all 64 filter tap outputs.

Functional Overview (Continued)

When the format adjust block is bypassed, FA = 1. When there is no partial result input, PR(n – 1) = 0. When no right shifts are performed in the barrel shifter blocks, $2^{-G} = 1$. These conditions, together with variable input and output delays (D1 and D2) set to 0 and no absolute values calculated, result in the familiar convolution equation:

$$DO(n) = \sum_{i=0}^{63} hi\ DIO(n - i - 3).$$

Two-Dimensional Processing: The L64240 performs convolution/correlation of the form:

$$DO(n) = FA \quad PR(n - 1) + 2^{-G0} \bullet f \quad \sum_{i=0}^{3}\sum_{j=0}^{7} hi,j\ DIi(n - j - D2 - 3)$$

$$+2^{-G1} \bullet f \quad \sum_{i=4}^{7}\sum_{j=0}^{7} hi,j\ DIi(n - j - D2 - 3)$$

In a typical system, DIi(n) is the ith output of the L64210/L64211 video shift register and DO(n), which represents the time-domain filter output, is the raster scanned video output from the Multi-Bit Filter. The value of n can be converted to a position in the video image of line length L by:

$$n = Ly + x$$

where x and y are coordinates of the pixel represented by DO in the horizontal and vertical directions.

An 8 x 8 convolution of an image is considered in the equation, where i represents the row and j represents the column in the window in which a pixel is located. DIi(n – j) represents the pixel at location i, j in a moving window at time n. In 2-D processing, the input delay, D1, is always set to 0. The latency (D2 + 3) is the same as that explained in the 1-D case above. hi,j is the active coefficient in FIRi.j.

The convolution process is divided into convolutions in two 4 x 8 windows. f represents the optional absolute value operation on the sum of each of the 32nd order FIR filters. The resulting data may be scaled by right shifts (2^{-G0} and 2^{-G1}) in the barrel shifter blocks. The scaled results are summed with the partial result (PR(n – 1)) from another processor, if any.

FA represents the format adjustment functions performed on resulting data. If the format adjust block is bypassed, FA = 1. Also, if there are no partial results, no absolute values calculated, and G0 = G1 = D2 = 0, the familiar 2-D convolution equation is obtained:

$$DO(n) = \sum_{i=0}^{7}\sum_{j=0}^{7} hi,j\ DIi(n - j - 3).$$

Data I/O

The first 8-tap FIR filter section (FIR0) receives data directly form the first input bus (DI0). The other seven 8-tap filter sections (FIR1-FIR7) receive 8-bit input data from either an external input bus or from the shift register of the previous section. The multiplexer at the input to these sections determines the window shape of the filter. For example, if all multiplexers are set such that all sections receive input from the shift register output of the previous section, then the filter behaves as a 64-tap filter with only the DI0 bus active. When all multiplexers are set such that each of the eight sections receives its input from the eight input buses, then the filter behaves as an 8 x 8 2-D filter. Thus, by selectively setting the multiplexers, it is possible to set the window shape to 1 x 64, 2 x 32, 4 x 16 or 8 x 8.

One-Dimensional Configuration: When the L64240 is configured as a stand-alone 1-D filter, pins PR.0-PR.39 could be left unconnected. The internal partial result bits are automatically set LOW. When higher order 1-D filters are configured with several Multi-Bit Filters, up to 40 bits of partial result can be input to one processor from the output of the previous processor in the chain. The outputs SR0.0-SR0.7 are the data bits residing at FIR.7 delayed by an extra CLK cycle.

These bits are used as the DI0 bus inputs to the next processor in a 1-D chain. In the 1-D configuration, all 40 bits of the output (DO.0-DO.39) are available.

Two-Dimensional Configuration: Normally, an L64210/L64211 would be used to generate the multiline data inputs required for 2-D operation. At least 24 of the 40-bit output and partial result buses are available during 2-D processing. The L64240 uses the saved pins for data input buses. Data input buses DI1 and DI6 share the same package pins as PR.0-PR.7 and PR.8-PR.15, respectively, while data input buses DI3 and DI5 share the same pins with DO.0-DO.7 and DO.8-DO.15, respectively.

Data I/O
(Continued)

When any of the input multiplexors (MUX1 to MUX7) are selected to pass the external input data to the FIR filter sections (FIR1 to FIR7), the corresponding alternate function, if any, is disabled. When part of the PR bus is disabled, the disabled bits are forced internally to zero.

The available inputs and outputs for common configurations are given below:

Configuration	Active Inputs	Active Outputs	Active PR
1 x 64	DI0	DO.39:0	PR.39:0
2 x 32	DI0, DI4	DO.39:0	PR.39:0
4 x 16	DI0, DI2, DI4, DI6	DO.39:0	PR.39:16
8 x 8	All	DO.39:16	PR.39:16

Loading of Coefficients

The L64240 has an 8-bit coefficient input (CI.0 to CI.7). The location of the master register in which the coefficient should be stored is selected by the pins REGADR.0 to REGADR.5. Coefficient loading occurs only when $\overline{WE}$ and $\overline{COEFF}$ are set LOW. The coefficient destination address decoding scheme is summarized in the following table.

Coefficient Address Decoding ($\overline{WE}$ = LOW $\overline{COEFF}$ = LOW)

REGADR.0-REGADR.5	Coefficient (CI.0-CI.7) Destination
0	FIR0.0
1	FIR0.1
2	FIR0.2
3	FIR0.3
4	FIR0.4
5	FIR0.5
6	FIR0.6
7	FIR0.7
8	FIR1.0
9	FIR1.1
•	•
•	•
•	•
62	FIR7.6
63	FIR7.7

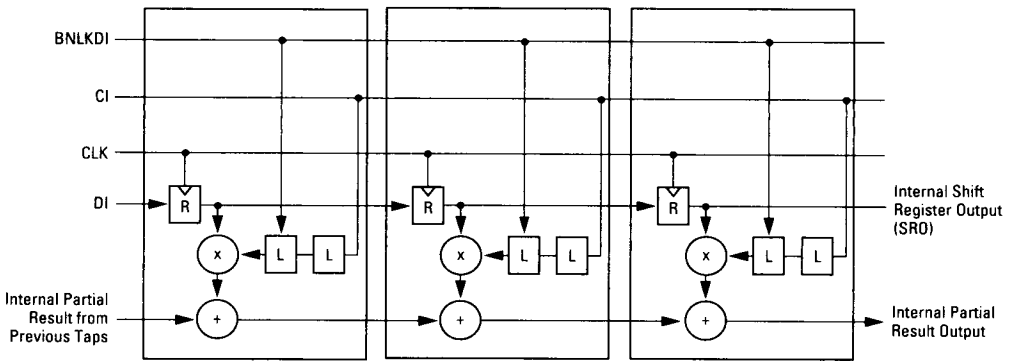
Coefficient Loading: The diagram "3-Cell Filter Section" shows three of the eight filter taps that make up FIR0, FIR1, etc. Coefficients are double-buffered with two level-triggered latches (master and slave) placed before the 8 x 8 multiplier of each cell. The process of providing a valid coefficient to the multiplier of each filter cell consists of first loading the coefficient to the master latch, then transferring it to the slave latch. There are three methods of loading and transferring coefficients. The first method is to load the coefficient to the master latch asynchronously to the system CLK and to transfer it to the slave latch in a manner synchronous to the CLK. The coefficient is loaded into the master latch at the filter location selected by the REGADR.0- REGADR.5 address when COEFF and WE are LOW. This is then repeated for each new coefficient for other filter cells in the processor. When the master latches of all the filter cells have been updated, the coefficients can be bank loaded simultaneously into the multipliers by enabling the slave latches when BLKLDI and CLK are HIGH. The transfer of coefficients from the master to the slave latches is synchronous to the CLK. This is illustrated in the diagram "AC Timing Waveforms – Bank Loading of Controls." This method provides flexibility in the loading of new coefficients into the processor without modifying the active set of coefficients.

The second method is to load and transfer coefficients synchronously to the system clock. This can be done with BNKLDI tied HIGH. WE is set from HIGH to LOW when CLK is LOW. During this time a new coefficient on bus CI is loaded into the master latch of the filter cell whose location has been determined by REGADR.0–REGADR.5. On the next rising edge of CLK the coefficient is transferred to the slave latch, thus loading the active coefficient for the multiplier. In this way a new coefficient can replace the current one within one clock cycle. This can be done only with slower clock speed, cycle times of 80 ns (COM) or more.

The third method is to asynchronously load and transfer new coefficients over several cycles. This technique is used if it is not convenient to supply BNKLDI or WE signals synchronous to CLK. BNKLDI can be tied HIGH and WE operated asynchronously. In this case, every time a new coefficient is loaded the processor output could be invalid for up to 20 cycles after the rising edge of WE.

Loading of Coefficients (Continued)

3-Cell Filter Section



Loading of Control Bits

In addition to acting as input pins coefficient loading, the bus pins CI.0 to CI.7 are also used for loading encoded control bits. COEFF must be HIGH and $\overline{WE}$ must be LOW to load control bits into the processor. The decoding scheme for control bits follows:

Control Bit Map (WE = LOW, COEFF = HIGH)

REGADR.0-REGADR.5	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
0	X	MUXCON.7	MUXCON.6	MUXCON.5	MUXCON.4	MUXCON.3	MUXCON.2	MUXCON.1
1	X	X	32COEFF	$\overline{ABSVAL}$*	$\overline{TCCI}$	$\overline{TCCO}$	TCD1	TCD0
2	X	X	X	BARREL0.0*	BARREL0.4*	BARREL0.3*	BARREL0.2*	BARREL0.1*
3	X	INDEL.1	INDEL.0	BARREL1.0*	BARREL1.4*	BARREL1.3*	BARREL1.2*	BARREL1.1*
4	NEGCLIP*	FORMAT.1*	FORMAT.0*	$\overline{TCO}$*	OUTREG	SAT*	PASS*	X
5	GAIN.0*	GAIN.3*	GAIN.2*	GAIN.1*	OUTDEL.3	OUTDEL.2	OUTDEL.1	OUTDEL.0

In the preceding table, REGADR ≥ 6, while COEFF = HIGH generates an invalid destination address. X means that the state of CI is ignored.

All internal signals marked with * shown in the Control Bit Map table are double-buffered in the same manner as the coefficients, as previously described. All other internal signals are loaded directly. Hence, the loading of these controls is independent of CLK and BNKLDI. These parameters must be set during initialization. Whenever these parameters are changed during filter operation it significantly modifies the processor configuration. During such reconfiguration of the processor, the internal states may be corrupted and the output may not be valid for up to 80 cycles.

The internal signals MUXCON.1 to MUXCON.7 are the select lines for MUX1 to MUX7. When any MUXCON is HIGH, the corresponding MUX select line is set such that external data residing at the input bus pins is transferred to the corresponding 8-tap FIR block.

When LOW, data is transferred from the previous FIR block to the output of the MUX. The following table summarizes various configurations of the L64240 window, which must be set during initialization of the processor.

Typical Window Shapes

MUXCON.1-MUXCON.7	Window Shape	Active Inputs
0000000	1 x 64	D0
0001000	2 x 32	D0,D4
0101010	4 x 16	D0, D2, D4, D6
1111111	8 x 8	All

The preceding are typical configurations of the window shape. Other configurations are possible.

Loading of Control Bits (Continued)

The L64240 supports two's complement, unsigned, or mixed-mode formats for operations with the data and coefficients. The interpretation of the formats is done in the following manner:

Internal Control Signal	State	Data/ Coefficient	Filter Cell Blocks	TC/ Unsigned
TCD0	LOW	Data	FIR0-FIR3	Unsigned
TCD0	HIGH	Data	FIR0-FIR3	TC
TCD1	LOW	Data	FIR4-FIR7	Unsigned
TCD1	HIGH	Data	FIR4-FIR7	TC
TCC0	HIGH	Coefficient	FIR0-FIR3	Unsigned
TCC0	LOW	Coefficient	FIR0-FIR3	TC
TCC1	HIGH	Coefficient	FIR4-FIR7	Unsigned
TCC1	LOW	Coefficient	FIR4-FIR7	TC

When 32COEFF is set HIGH, any coefficient loaded into the master latch of FIRy.x is also loaded into FIR(y + 4).x, where $y \leq 3$, $x \leq 7$, and $x,y \geq 0$. This is a useful feature in some applications where identical coefficients are loaded into both upper and lower halves of the filter. 32COEFF, $\overline{TCC0}$, $\overline{TCC1}$ must all be set before any coefficients are loaded.

INDEL.0, INDEL.1 set the delay (in number of cycles) from bus pins DI0 to the input of FIR0. This must be set during initialization of the system.

INDEL.1	INDEL.0	No. Cycles Input Delay
0	0	0
0	1	1
1	0	2
1	1	3

Internal signal OUTREG selects if the output data register is included in the data path. When OUTREG is HIGH, the output register is bypassed. This is done when using the L64240 as an IIR filter processor. OUTREG must be set during initialization of the system.

Initialization

$\overline{RESET}$ LOW forces all bidirectional pins into a high impedance state and internal coefficients to zero to prevent high static current.

$\overline{RESET}$ should be LOW when the device is powered on. It should be held LOW until the device has been initialized. The device is initialized by loading coefficients 0-63 (page 7) and control words 0-5 (page 8) to the device. Once the device has been initialized, $\overline{RESET}$ should be taken HIGH.

$\overline{RESET}$ must be held HIGH through normal operation of the device and for subsequent loading of new coefficients and control.

BNKLDI is ignored when $\overline{RESET}$ is LOW. BNKLDI must go HIGH after $\overline{RESET}$ goes HIGH to cause the coefficients to become active.

Should the L64240 be powered down for any reason, it must be reinitialized by the procedure described above.

Format Control, Barrel Shifters, and Partial Result Addition

The format control blocks convert the 22-bit sums of the 32 filter tap outputs to a 23-bit two's complement format. The absolute value of the data can be calculated by setting the internal signal ABSVAL LOW.

The L64240 has two barrel shifters (barrel shifter0 and barrel shifter1) which scale the sums of the outputs of the format control blocks. The inputs and outputs of each of the barrel shifters are 40 bits wide. The number of right shifts (0 to 23) are controlled by the internal control signals BARREL0.0– BARREL0.4 in barrel shifter0 and by BARREL1.0– BARREL1.4 in barrel shifter1. The barrel shifter controls should never be set greater than 23.

The L64240 provides a very large dynamic range for the data output. The barrel shifters provide the flexibility of weighting data to handle extended precision computations or to prevent overflow in a multiprocessor system.

The barrel shifter outputs are summed and delayed by the variable length delay block. By setting the internal control signals OUTDEL.0-OUTDEL.3 it is possible to set the variable length delay to delay the data received by 0 to 8 cycles. OUTDEL.0-OUTDEL.3 should not be set greater than 8. When using the L64240 for FIR filter applications it is recommended to set the delay to at least 1 for extra pipelining for maximum performance. Extra delays are required for multiprocessor 2-D applications.

Format Control, Barrel Shifters, and Partial Result Addition (Continued)

The 40-bit output of the variable length delay is added to the two's complement partial result coming from the outputs of another L64240, if any. This may cause the result to exceed the valid range of values (that is, + or – overflow), which sets the OVF output HIGH. Assume that the sign bit of the variable length delay output is MSBa and the sign bit of the partial result bits is MSBb. When the two numbers are added let the MSB of the sum be MSBr. The following table states the conditions when OVF is generated.

Overflow Generation Condition

MSBa	MSBb	MSBr	OVF/UNF	Exception Type
0	0	1	1	+ Overflow
1	1	0	1	- Overflow
All Other Combinations			0	None

When added to the variable length delay output, the partial result bits can be used to vary the brightness of the resulting image. This gives flexibility in varying thresholds (that is, regions of positive and negative values) which can be formatted for video output in the format adjust block described below.

Format Adjustments

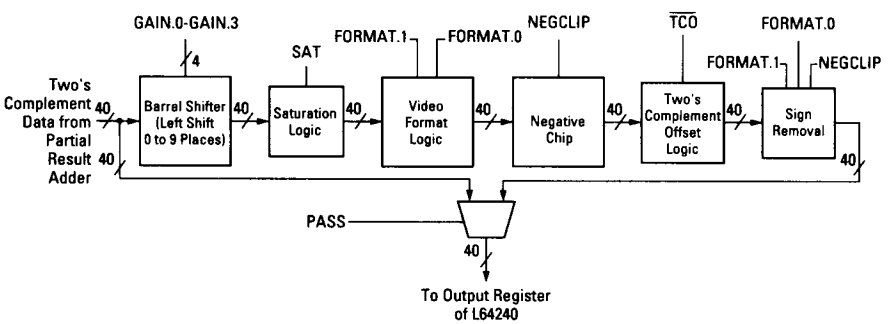
The format adjust block receives 40-bit two's complement data. A block diagram of the architecture of the format adjust block is shown below.

When the latched signal PASS is set HIGH, the format adjust block is bypassed. SAT is reserved for future enhancements and currently must be set HIGH.

The format adjust block has a barrel shifter which provides additional control over the gain of the output. The number of left shifts can be set from 0 to 9 by setting internal signals GAIN.0 to GAIN.3, which should never be set greater than nine. The barrel shifter is useful for normalizing the data or increasing the contrast of video images.

The internal signals FORMAT.1 and FORMAT.0 control the function of the video format logic block as follows:

FORMAT.0	FORMAT.1	Function
0	0	INVERT
1	0	BINCLIP
0	1	FABSVAL
1	1	PASS DATA



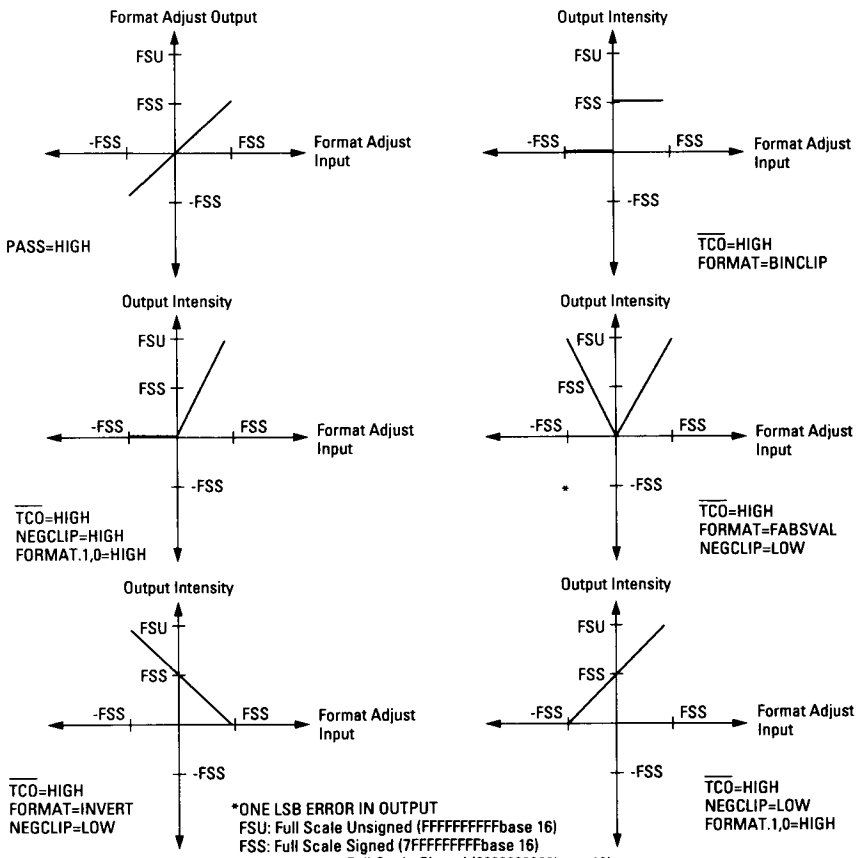
Format Adjustment (Continued)

INVERT simply inverts every bit, which is an approximation to Y= -X. This function makes the light regions of the resulting image dark and the dark regions light. BINCLIP transforms positive outputs from the barrel shifter to 0 and negative outputs to 8000000000 (base 16). This creates binary images. FABSVAL performs the transformation Y= |X|. When performing the absolute value operation, the result will have an error of one LSB (the actual result = the desired result - 1) when data from the barrel shifter is negative.

When FORMAT.1 and FORMAT.0 are HIGH, it is possible to negative clip the output signal. When internal signal NEGCLIP is HIGH, any negative data is replaced by 0.

When $\overline{TCO}$ (two's complement output) is LOW, the output is in two's complement format. When $\overline{TCO}$ is HIGH, the sign bit is inverted to generate an unsigned offset binary output suitable for video display. When this is done in conjunction with the other format adjustments previously described, the effects are illustrated below. Finally, the result is left-shifted one position (thus losing the sign bit) when absolute value and/or negative clipping operations are performed. Hence, the result in both cases is always a positive, unsigned number and the LSB of the output, DO.0, is undefined.

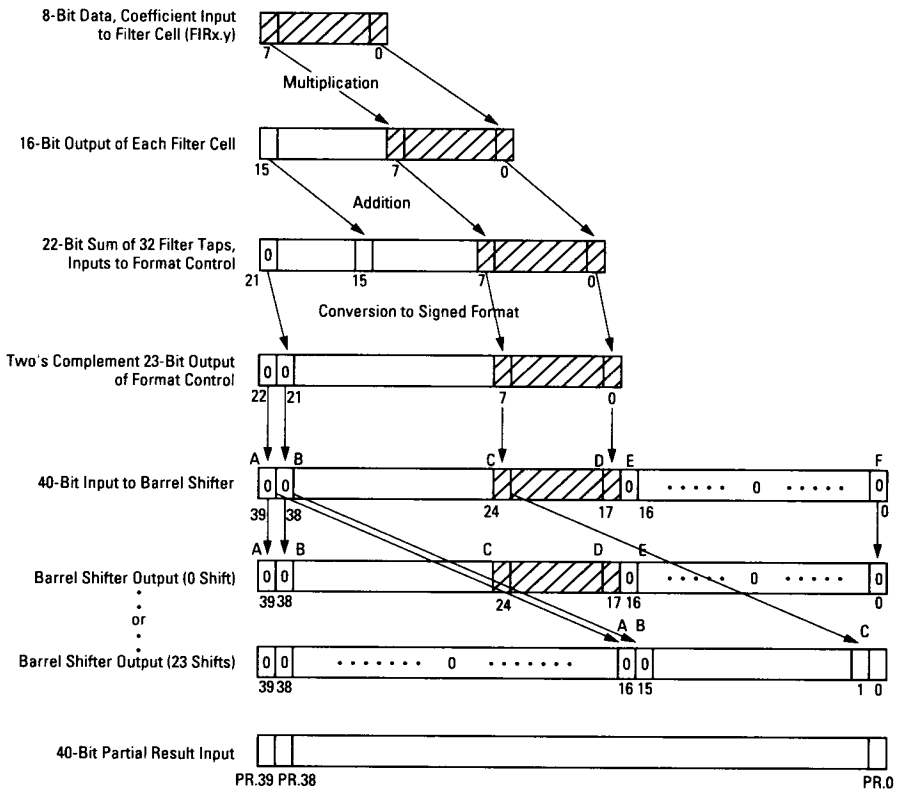
The first partial result in any system is available to provide an offset that will shift all the transfer characteristics (shown below) left or right.



*ONE LSB ERROR IN OUTPUT
FSU: Full Scale Unsigned (FFFFFFFFFFbase 16)
FSS: Full Scale Signed (7FFFFFFFFFbase 16)
-FSS: Negative Full Scale Signed (8000000000base 16)
Assumption: All above examples with (GAIN.0-GAIN.3) = 0

Internal Data Representations

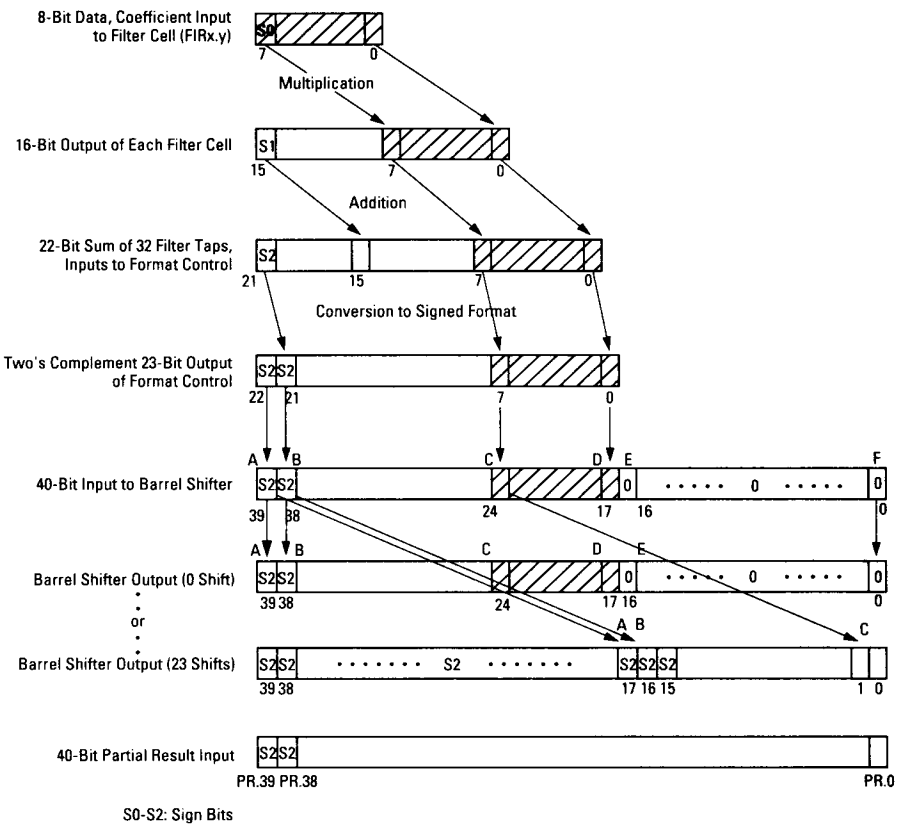
In this section, the size of the operands, filter cell outputs, filter output sums, and the treatment of data in the format control and barrel shifter blocks are illustrated in greater detail. The table shows the effect of right shifting the filter output sums relative to the partial result (assumed to be an unshifted result from another L64240).



Traces the region of interest in the extreme case when the L64240 has only one filter cell with a non-zero coefficient. Inthis case, the non-Zero coefficient has value 1. When multiplied with 8-bit data, the result ends up in bit positions 17-24 at the barrel shifter inputs.

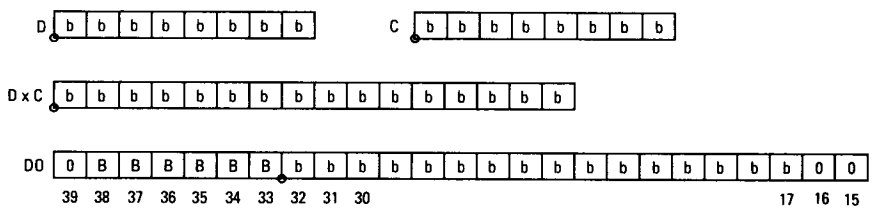
Internal Data Representations (Continued)

Two's Complement Data and Coefficients

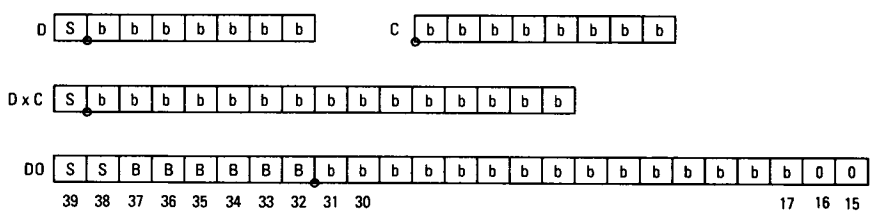


Fractional Data Formats and the L64240

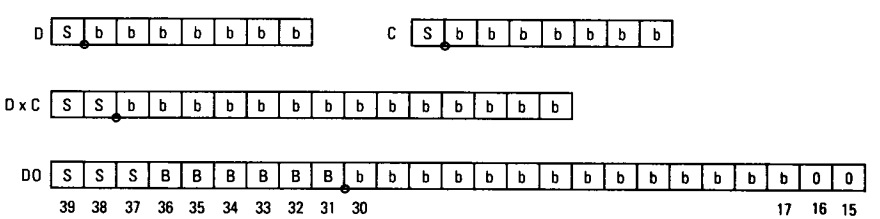
Any combination of fractional signed and unsigned data and coefficients can be handled by the L64240. A fractional number is one in which the magnitude is always strictly less than one. The diagrams below indicate the output format for different combinations of signed and unsigned data and coefficients. In each case, it is assumed that the partial results (PR) are set to zero and no shifting or format adjustment is performed. Because each product (D x C) has magnitude less than one, the output (DO) has magnitude less than 64. The bits marked 'B' are bits that are significant in the worst case (of course if not all multipliers are used, not all of the 'B' bits will be significant).



In unsigned data and coefficient case (above), the output will contain a leading '0' because the output is signed. To remove this '0' the format adjust should be set to NEGCLIP or ABSVAL.



In the case in which one operand is signed and the other is unsigned (above), the output will be signed extended by one bit. This bit can be removed by performing a left shift in the format adjust.



In the signed data and coefficient case (above), the output will be signed extended by two bits. These bits can be removed by performing a left shift in the format adjust.

Other Variations

Extended Precision Operation
If the device is operated as a 32-tap filter (with 16-bit data or coefficients) and the barrel shifters are set to shift by zero and eight places, for each of the cases above, there will be one additional sign bit (the most significant 'B' bit will become a sign extension bit).

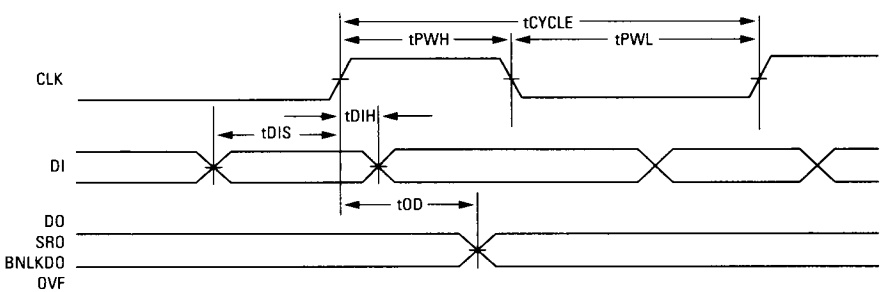
Data Output in Different Bit Positions
The barrel shifters can be used to force the data to come out at different bit positions at the device output. Each right shift will move the binary point and all data bits to the right (towards the LSB) one position. The output will always be sign extended. Each left shift will move the binary point and all data bits to the left (towards the MSB) one position. The output will saturate (clip to largest representable values) if overflow occurs.

Gain Control with Right Shifts in Barrel Shifter1, Barrel Shifter0

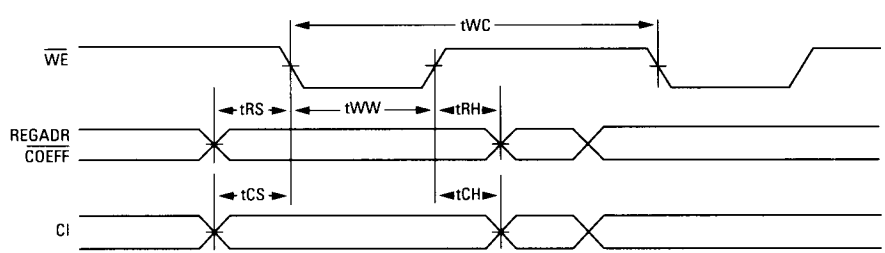
No. of Shifts	Bit A Position	Bit B Position	Bit C Position	Bit D Position	Bit E Position	Bit F Position	Bias of Barrel Shifter Output with Respect to PR
0	39	38	24	17	16	0	2^{0}
1	38	37	23	16	15	Lost	2^{-1}
2	37	36	22	15	14	Lost	2^{-2}
3	36	35	21	14	13	Lost	2^{-3}
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
15	24	23	9	2	1	Lost	2^{-15}
16	23	22	8	1	0	Lost	2^{-16}
17	22	21	7	0	Lost	Lost	2^{-17}
18	21	20	6	Lost	Lost	Lost	2^{-18}
19	20	19	5	Lost	Lost	Lost	2^{-19}
20	19	18	4	Lost	Lost	Lost	2^{-20}
21	18	17	3	Lost	Lost	Lost	2^{-21}
22	17	16	2	Lost	Lost	Lost	2^{-22}
23	16	15	1	Lost	Lost	Lost	2^{-23}

AC Timing Waveforms

Normal Filter Operation

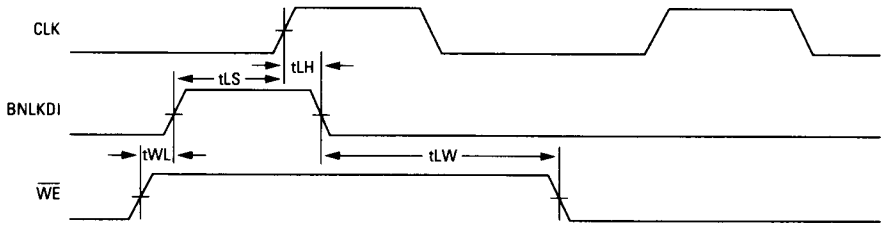


Loading Controls into Master Section (Methods I, II, III)

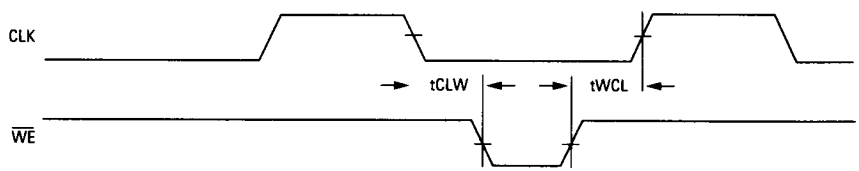


AC Timing Waveforms
(Continued)

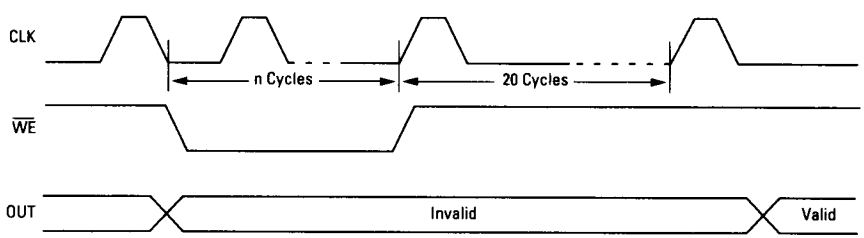
Bank Loading Of Controls–Synchronous Transfer From Master to Slave Registers (Method I)



Synchronous Loading of Master Section and Synchronous Transfer to Slave Section with Bank Load HIGH (Method II)



Asynchronous Loading of Master Section and Asynochronous Transfer to Slave Section with Bank Loads HIGH (Method III)



AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64240-20		L64240-15	
		Min	Max	Min	Max
tCYCLE	Minimum clock (CLK) cycle time	50		65	
tPWH	Minimum clock (CLK) pulse width HIGH	20		25	
tPWL	Minimum clock (CLK) pulse width LOW	20		25	
tDIS	Input data (DI) set-up time	16		22	
tDIH	Input data (DI) hold time	5		7	
tPRS	Input partial result (PR) set-up time	20*		30*	
tPRH	Input partial result (PR) hold time	5		7	
tOUT	Output delay (DO) from CLK		22**		28**
tOD	Output delay (SRO, BNKLDO) from CLK		22**		28**
tLS	BNLKDI set-up time with respect to CLK	15		20	
tLH	BNLKDI hold time with respect to CLK	5		7	
tWL	$\overline{WE}$ set-up time with respect to BNKLDI	5		7	
tLW	$\overline{WE}$ hold time with respect to BNKLDI	tPWH + 15***		tPWH + 20***	
tRS	REGADR set-up time with respect to $\overline{WE}$	10		15	
tRH	REGADR hold time with respect to $\overline{WE}$	10		15	
tCS	CI set-up time with respect to $\overline{WE}$	10		15	
tCH	CI hold time with respect to $\overline{WE}$	10		15	
tWW	Minimum $\overline{WE}$ pulse width LOW	20		25	
tWC	Minimum $\overline{WE}$ cycle time	50		65	
tCLW	CLK before $\overline{WE}$	20		25	
tWCL	CLK after $\overline{WE}$	20		25	

*Assume format adjust block disabled. tPRS = 35 ns (L64240-20) or 45 ns (L64240-15) WCCOM, when format adjust enabled.
**Assume output register enabled.
***tPWH refers to actual Clock Pulse Width HIGH.
All times are in ns, output loading = 50 pF

AC Switching Characteristics: Military (TA = 55°C to 125°C, VDD = 4.75 V to 5.5 V)

Symbol	Parameter	L64240-16		L64240-12	
		Min	Max	Min	Max
tCYCLE	Minimum clock (CLK) cycle time	65		80	
tPWH	Minimum clock (CLK) pulse width HIGH	25		30	
tPWL	Minimum clock (CLK) pulse width LOW	25		30	
tDIS	Input data (DI) set-up time	20		25	
tDIH	Input data (DI) hold time	7		10	
tPRS	Input partial result (PR) set-up time	30*		40*	
tPRH	Input partial result (PR) hold time	7		10	
tOUT	Output delay (DO) from CLK		28**		34**
tOD	Output delay (SRO, BNKLDO) from CLK		28**		34**
tLS	BNLKDI set-up time with respect to CLK	20		30	
tLH	BNLKDI hold time with respect to CLK	7		10	
tWL	$\overline{WE}$ set-up time with respect to BNKLDI	7		10	
tLW	$\overline{WE}$ hold time with respect to BNKLDI	tPWH + 20***		tPWH + 25***	
tRS	REGADR set-up time with respect to $\overline{WE}$	15		20	
tRH	REGADR hold time with respect to $\overline{WE}$	15		20	
tCS	CI set-up time with respect to $\overline{WE}$	15		20	
tCH	CI hold time with respect to $\overline{WE}$	15		20	
tWW	Minimum $\overline{WE}$ pulse width LOW	25		30	
tWC	Minimum $\overline{WE}$ cycle time	65		80	
tCLW	CLK before $\overline{WE}$	25		30	
tWCL	CLK after $\overline{WE}$	25		30	

*Assume format adjust block disabled. tPRS = 45 ns (L64240-16) or 55 ns (L64240-12) WCMIL, when format adjust enabled.
**Assume output register enabled.
***tPWH refers to actual Clock Pulse Width HIGH.
All units in ns, output loading = 50 pF

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to + 7	V
Input voltage	VIN	-0.3 to VDD + 0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to + 150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to + 6	V
Operating ambient temperature range			
Military	TA	-55 to + 125	°C
Commercial	TA	0 to + 70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges (1)

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIL	Low level input voltage				0.8	V
VIH	High level input voltage					
	Commercial temperature range		2.0			V
	Military temperature range		2.25			V
IIN	Input current	VIN = VDD	-150		200	µA

DC Characteristics (Continued): Specified at VDD = 5 V over the specified temperature and voltage ranges [1]

Symbol	Parameter	Condition			Min	Typ	Max	Units
VOH	High level output voltage		Comm	Mil				
		IOH =	-4 mA	-3.2 mA	2.4	4.5		V
VOL	Low level output voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOS	Output short circuit current [2]	VDD = Max, VO = VDD			15		130	mA
		VDD = Max, VO = OV			-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS					10	mA
IDD	Operating supply current	tCYCLE = 50 ns tCYCLE = 65 ns				500 380		mA
CIN	Input capacitance	Any input				5		pF
COUT	Output capacitance	Any output				10		pF

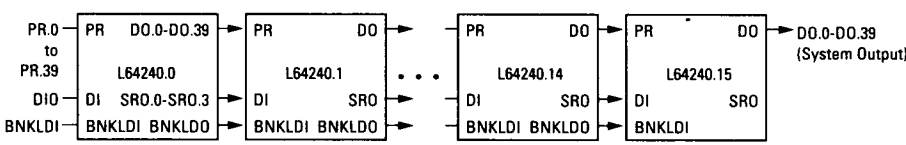
Notes:
1. Military temperature range is -55°C to + 125°C, ± 10% power supply; ± 5% power supply; commercial temperature range is 0°C to 70°C, ± 5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.

Application Examples

The L64240 architecture provides the flexibility of configuring a higher-order FIR system with larger data and coefficient widths. This can be done for both 1-D and 2-D systems by cascading multiple processors, as shown in the following examples.

Example No.1: 1-D System Example
Each processor computes 64 taps of the 1024 taps. The coeffcients of processor L64240 should be loaded with h64i to h64i + 63. BNLKDO of any processor is shown as the input to the succeeding processor. This is done to prevent skews between the coefficients bank loaded into the filter taps and the partial results or input data, both of which encounter an extra cycle of latency in output registers.

1 x 1024 Window, 8-Bit Data, 8-Bit Coefficient



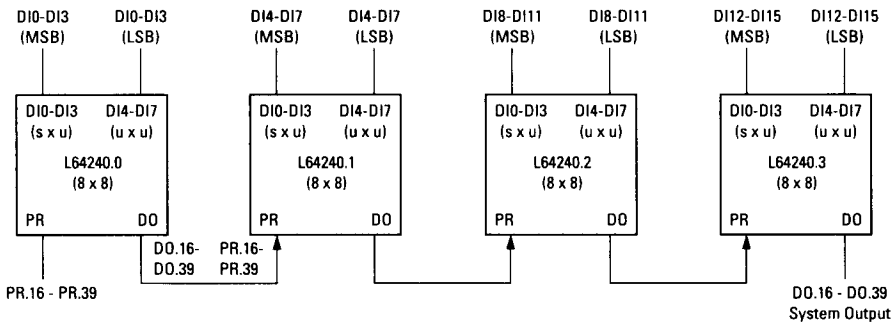
Initialization of System

Device	Pins/Internal Control Signals	Value	Comments
L64240.0	PR.0–PR.39	Constant	Can be set to zero by leaving pins unconnected. Non-zero value useful for format adjustment.
All	BARREL.0–BARREL.4	4	Relative gain of 2^{-4} to prevent saturation of intermediate results.
All	OUTDEL.0–OUTDEL.3	1	One extra pipeline stage.
All	MUXCON.1–MUXCON.7	0	All processors configured for 1-D processing.
All	INDEL.0–INDEL.1	0	
All	32COEFF	0	
All	OUTREG	0	Configures each processor as FIR filter.

Application Examples
(Continued)

Example No.2: 2-D System Example
Each processor computes a FIR filter over a 4 x 8 window with 16-bit data and 8-bit coefficient. The first processor computes the convolution over the top 4 x 8 sub-region of the 16 x 8 window. The other processors similarly compute a convolution over adjacent 4 x 8 sub-regions.

16 x 8 Window, 16-Bit Signed Data, 8-Bit Unsigned Coefficients



Initialization of System

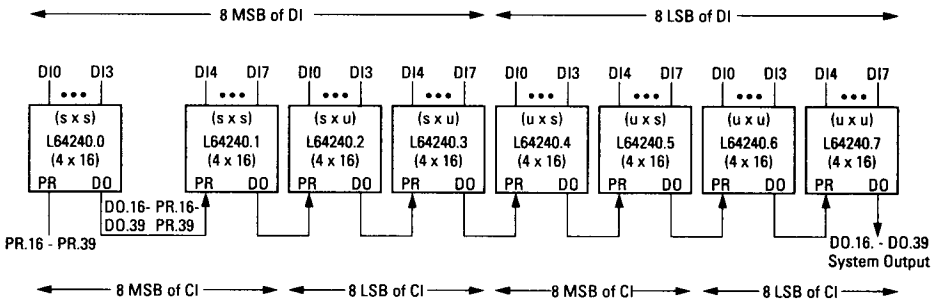
Device	Pins/Internal Control Signals	Value	Comments
L64240.0	PR.16–PR.39	Constant	Can be set to zero by having pins unconnected. Non-zero value useful for format adjustment.
L64240.0	BAREL1.0–BAREL1.4	10	Relative gain of 2^{-10} (LSB x coefficient).
L64240.0	BAREL0.0–BAREL0.4	2	Relative gain of 2^{-2}. Extra right shift prevents saturation of internal results (MSB x coefficient).
L64240.1	BAREL1.0–BAREL1.4	10	
L64240.1	BAREL0.0–BAREL0.4	2	
L64240.2	BAREL1.0–BAREL1.4	10	
L64240.2	BAREL0.0–BAREL1.4	2	
L64240.3	BAREL1.0–BAREL1.4	10	
L64240.3	BAREL0.0–BAREL0.4	2	
L64240.0	OUTDEL.0–OUTDEL.3	1	1-cycle delay introduced in variable length delay.
L64240.1	OUTDEL.0–OUTDEL.3	2	2-cycle delay.
L64240.2	OUTDEL.0–OUTDEL.3	3	3-cycle delay.
L64240.3	OUTDEL.0–OUTDEL.3	4	4-cycle delay.
All	MUXCON.1–MUXCON.7	127	Configures each processor as 2-D (8 x 8) filter.
All	INDEL.0–INDEL.1	0	
All	32COEFF	1	This scheme halves the number of cycles needed to load coefficients.
All	OUTREG	0	Configures each processor as FIR filter.
All	BNKLDI		Tied together.
All	$\overline{\text{BNKLDO}}$		Unconnected.
All	$\overline{\text{TCC1}}$	1	Unsigned coefficients.
All	TCC0	1	Unsigned coefficients.
All	TCD1	1	MSB data signed.
All	TCD0	0	LSB data unsigned.
L64240.0	h0.0–h3.7	C0.0–C3.7	First 4 x 8 block of coefficients.
L64240.1	h0.0–h3.7	C4.0–C7.7	Second 4 x 8 block of coefficients.
L64240.2	h0.0–h3.7	C8.0–C11.7	Third 4 x 8 block of coefficients.
L64240.3	h0.0–h3.7	C12.0–C15.7	Fourth 4 x 8 block of coefficients.

Application Examples
(Continued)

Example No. 3: 2-D System Example

Each consecutive pair of processors computes the convolution over the entire 8 x 16 window with different 8-bit segments of the data and coefficients. The first pair works with the MSB data and coefficients, the second with the MSB data and LSB coefficients, and so on. The data and coefficient formats (signed [s] or unsigned [u]) are shown inside each processor block.

8 x 16 Window, 16-Bit Signed Data, 16-Bit Signed Coefficients



In both 2-D examples, the data outputs of on processor are connected to the partial result inputs of the next processor. The presence of the output data registers causes an extra delay of one cycle. Therefore, in a given processor the latency of the partial result input is greater than that of the barrel shifter output sum by one cycle. To compensate for this it is necessary to provide an extra cycle of latency to the barrel shifter output sum. Since the variable length delay provides a maximum of eight extra cycles of delay, a maximum of eight processors can be cascaded in a variety of 2-D configurations.

For any of the processor examples shown, PASS can be set according to user's choice, thus including the corresponding format adjust block in the data path. In this case, the rest of the format adjust internal control signals are recommended to be set during initialization of the system. These signals could be given new values during processing. Since each processor is using all 64 filter taps, the user must be careful since a left shift of data in the format adjust block of preceding processors could cause the result to overflow in successive processors. Therefore, it is recommended that left shifts during format adjustment be done only in the last processor, provided the nature of data and coefficients are such that positive or negative fullscale results have not been generated already. This prevents the unnecessary loss of MSBs during left shift.

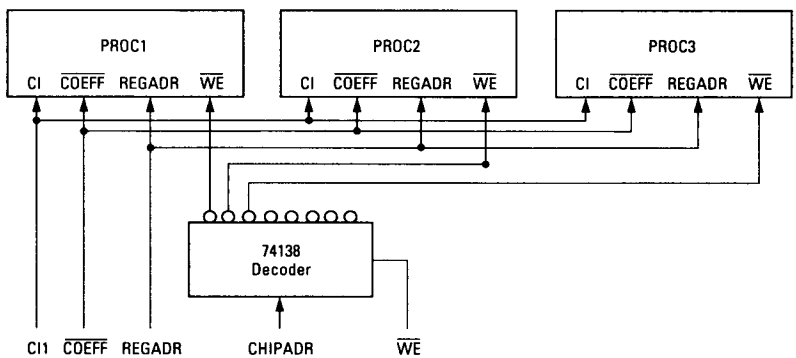
Application Examples **Initialization of System**
(Continued)

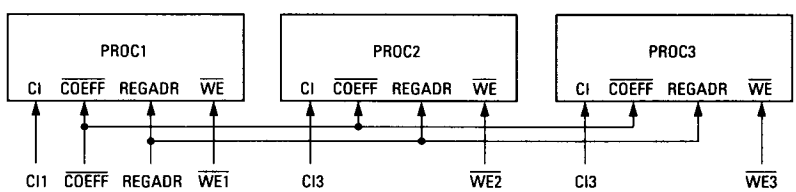
Device	Pins/Internal Control Signals	Value	Comments
L64240.0	PR.16–PR.39	Constant	Set to zero by unconnected pins.
L64240.0–L64240.1	BARREL.0–BARREL.4	3	Relative gain of 2^{-3}. Extra shift to prevent saturation of intermediate results.
L64240.2–L64240.5	BARREL.0–BARREL.4	11	Relative gain of 2^{-11}.
L64240.6–L64240.7	BARREL.0–BARREL.4	19	Relative gain of 2^{-19}.
L64240.0	OUTDEL.0–OUTDEL.3	1	One cycle extra delay.
L64240.1	OUTDEL.0–OUTDEL.3	2	Two cycles.
L64240.2	OUTDEL.0–OUTDEL.3	3	Three cycles.
L64240.3	OUTDEL.0–OUTDEL.3	4	Four cycles.
L64240.4	OUTDEL.0–OUTDEL.3	5	Five cycles.
L64240.5	OUTDEL.0–OUTDEL.3	6	Six cycles.
L64240.6	OUTDEL.0–OUTDEL.3	7	Seven cycles.
L64240.7	OUTDEL.0–OUTDEL.3	8	Eight cycles.
All	MUXCON.1–MUXCON.7	42	Configures each processor for (4 x 16) window.
All	INDEL.0–INDEL.1	0	
All	32COEFF	0	
All	OUTREG	0	Configures each processor as FIR filter.
All	BNKLDI		Tied together.
All	BNKLDO		Unconnected.
L64240.0–L64240.3	TCD0,TCD1	1	
L64240.4–L64240.7	TCD0,TCD1	0	
L64240.0, L64240.1, L64240.4, L64240.5	$\overline{TCC0}$,$\overline{TCC1}$	0	
L64240.2, L64240.3 L64240.6, L64240.7	$\overline{TCC0}$, $\overline{TCC1}$	1	
L64240.0 L64240.4	h0.0–h7.7	MSB of C0.0–C3.15	MSB of first 4 x 16 block of coefficients.
L64240.1 L64240.5	h0.0–h7.7	MSB of C4.0–C7.15	MSB of second 4 x 16 block of coefficients.
L64240.2 L64240.6	h0.0–h7.7	LSB of C0.0–C3.15	LSB of first 4 x 16 block of coefficients.
L64240.3 L64240.7	h0.0–h7.7	MSB of C4.0–C7.15	LSB of second 4 x 16 block of coefficients.

Application Examples (Continued)

In a multiprocessor system, the user has some added flexibility in the amount of time it will take to change the operating parameters of the system. For example, the CI, REGADR, COEFF and WE inputs for all processors could be connected as shown in the following illustrations, In the first case, each chip is initialized in succession and the total time to initialize the system increases with the number of processors. This solution is suitable for applications requiring operating parameters to change infrequently.

Another solution would be to connect the signals as shown in the second case. In this case, one parameter of each processor can be changed each cycle, keeping the total initialization time to a minimum. Adaptive filters that have a high coefficient update rate could benefit from this configuration.





Pinout Diagram **155-Pin Ceramic Pin Grid Array**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A		VSS	DI2.2	DI2.5	PR.16	PR.19	PR.22	VSS	VDD	PR.27	PR.30	PR.33	PR.36	PR.39	VDD	VSS
B	VDD	OVF	DO2.1	DI2.4	DI2.7	PR.18	PR.21	PR.24	PR.25	PR.28	PR.31	PR.34	PR.37	DI4.0	DI4.1	VDD
C	CI.0	DI0.7	DI2.0	DI2.3	DI2.6	PR.17	PR.20	PR.23	PR.26	PR.29	PR.32	PR.35	PR.38	DI4.2	DI4.2	DI6.0 PR.8
D	CI.3	CI.2	CI.1											DI6.1 PR.9	DI6.2 PR.10	DI6.3 PR.11
E	CI.6	CI.5	CI.4											DI7.4 SRO.4	DI6.5 PR.13	DI6.6 PR.14
F			CI.7											DI7.1 SRO.1	DI4.4	DI4.5
G	REG ADR.0	$\overline{\text{RESET}}$												DI4.6	DI4.7	DI0.0
H	VSS	REG-ADR.2	REG-ADR.1											DI0.2	DI0.4	VSS
J	VDD	REG-ADR.3	REG-ADR.4					Top View Cavity Down						DI0.1	DI0.6	VDD
K	REG-ADR.5	$\overline{\text{COEFF}}$	$\overline{\text{WE}}$											DI7.7 SRO.7	DI0.5	DI0.3
L	DI1.0 PR.0	DI1.1 PR.1	DI1.2 PR.2											DI7.4 SRO.4	DI7.5 SRO.5	DI7.6 SRO.6
M	DI1.3 PR.3	DI1.4 PR.4	DI1.5 PR.5											DI7.1 SRO.1	DI7.2 SRO.2	DI7.3 SRO.3
N	DI1.6 PR.6	DI1.7 PR.7	DO.33											BNKLDO	BNKLDI	DI7.0 SRO.0
P	DO.32	DO.34	DO.35	DO.38	DO.18	DI3.0 DO.0	DI3.0 DO.0	DI3.0 DO.0	DO.21	DO.24	DO.27	DO.30	DI5.1 DO.9	DI3.0 DO.0	DI5.7 DO.15	CLK
R	VSS	DO.36	DO.37	DO.16	DI3.0 DO.0	DI3.0 DO.0	DI3.0 DO.0	DO.19	DO.20	DO.23	DO.26	DO.29	DI5.0 DO.8	DI3.0 DO.0	DI5.6 DO.14	VSS
T	VDD	VSS	DO.39	DO.17	DI3.1 CO.1	DI3.1 CO.1	VSS	VDD	VSS	DO.22	DO.25	DO.28	DO.31	DI3.1 CO.1	DI5.4 DO.12	VDD

Packaging

155-Pin Grid Array Ceramic Cavity Down Package: See FR Package in Package Selector Guide

Ordering Information