

HI-8282

ARINC 429 SERIAL TRANSMITTER AND DUAL RECEIVER

General Description

The HI-8282 is a silicon gate CMOS device for interfacing the ARINC 429 serial data bus to a 16-bit parallel data bus. Two receivers and an independent transmitter are provided. The receiver input circuitry and logic are designed to meet the ARINC 429 specifications for loading, level detection, timing, and protocol. The transmitter section provides the ARINC 429 communication protocol, and requires additional interface circuitry to translate the 5 volt logic outputs to ARINC 429 drive levels.

The 16-bit parallel data bus exchanges the 32-bit ARINC data word in two steps when either loading the transmitter or interrogating the receivers. The data bus interfaces with CMOS and TTL.

Timing of all the circuitry begins with the master clock input, CLK. For ARINC 429 applications, the master clock frequency is 1 MHz.

Each independent receiver monitors the data stream with a sampling rate 10 times the data rate. The sampling rate is selectable at either 1MHz or 125KHz. The results of a parity check are available as the 32nd ARINC bit. The HI-8282 examines the null and data timings and will reject erroneous patterns. For example, with a 125 KHz clock selection, the data frequency must be between 10.4 KHz and 15.6 KHz.

The transmitter has a First In, First Out (FIFO) memory to store 8 ARINC words for transmission. The data rate of the transmitter is selectable as either divide by 10 or divide by 80 from the master clock. The master clock is used to set the timing of the ARINC transmission within the required resolution.

The transmitter and receiver functions are each macrocells in Holt's semicustom library and are available to create other chips incorporating the ARINC interface.

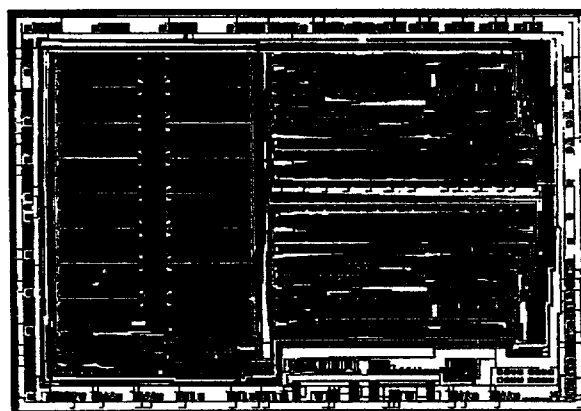
Features

- ARINC Specification 429 Compatible
- 16-Bit Parallel Data Bus
- Direct Receiver Interface to ARINC Bus
- Timing Control 10 Times the Data Rate
- Selectable Data Clocks
- Receiver Error Rejection Per ARINC Specification 429
- Automatic Transmitter Data Timing
- Self Test Mode
- Parity Functions
- Low Power, Single 5 Volt Supply
- Full Military Temperature

Applications

- Avionics Data Communication
- Serial to Parallel Conversion
- Parallel to Serial Conversion

Chip Topography



Pin Configuration

Vcc	1	40	NC
(Rec. 1 Input) 429DI1(A)	2	39	MR (Master Reset)
(Rec. 1 Input) 429DI1(B)	3	38	TX CLK (Xmit Clock Out)
(Rec. 2 Input) 429DI2(A)	4	37	CLK (Master Clock In)
(Rec. 2 Input) 429DI2(B)	5	36	NC
(Rec. 1 Data Flag) D/R1	6	35	NC
(Rec. 2 Data Flag) D/R2	7	34	CWSTR (Control Word Strobe)
(Rec. Byte Select) SEL	8	33	ENTX (Enable Xmit)
(Rec. 1 Output Enable) EN1	9	32	429DO (Xmit Data)
(Rec. 2 Output Enable) EN2	10	31	429DO (Xmit Data)
BD15	11	30	TX/R (Xmit Ready Flag)
BD14	12	29	PL2 (Xmit Byte 2 LE)
BD13	13	28	PL1 (Xmit Byte 1 LE)
BD12	14	27	BD00
BD11	15	26	BD01
BD10	16	25	BD02
BD09	17	24	BD03
BD08	18	23	BD04
BD07	19	22	BD05
BD06	20	21	GND

HOLT INC
INTEGRATED CIRCUITS

Pin Descriptions

SYMBOL	FUNCTION	DESCRIPTION	SYMBOL	FUNCTION	DESCRIPTION
VCC	POWER	+5V $\pm$ 5%	BD05	I/O	Data bus
429DI1(A)	INPUT	ARINC receiver 1 positive input.	BD04	I/O	Data bus
429DI1(B)	INPUT	ARINC receiver 1 negative input.	BD03	I/O	Data bus
429DI2(A)	INPUT	ARINC receiver 2 positive input.	BD02	I/O	Data bus
429DI2(B)	INPUT	ARINC receiver 2 negative input.	BD01	I/O	Data bus
$\overline{D/R1}$	OUTPUT	Receiver 1 data ready flag.	BD00	I/O	Data bus
$\overline{D/R2}$	OUTPUT	Receiver 2 data ready flag.	$\overline{PL1}$	INPUT	Latch enable for byte 1 entered from data bus to transmitter FIFO.
SEL	INPUT	Receiver data byte selection. 0 = BYTE 1 1 = BYTE 2	$\overline{PL2}$	INPUT	Latch enable for byte 2 entered from data bus to transmitter FIFO. Must follow $\overline{PL1}$.
$\overline{EN1}$	INPUT	Data bus control, enables receiver 1 data to outputs.	TX/R	OUTPUT	Transmitter ready flag. Goes low when ARINC word loaded into FIFO. Goes high after transmission and FIFO empty.
$\overline{EN2}$	INPUT	Data bus control, enables receiver 2 data to outputs if $\overline{EN1}$ is high.	429DO	OUTPUT	"ONES" data output from transmitter.
BD15	I/O	Data bus	$\overline{429DO}$	OUTPUT	"ZEROES" data output from transmitter.
BD14	I/O	Data bus	ENTX	INPUT	Enable Transmission.
BD13	I/O	Data bus	$\overline{CWSTR}$	INPUT	Clock for control word register.
BD12	I/O	Data bus	CLK	INPUT	Master Clock input.
BD11	I/O	Data bus	TX CLK	OUTPUT	Transmitter Clock equal to Master Clock (CLK), divided by either 10 or 80.
BD10	I/O	Data bus	$\overline{MR}$	INPUT	Master Reset, active low.
BD09	I/O	Data bus			
BD08	I/O	Data bus			
BD07	I/O	Data bus			
BD06	I/O	Data bus			
GND	POWER	0V			

Functional Description

Control Word Register

The HI-8282 contains 10 data flip flops whose D inputs are connected to the data bus and clocks connected to $\overline{CWSTR}$. Each flip flop provides options to the user as follows:

CONTROL WORD			
DATA BUS PIN	FUNCTION	CONTROL	DESCRIPTION
BD05	Self Test	0 = Enable	If enabled, an internal connection is made passing 429DO and 429DO to the receiver logic inputs.
BD06	Receiver 1 Decoder	1 = Enable	If enabled, ARINC bits 9 and 10 must match the next two control word bits.
BD07	—	—	If Receiver 1 Decoder is enabled, then ARINC bit 9 must match this bit.
BD08	—	—	If Receiver 1 Decoder is enabled, then ARINC bit 10 must match this bit.
BD09	Receiver 2 Decoder	1 = Enable	If enabled, ARINC bits 9 and 10 must match the next two control word bits.
BD10	—	—	If Receiver 2 Decoder is enabled, then ARINC bit 9 must match this bit.
BD11	—	—	If Receiver 2 Decoder is enabled, then ARINC bit 10 must match this bit.
BD12	Invert XMTR Parity	1 = Enable	Logic 0 enables normal odd parity and Logic 1 enables even parity output in transmitter 32nd bit.
BD13	XMTR Data Clock Select	0 = +10 1 = +80	CLK is divided either by 10 or 80 to obtain XMTR data clock.
BD14	RCVR Data Clock Select	0 = +10 1 = +80	CLK is divided either by 10 or 80 to obtain RCVR data clock.

ARINC 429 Data Format

The following table shows the bit positions in exchanging data with the receiver or the transmitter. ARINC bit 1 is the first bit transmitted or received.

BYTE 1															
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01
ARINC BIT	13	12	11	10	9	31	30	32	1	2	3	4	5	6	7

BYTE 2															
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01
ARINC BIT	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15

The Receivers

ARINC Bus Interface

Figure 1 shows the input circuit for each receiver.

The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
One	+6.5V to +13V
Null	+2.5V to -2.5V
Zero	-6.5V to -13V

The HI-8282 guarantees recognition of these levels with a common mode voltage with respect to GND less than $\pm 4V$ for the worst case condition (4.75V supply and 13V signal level). This is equivalent to $\pm 17V$ with respect to GND.

The tolerances in the design guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

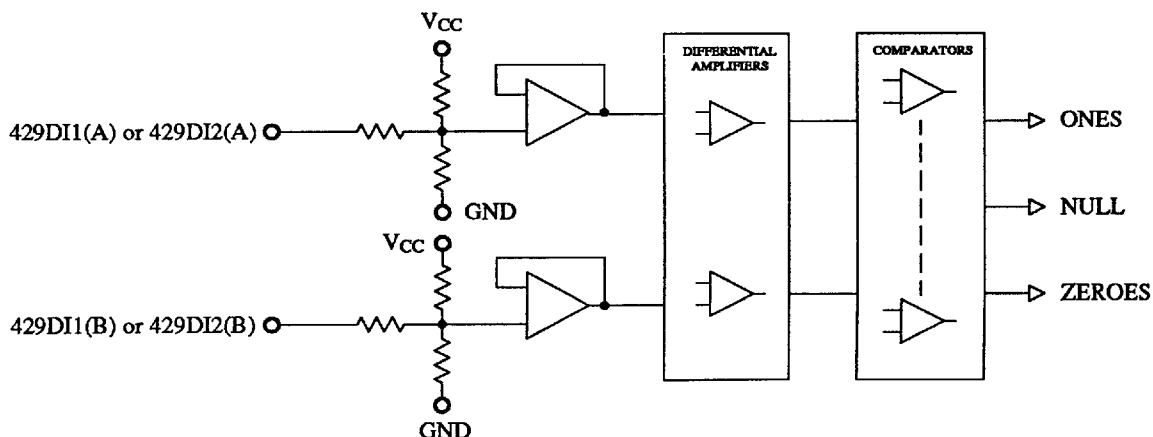


FIGURE 1. ARINC RECEIVER INPUT

Functional Description (cont.)

Receiver Logic Operation

Figure 2 shows a block diagram of the logic section of each receiver.

Bit Timing

The ARINC 429 specification contains the following timing specification for the received data:

	<u>HIGH SPEED</u>	<u>LOW SPEED</u>
Bit Rate	100K BPS $\pm$ 1%	12K - 14.5K BPS
Pulse Rise Time	1.5 $\pm$ 0.5 μ sec	10 $\pm$ 5 μ sec
Pulse Fall Time	1.5 $\pm$ 0.5 μ sec	10 $\pm$ 5 μ sec
Pulse Width	5 μ sec $\pm$ 5%	34.5 to 41.7 μ sec

Again, the HI-8282 accepts signals that meet these specifications and rejects outside the tolerances. The way the logic operation achieves this is described below:

1. Key to the performance of the timing checking logic is an accurate 1MHz clock source. Less than 0.1% error is recommended.
2. The sampling shift registers are 10 bits long and must show three consecutive Ones, Zeros or Nulls to be considered valid data. Additionally, for data bits, the One or Zero in the upper bits of the sampling shift registers must be followed by a Null in the lower bits within the data bit time. For a Null in the Word Gap, three consecutive Nulls must be found in both the upper and lower bits of the sampling shift register. In this manner the minimum pulse width is guaranteed.
3. Each data bit must follow its predecessor by not less than 8 samples and no more than 12 samples. In this manner the bit rate is checked. With exactly 1MHz input clock frequency, the acceptable data bit rates are as follows:

	<u>HIGH SPEED</u>	<u>LOW SPEED</u>
Data Bit Rate Min.	83K BPS	10.4K BPS
Data Bit Rate Max.	125K BPS	15.6K BPS

4. The Word Gap timer samples the Null shift register every 10 input clocks (80 for low speed) after the last data bit of a valid reception. If the Null is present, the Word Gap counter is incremented. A count of 3 will enable the next data reception.

Receiver Parity

The receiver parity circuit counts Ones received, including the parity bit, ARINC bit 32. If the result is odd, then "0" will appear in the 32nd bit.

Retrieving Data

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). If the receiver decoder is enabled and the 9th and 10th ARINC bits match the control word program bits or if the receiver decoder is disabled, then EOS clocks the data ready flag flip flop to a "1". $\overline{D/R1}$ or $\overline{D/R2}$ (or both) will go low. The data flag for a receiver will remain low until after both ARINC bytes from that receiver are retrieved. This is accomplished by activating $\overline{EN}$ with SEL, the byte selector, low to retrieve the first byte and activating $\overline{EN}$ with SEL high to retrieve the second byte. $\overline{EN1}$ retrieves data from receiver 1 and $\overline{EN2}$ retrieves data from receiver 2.

If another ARINC word is received, and a new EOS occurs before the two bytes are retrieved, the data is overwritten by the new word.

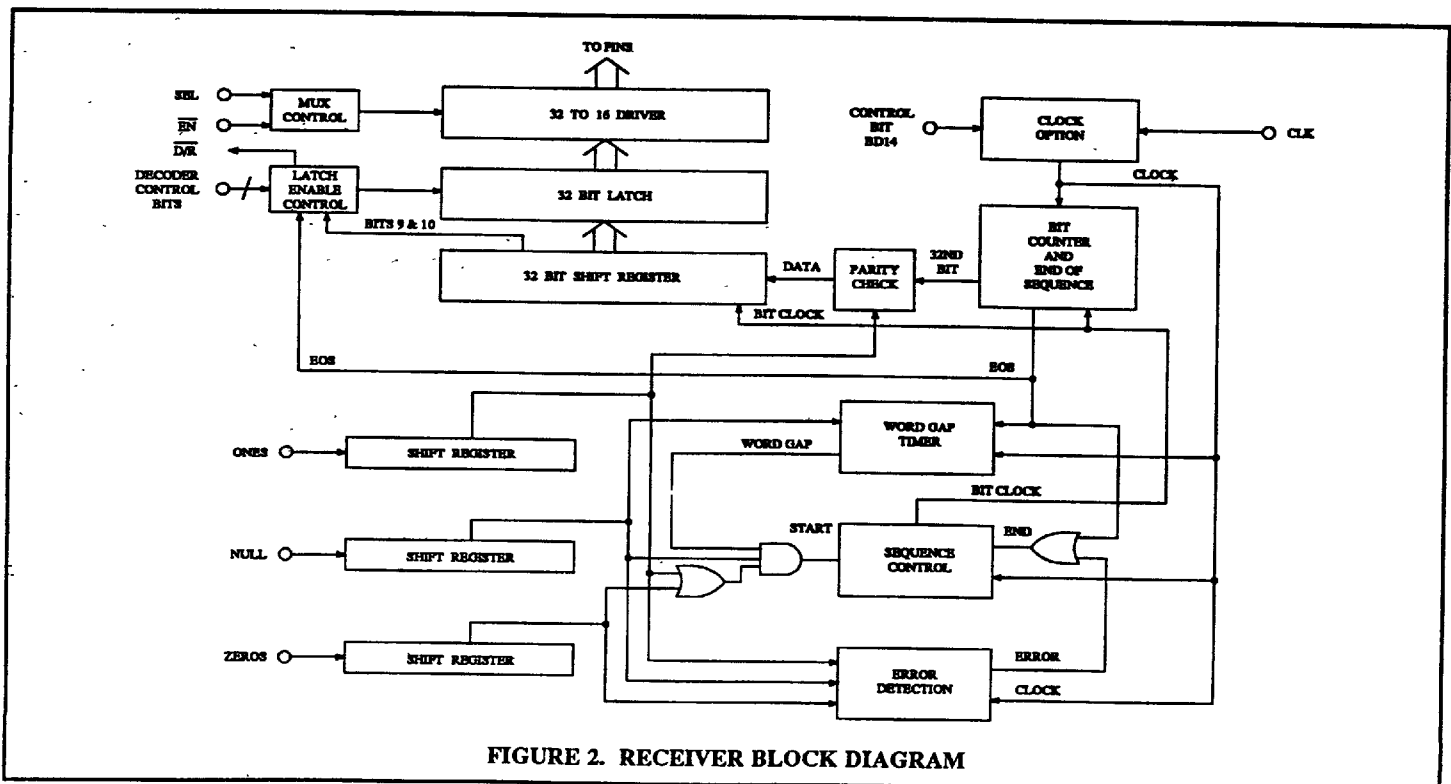


FIGURE 2. RECEIVER BLOCK DIAGRAM

Transmitter

A block diagram of the transmitter section is shown in Figure 3.

FIFO Operation

The FIFO is loaded sequentially by first pulsing $\overline{PL1}$ to load byte 1 and then $\overline{PL2}$ to load byte 2. The control logic automatically loads the 31 bit word in the next available position of the FIFO. If TX/R, the transmitter ready flag is high (FIFO empty), then 8 words, each 31 bits long, may be loaded. If TX/R is low, then only the available positions may be loaded. If all 8 positions are full, the FIFO ignores further attempts to load data.

Data Transmission

When ENTX goes high, enabling transmission, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at either 429DO or 429DO. The 31 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

	HIGH SPEED	LOW SPEED
ARINC Data Bit Time	10 Clocks	80 Clocks
Data Bit Time	5 Clocks	40 Clocks
Null Bit Time	5 Clocks	40 Clocks
Word Gap Time	40 Clocks	320 Clocks

The word counter detects when all loaded positions are transmitted and sets the transmitter ready flag, TX/R, high.

Transmitter Parity

The parity generator counts the Ones in the 31-bit word. If the BD12 control word bit is set low, the 32nd bit transmitted will make parity odd. If the control bit is high the parity is even.

Self Test

If the BD05 control word bit is set low, 429DO or 429DO become inputs to the receiver bypassing the interface circuitry.

System Operation

The two receivers are independent of the transmitter. Therefore, control of data exchanges are strictly at the option of the user. The only restrictions are:

1. The received data may be overwritten if not retrieved within one ARINC word cycle.
2. The FIFO can store 8 words maximum and ignores attempts to load additional data if full.
3. Byte 1 of the transmitter data must be loaded first.
4. Either byte of the received data may be retrieved first. Both bytes must be retrieved to clear the data ready flag.
5. After ENTX, transmission enable, goes high, it cannot go low until TX/R, transmitter ready flag, goes high. Otherwise, one ARINC word is lost during transmission.

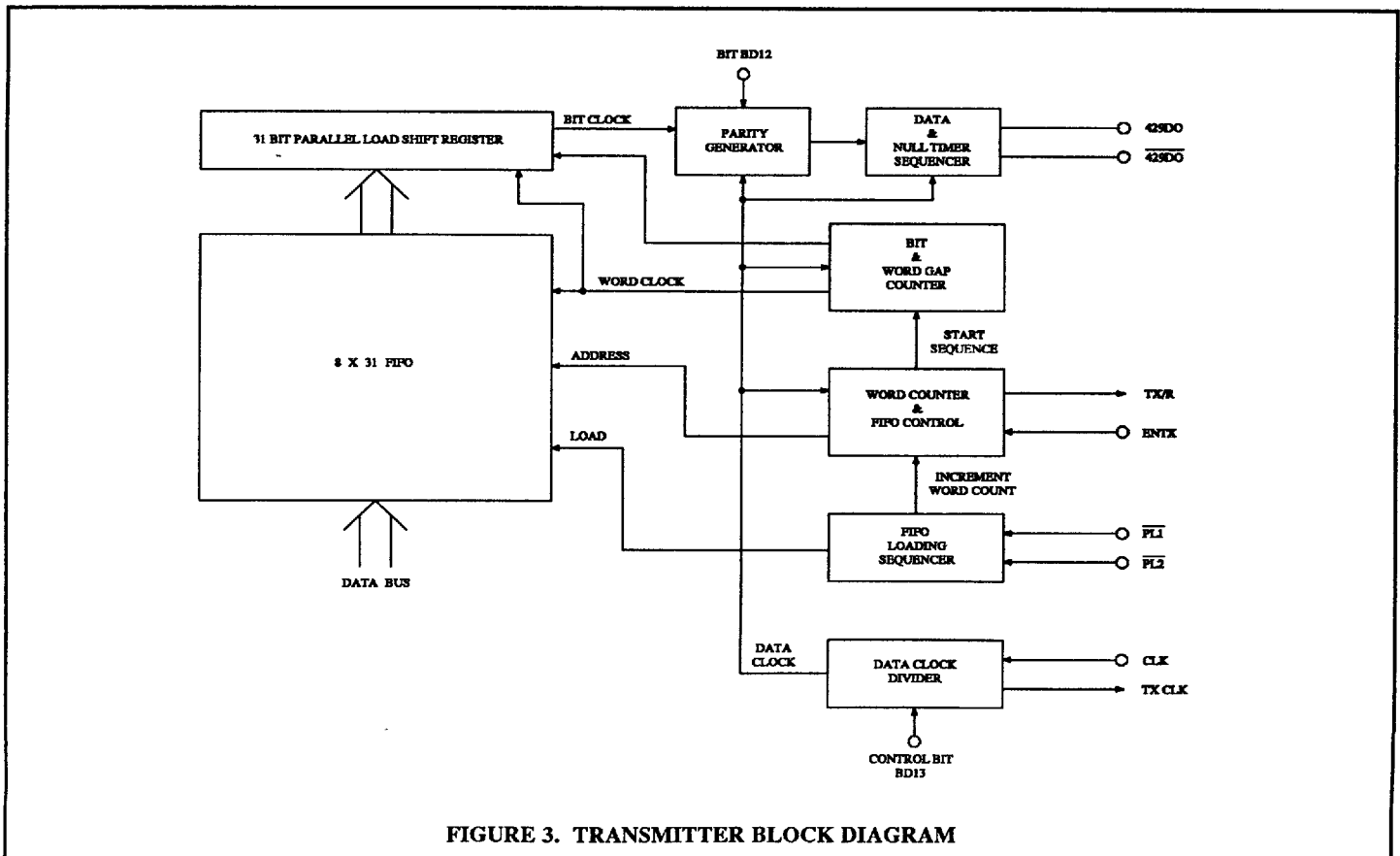


FIGURE 3. TRANSMITTER BLOCK DIAGRAM

Functional Description (cont.)

Repeater Operation

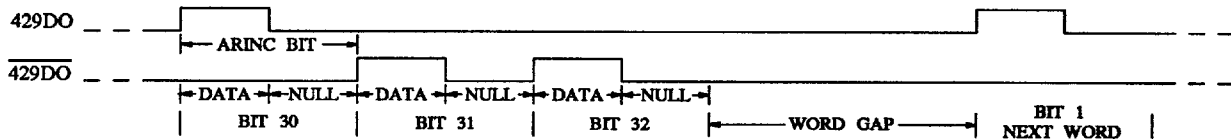
The repeater mode of operation allows a data word that has been received by the HI-8282 to be placed directly into its FIFO for transmission. After a 32-bit word has been shifted into the receiver shift register, the $\overline{D/R}$ flag will go low. A logic "0" is placed on the SEL line and $\overline{EN}$ is strobed. This is the same procedure as for normal receiver operation and it places the lower byte (16 bits) of the data word on the data bus. By strobing $\overline{PL1}$ at the same time as $\overline{EN}$, the byte will also be placed into the transmitter FIFO. SEL is then taken high and $\overline{EN}$ is strobed again to place the upper byte of the

data word on the data bus. By strobing $\overline{PL2}$ at the same time as $\overline{EN}$, the second byte will also be placed into the FIFO. The data word is now ready to be transmitted according to the parity programmed into the control word register.

In normal operation, either byte of a received data word may be read from the receiver latches first by use of the SEL input. During repeater operation however, the lower byte of the data word must be read first. This is necessary because, as the data is being read, it is also being loaded into the FIFO and the transmitter FIFO is always loaded with the lower byte of the data word first.

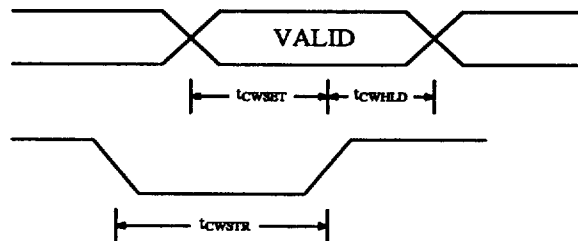
Timing Diagrams

DATA RATE - EXAMPLE PATTERN

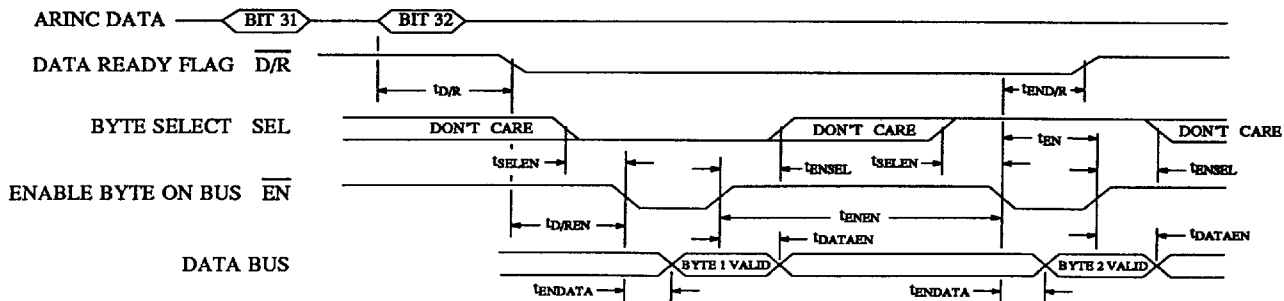


LOADING CONTROL WORD

DATA BUS

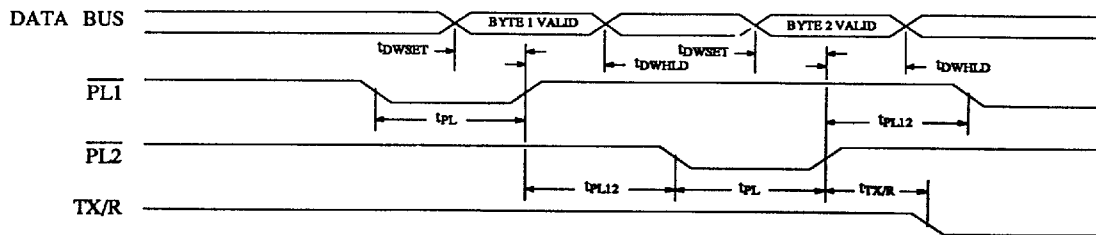
 $\overline{CWSTR}$ 

RECEIVER OPERATION

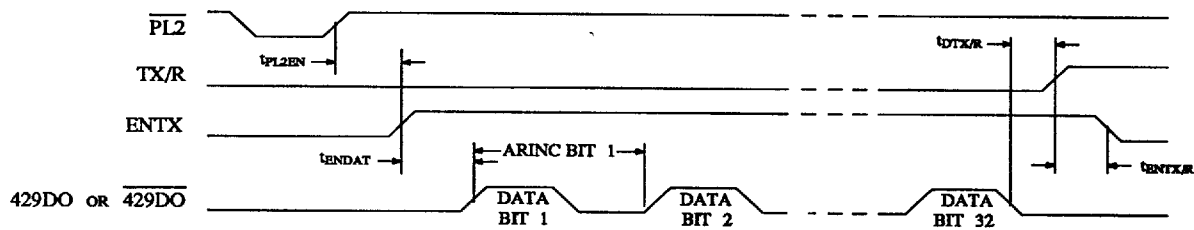


Timing Diagrams (cont.)

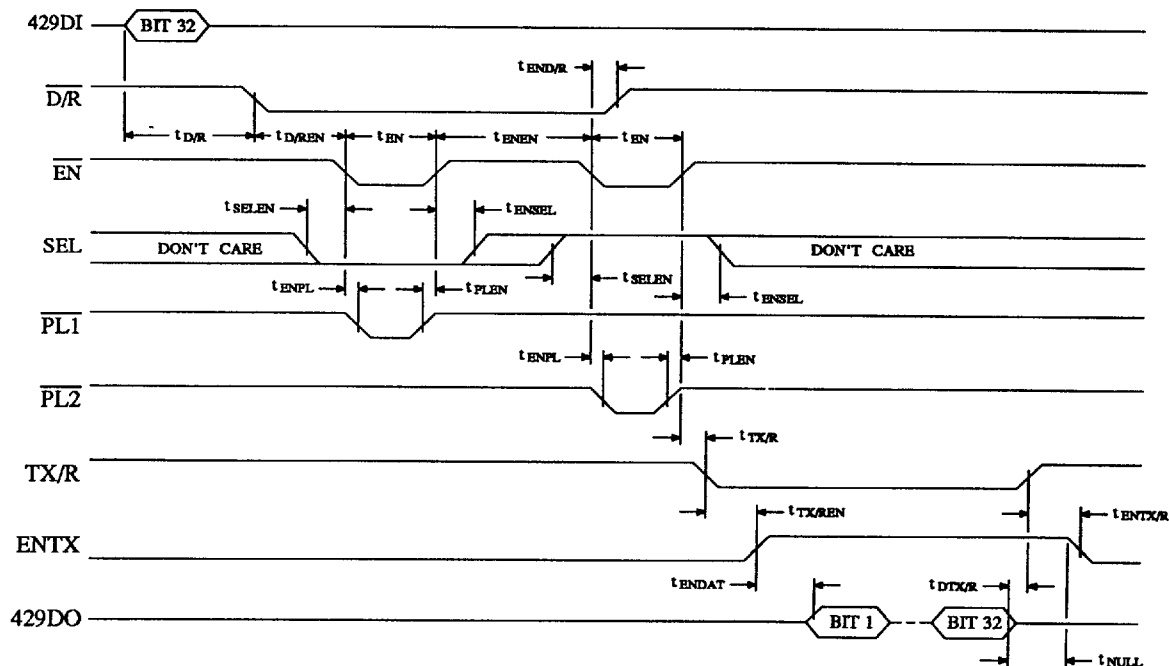
TRANSMITTER OPERATION



TRANSMITTING DATA



REPEATER OPERATION TIMING



Absolute Maximum Ratings

Voltages referenced to GND

Supply Voltage V_{CC}	-0.3V to +7V	Power Dissipation	500mW
Voltage at pins 2, 3, 4 & 5	-29V to +29V	Operating Temperature Range: Industrial . . .	-40°C to +85°C
Voltage at any other pin	-0.3V to $V_{CC} + 0.3V$	Military . . .	-55°C to +125°C
DC Current Drain per input pin	10mA	Storage Temperature Range: Industrial . .	-50°C to +150°C
		Military . . .	-65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

$V_{CC} = 5V \pm 5\%$, $GND = 0V$, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT		
			MIN	TYP	MAX			
ARINC Inputs – Pins 2, 3, 4 & 5								
Differential Input Voltage:	ONE ZERO NULL	V_{IH} V_{IL} V_{NUL}	Pins 2 to 3, 4 to 5. Common mode voltage less than $\pm 4V$ with respect to GND.		6.5 -13.0 -2.5	10.0 -10.0 0	13.0 -6.5 2.5	V V V
Input Resistance:	Differential to GND to VCC	R_I R_G R_H			12 12 12	27 27		K Ω K Ω K Ω
Input Current:	Input Sink Input Source	I_{IH} I_{IL}			-450		200	μA μA
Input Capacitance: (Guaranteed but not tested)	Differential to GND to VCC	C_I C_G C_H	Pins 2 to 3, 4 to 5.				20 20 20	pF pF pF
Bi-Directional Inputs – Pins 11-20, 22-27								
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}			2.1		0.7	V V
Input Current:	Input Sink Input Source	I_{IH} I_{IL}			-1.5		1.5	μA μA
All Other Inputs – Pins 8-10, 28, 29, 33, 34, 37 & 39								
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}			3.5		0.7	V V
Input Current:	Input Sink Input Source	I_{IH} I_{IL}			-20		10	μA μA
Outputs – Pins 6, 7, 11-20, 22-27, 30-32, 38								
Output Voltage: Logic "1" Output Voltage Logic "0" Output Voltage		V_{OH} V_{OL}	$I_{OH} = -1.5mA$ $I_{OL} = 1.8mA$		2.7		0.4	V V
Output Current:	Output Sink (Bi-directional Pins) Output Source	I_{OL} I_{OH}	$V_{OUT} = 0.4V$ $V_{OUT} = V_{CC} - 0.4V$		3.0 1.5			mA mA
Output Current:	Output Sink (All Other Outputs) Output Source	I_{OL} I_{OH}	$V_{OUT} = 0.4V$ $V_{OUT} = V_{CC} - 0.4V$		3.6 1.5			mA mA
Output Capacitance		C_O					15	pF
Supply Input – Pin 1								
Standby Supply Current		$ICC1$					20	mA
Operating Supply Current		$ICC2$					20	mA

AC Electrical Characteristics

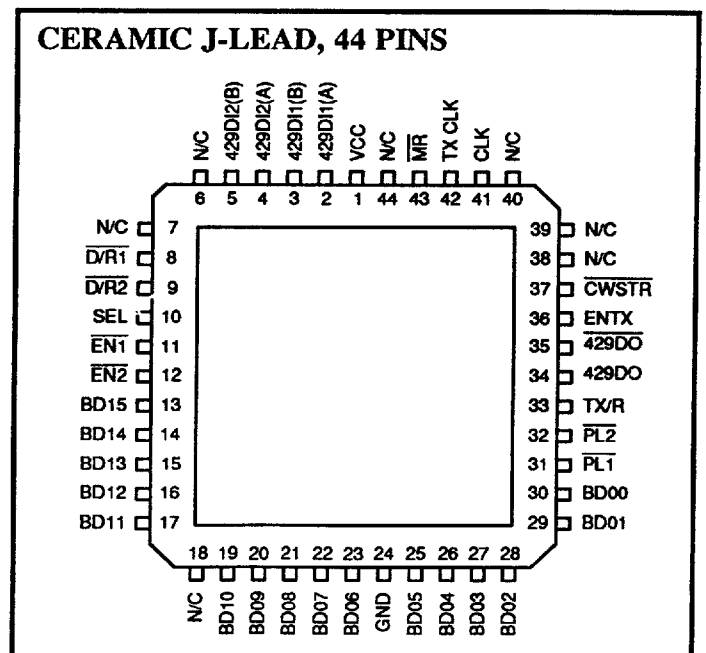
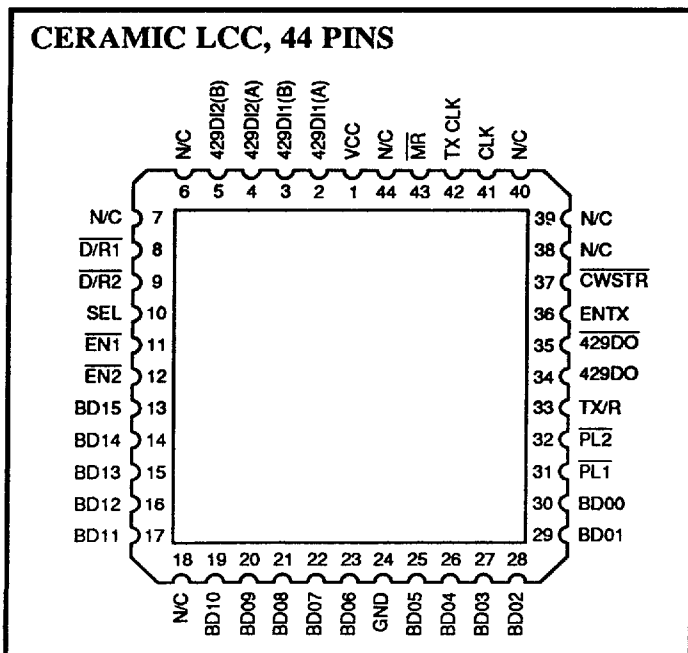
$V_{CC} = 5V$, $GND = 0V$, T_A = Operating Temperature Range, $f_{IN} = 1MHz \pm 0.1\%$, max. 60/40 duty cycle, applied at CLK.

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Control Word Timing						
Pulse Width - $\overline{CWSTR}$	t_{CWSTR}		130			ns
Setup - Data to $\overline{CWSTR}$	t_{CWSET}		140			ns
Hold - Data to $\overline{CWSTR}$	t_{CWHLD}		0			ns
Receiver Timing						
Delay-Start ARINC 32nd Bit to $\overline{D/R}$ Go LO:						
High Speed	$t_{D/R2}$				16	μs
Low Speed	$t_{D/R2}$				128	μs
Delay - $\overline{D/R}$ Go LO to Apply $\overline{EN}$	$t_{D/REN}$		0			ns
Delay - $\overline{D/R}$ Go HIGH from $\overline{EN}$	$t_{END/R}$				200	ns
Setup - SEL to $\overline{EN}$	t_{SELEN}		20			ns
Hold - SEL to $\overline{EN}$	t_{ENSEL}		50			ns
Delay - DATA BUS Valid from $\overline{EN}$	t_{ENDATA}				200	ns
Delay - DATA BUS Hi-Z from $\overline{EN}$	t_{DATAEN}				30	ns
Data Enable Pulse Width	t_{EN}		240			ns
Data Enable to Data Enable	t_{ENEN}		50			ns
FIFO Timing						
Pulse Width - $\overline{PL1}$ or $\overline{PL2}$	t_{PL}		200			ns
Setup - DATA to $\overline{PL}$	t_{DWSET}		110			ns
Hold - DATA to $\overline{PL}$	t_{DWHLD}		20			ns
Spacing - $\overline{PL1}$ to $\overline{PL2}$	t_{PL12}		0			ns
Delay - $\overline{PL2}$ to TX/R Go LOW	$t_{TX/R}$				840	ns
Transmission Timing						
Spacing - $\overline{PL2}$ to ENTX	t_{PL2EN}		0			μs
Delay - ENTX to 429DO or 429D $\overline{O}$:						
High Speed	t_{ENDAT}				25	μs
Low Speed	t_{ENDAT}				200	μs
Delay - 32nd ARINC Bit to TX/R HIGH:	$t_{DTX/R}$				400	ns
Spacing - TX/R Go HIGH to ENTX Go LOW	$t_{ENTX/R}$		0			ns
Repeater Operation Timing						
Data Enable to Parallel Load Delay Time	t_{ENPL}		0			ns
Data Enable Hold for Parallel Load Time	t_{PLEN}		0			ns
Enable Transmit Delay Time	$t_{TX/REN}$		0			ns
Master Reset Pulse Width	t_{MR}		400			ns
ARINC Data Rate and Bit Timing					$\pm 1\%$	

Terminal Connections

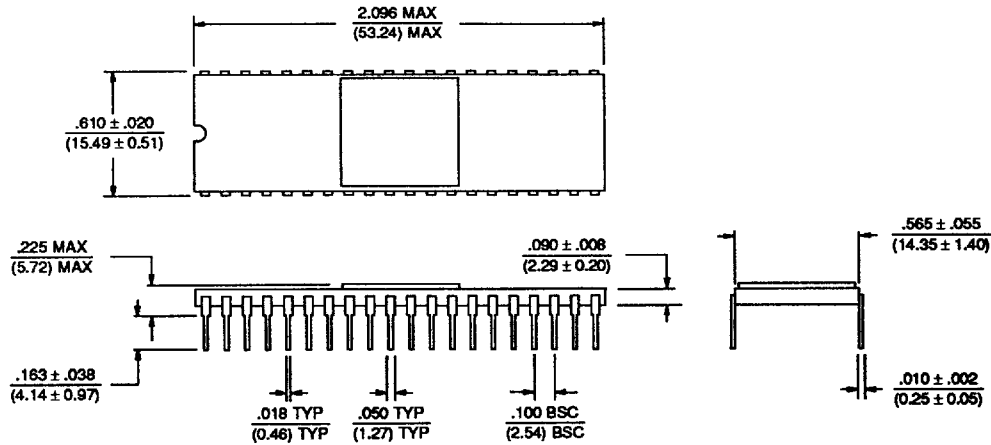
CERAMIC SIDE BRAZED DIP, 40 PINS				CERAMIC LCC, 44 PINS				CERAMIC J-LEAD, 44 PINS			
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VCC	21	GND	1	VCC	23	BD06	1	VCC	23	BD06
2	429DI1(A)	22	BD05	2	429DI1(A)	24	GND	2	429DI1(A)	24	GND
3	429DI1(B)	23	BD04	3	429DI1(B)	25	BD05	3	429DI1(B)	25	BD05
4	429DI2(A)	24	BD03	4	429DI2(A)	26	BD04	4	429DI2(A)	26	BD04
5	429DI2(B)	25	BD02	5	429DI2(B)	27	BD03	5	429DI2(B)	27	BD03
6	$\overline{D/R1}$	26	BD01	6	N/C	28	BD02	6	N/C	28	BD02
7	$\overline{D/R2}$	27	BD00	7	N/C	29	BD01	7	N/C	29	BD01
8	SEL	28	$\overline{PL1}$	8	$\overline{D/R1}$	30	BD00	8	$\overline{D/R1}$	30	BD00
9	$\overline{EN1}$	29	$\overline{PL2}$	9	$\overline{D/R2}$	31	$\overline{PL1}$	9	$\overline{D/R2}$	31	$\overline{PL1}$
10	$\overline{EN2}$	30	TX/R	10	SEL	32	$\overline{PL2}$	10	SEL	32	$\overline{PL2}$
11	BD15	31	429DO	11	$\overline{EN1}$	33	TX/R	11	$\overline{EN1}$	33	TX/R
12	BD14	32	$\overline{429DO}$	12	$\overline{EN2}$	34	429DO	12	$\overline{EN2}$	34	429DO
13	BD13	33	ENTX	13	BD15	35	$\overline{429DO}$	13	BD15	35	$\overline{429DO}$
14	BD12	34	$\overline{CWSTR}$	14	BD14	36	ENTX	14	BD14	36	ENTX
15	BD11	35	N/C	15	BD13	37	$\overline{CWSTR}$	15	BD13	37	$\overline{CWSTR}$
16	BD10	36	N/C	16	BD12	38	N/C	16	BD12	38	N/C
17	BD09	37	CLK	17	BD11	39	N/C	17	BD11	39	N/C
18	BD08	38	TX CLK	18	N/C	40	N/C	18	N/C	40	N/C
19	BD07	39	$\overline{MR}$	19	BD10	41	CLK	19	BD10	41	CLK
20	BD06	40	N/C	20	BD09	42	TX CLK	20	BD09	42	TX CLK
				21	BD08	43	$\overline{MR}$	21	BD08	43	$\overline{MR}$
				22	BD07	44	N/C	22	BD07	44	N/C

Pin Configurations

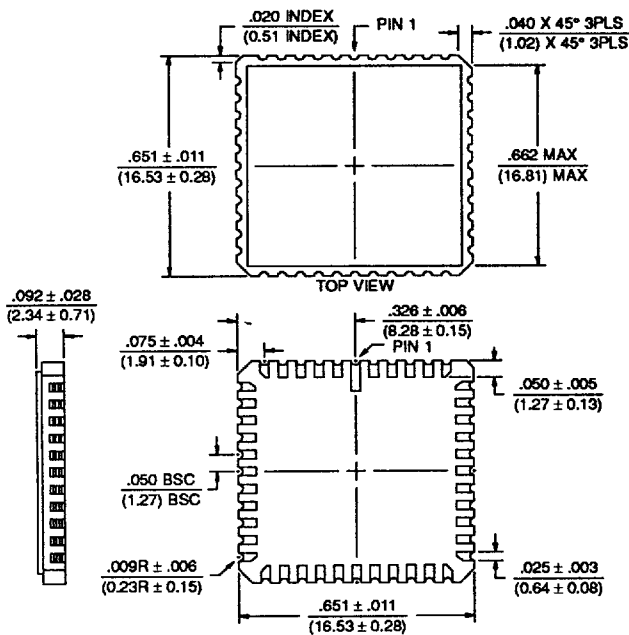


HI-8282 Standard Packaging

CERAMIC SIDE BRAZED DIP, 40 PINS



CERAMIC LCC, 44 PINS



Ordering Information

HI-8282C - Ceramic DIP, 40 pins, Industrial
 HI-8282S - Ceramic LCC, 44 pins, Industrial

HI-8282CM - Ceramic DIP, 40 pins, Military
 HI-8282SM - Ceramic LCC, 44 pins, Military

Additional packaging and screening options are available upon request.

Vender CAGE Number: 44270