EL7562

Data Sheet **June 26, 2002** **FN7295**

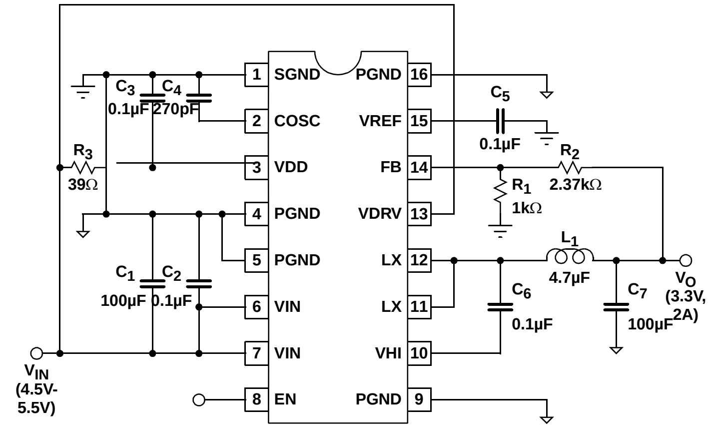
Monolithic 2Amp DC:DC Step-Down Regulator

The EL7562 is an integrated, synchronous step-down regulator with output voltage adjustable from 1.0V to 3.8V. It is capable of delivering 2A continuous current at up to 95% efficiency. The EL7562 operates at a constant frequency pulse width modulation (PWM) mode, making external synchronization possible. Patented on-chip resistorless current sensing enables current mode control, which provides cycle-by-cycle current limiting, over-current protection, and excellent step load response. The EL7562 is available in a fused-lead 16-pin QSOP package. With proper external components, the whole converter fits into a less than 0.5 in^2 area. The minimal external components and small size make this EL7562 ideal for desktop and portable applications.

The EL7562 is specified for operation over the 0°C to +70°C temperature range.

Pinout

EL7562
(16-PIN QSOP)
TOP VIEW



Please refer to page 4 for 3.3V input Application Diagram

Manufactured under U.S. Patent No. 57,323,974

Features

- Integrated synchronous MOSFETs and current mode controller
- 2A continuous output current
- Up to 95% efficiency
- 3.3V or 5V nominal input voltage
- Adjustable output from 1V to 3.8V
- Cycle-by-cycle current limit
- Precision reference
- ±0.5% load and line regulation
- Adjustable switching frequency to 1MHz
- Oscillator synchronization possible
- Internal soft-start
- Over-temperature protection
- Under-voltage lockout
- 16-pin QSOP package

Applications

- DSP, CPU core and IO supplies
- Logic/Bus supplies
- Portable equipment
- DC:DC converter modules
- GTL + Bus power supply

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. NO.
EL7562CU	16-Pin QSOP	-	MDP0040

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_{IN} or V_{DD} and GND . . . . +6.5V
V_{LX} Voltage . . . . V_{IN} +0.3V
Input Voltage . . . . GND -0.3V, V_{DD} +0.3V
V_{HI} Voltage . . . . GND -0.3V, V_{LX} +6V

Storage Temperature . . . . -65°C to +150°C
Operating Ambient Temperature . . . . 0°C to +70°C
Operating Junction Temperature . . . . +135°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

$V_{DD} = V_{IN}$ = 5V, $T_A = T_J$ = 25°C, C_{OSC} = 270pF, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference Accuracy		1.24	1.26	1.28	V
V_{REFTC}	Reference Temperature Coefficient			50		ppm/°C
$V_{REFLOAD}$	Reference Load Regulation	$0 < I_{REF} < 50\mu A$	-1			%
V_{RAMP}	Oscillator Ramp Amplitude			1.15		V
I_{OSC_CHG}	Oscillator Charge Current	$0.1V < V_{OSC} < 1.25V$		200		µA
I_{OSC_DIS}	Oscillator Discharge Current	$0.1V < V_{OSC} < 1.25V$		8		mA
$I_{VDD}+V_{DRV}$	$V_{DD}+V_{DRV}$ Supply Current	V_{EN} = 4V, F_{OSC} = 120kHz	2		6.5	mA
I_{VDD_OFF}	V_{DD} Standby Current	EN = 0		1	1.5	mA
V_{DD_OFF}	V_{DD} for Shutdown		2.5		2.7	V
V_{DD_ON}	V_{DD} for Startup		2.6		3	V
T_{OT}	Over-temperature Threshold			135		°C
T_{HYS}	Over-temperature Hysteresis			20		°C
I_{LEAK}	Internal FET Leakage Current	EN = 0, L_X = 5V (low FET), L_X = 0V (high FET)			20	µA
I_{LMAX}	Peak Current Limit		3			A
R_{DSON}	FET On Resistance	Wafer level test only		60	120	mΩ
R_{DSONTC}	R_{DSON} Tempco			0.2		mΩ/°C
V_{FB}	Output Initial Accuracy	I_{LOAD} = 0A	0.970	0.985	1.000	V
V_{FB_LINE}	Output Line Regulation	V_{IN} = 5V, ΔV_{IN} = 10%, I_{LOAD} = 0A		0.5		%
V_{FB_LOAD}	Output Load Regulation	$0.1A < I_{LOAD} < 1A$		0.5		%
V_{FB_TC}	Output Temperature Stability	-40°C < T_A < 85°C, I_{LOAD} = 0.5A		±1		%
I_{FB}	Feedback Input Pull Up Current	V_{FB} = 0V		100	200	nA
V_{EN_HI}	EN Input High Level			3.2	4	V
V_{EN_LO}	EN Input Low Level		1			V
I_{EN}	Enable Pull Up Current	V_{EN} = 0	-4	-2.5		µA

Closed-Loop AC Electrical Specifications

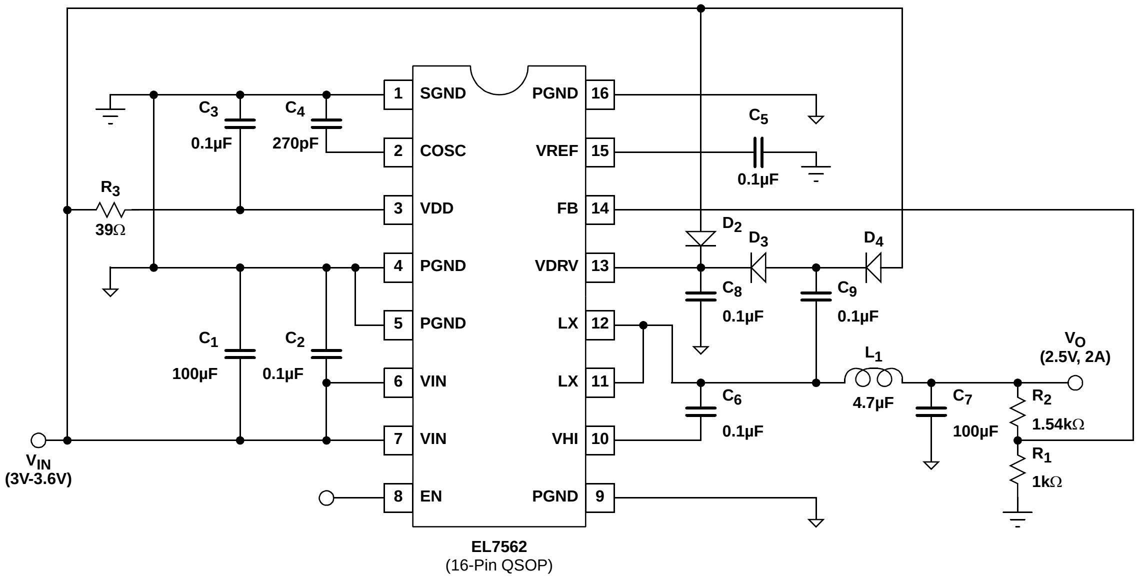
$V_S = V_{IN} = 5V$, $T_A = T_J = 25°C$, $C_{OSC} = 270pF$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
F_{OSC}	Oscillator Initial Accuracy		493	580	667	kHz
t_{SYNC}	Minimum Oscillator Sync Width			25		ns
M_{SS}	Soft-start Slope			0.5		V/ms
t_{BRM}	FET Break Before Make Delay			15		ns
t_{LEB}	High Side FET Minimum On Time			150		ns
D_{MAX}	Maximum Duty Cycle			95		%

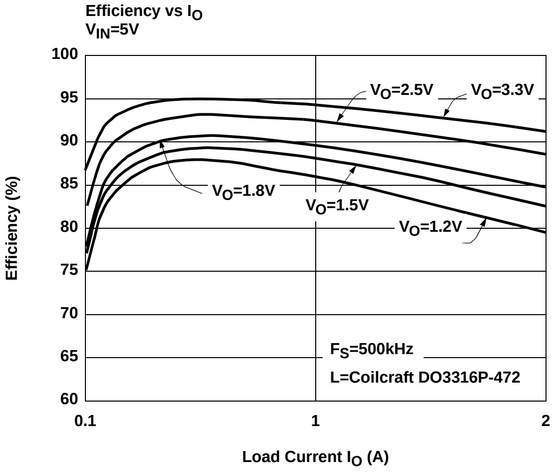
Pin Descriptions

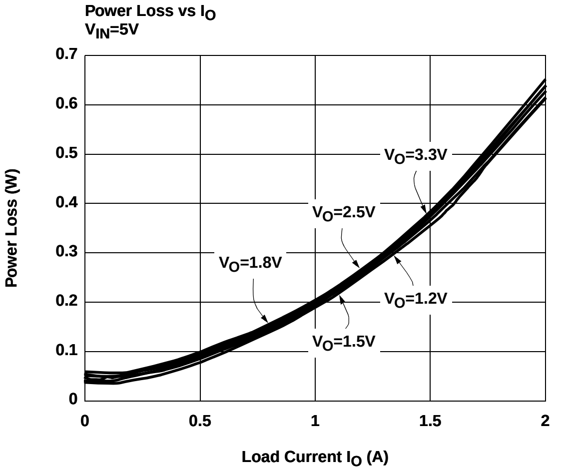
PIN NUMBER	PIN NAME	PIN FUNCTION
1	SGND	Control circuit negative supply
2	COSC	Oscillator timing capacitor; F_{OSC} can be approximated by: F_{OSC} (kHz) = $0.1843/C_{OSC}$, C_{OSC} in µF
3	VDD	Control circuit positive supply
4	PGND	Ground return of the regulator; connected to the source of the low-side synchronous NMOS power FET
5	PGND	Ground return of the regulator; connected to the source of the low-side synchronous NMOS power FET
6	VIN	Power supply input of the regulator; connected to the drain of the high-side NMOS power FET
7	VIN	Power supply input of the regulator; connected to the drain of the high-side NMOS power FET
8	EN	Chip enable, active high; a 2µA internal pull-up current enables the device if the pin is left open
9	PGND	Ground return of the regulator
10	VHI	Positive supply of the high-side driver
11	LX	Inductor drive pin; high current digital output whose average voltage equals the regulator output voltage
12	LX	Inductor drive pin; high current digital output whose average voltage equals the regulator output voltage
13	VDRV	Positive supply of the low-side driver and input voltage for the high-side boot strap
14	FB	Voltage feedback input; connected to an external resistor divider between V_{OUT} and GND; a 125nA pull-up current forces V_{OUT} to V_S in the event that FB is floating
15	VREF	Bandgap reference bypass capacitor; typically 0.1µF to GND
16	PGND	Ground return of the regulator

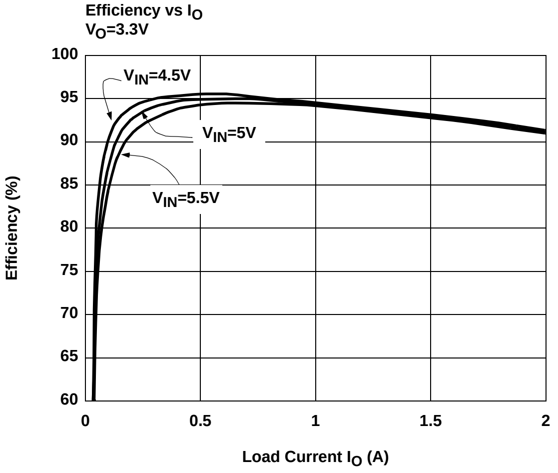
Application Diagram for 3.3V Input

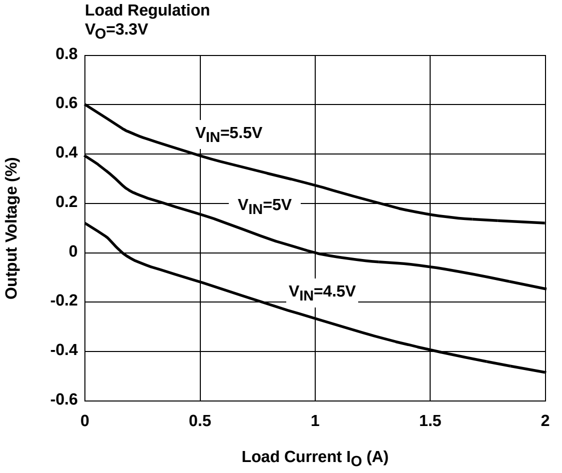


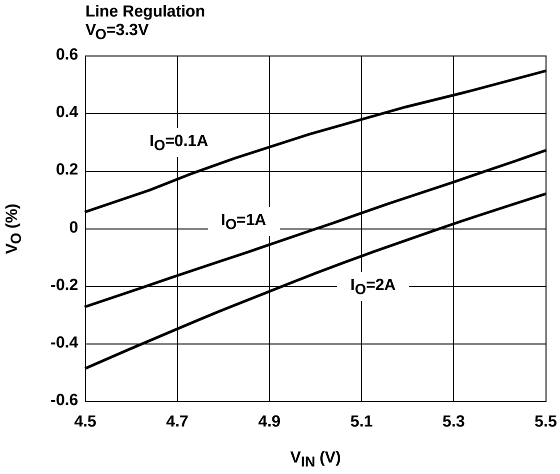
Typical Performance Curves

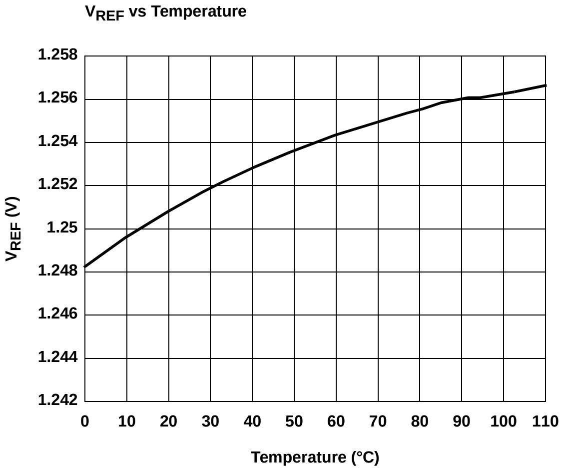




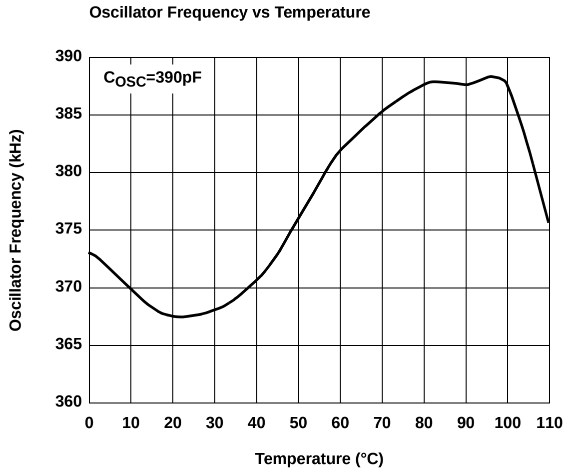


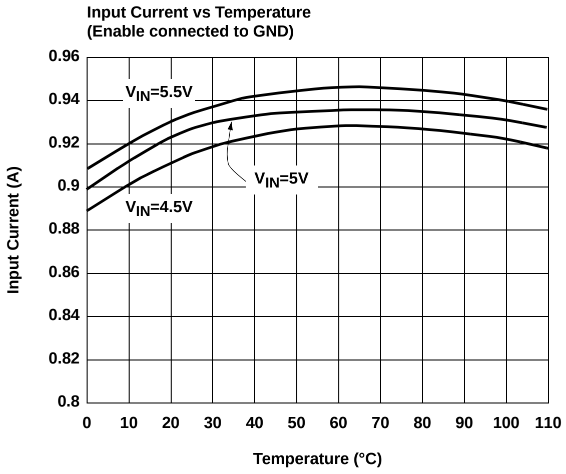


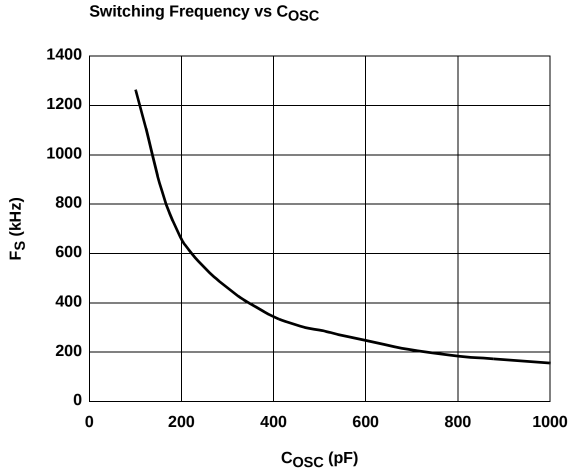




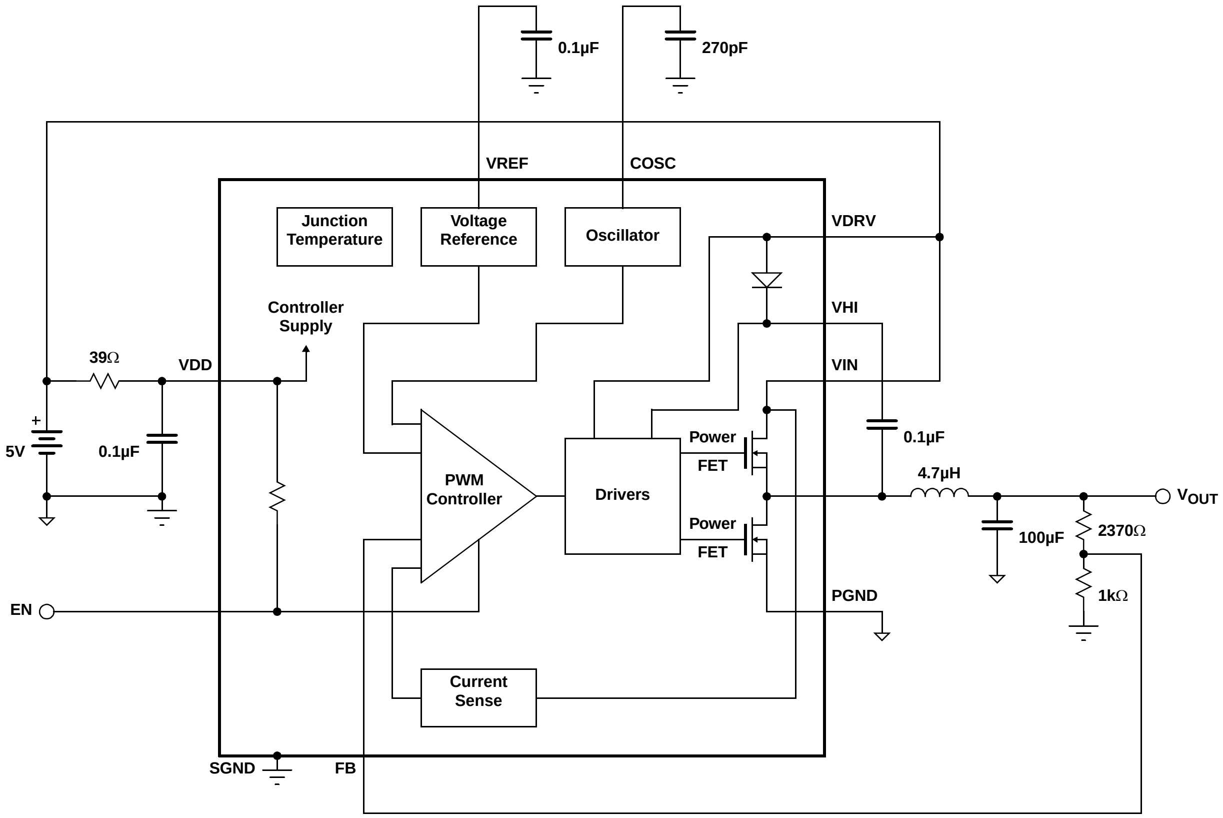
Typical Performance Curves (Continued)







Block Diagram



Applications Information

Circuit Description

General

The EL7562 is a fixed frequency, current mode controlled DC:DC converter with integrated N-channel power MOSFETs and a high precision reference. The device incorporates all the active circuitry required to implement a cost effective, user-programmable 2A synchronous step-down regulator suitable for use in DSP core power supplies.

Theory of Operation

The EL7562 is composed of 5 major blocks:

1. PWM Controller
2. NMOS Power FETs and Drive Circuitry
3. Bandgap Reference
4. Oscillator
5. Thermal Shut-down

PWM Controller

The EL7562 regulates output voltage through the use of current-mode controlled pulse width modulation. The three main elements in a PWM controller are the feedback loop and reference, a pulse width modulator whose duty cycle is controlled by the feedback error signal, and a filter which averages the logic level modulator output. In a step-down (buck) converter, the feedback loop forces the time-averaged output of the modulator to equal the desired output voltage. Unlike pure voltage-mode control systems, current-mode control utilizes dual feedback loops to provide both output voltage and inductor current information to the controller. The voltage loop minimizes DC and transient errors in the output voltage by adjusting the PWM duty-cycle in response to changes in line or load conditions. Since the output voltage is equal to the time-averaged of the modulator output, the relatively large LC time constant found in power supply applications generally results in low bandwidth and poor transient response. By directly monitoring changes in inductor current via a series sense resistor the controller's response time is not entirely limited by the output LC filter and can react more quickly to changes in line and load conditions. This feed-forward characteristic also simplifies AC loop compensation since it adds a zero to the overall loop response. Through proper selection of the current-feedback to voltage-feedback ratio the overall loop response will approach a one-pole system. The resulting system offers several advantages over traditional voltage control systems, including simpler loop compensation, pulse by pulse current limiting, rapid response to line variation and good load step response.

The heart of the controller is an input direct summing comparator which sum voltage feedback, current feedback, slope compensation ramp and power tracking signals together. Slope compensation is required to prevent system instability that occurs in current-mode topologies operating at duty-cycles greater than 50% and is also used to define the open-loop gain of the overall system. The slope compensation is fixed internally and optimized for 500mA inductor ripple current. The power tracking will not contribute any input to the comparator steady-state operation. Current feedback is measured by the patented sensing scheme that senses the inductor current flowing through the high-side switch whenever it is conducting. At the beginning of each oscillator period the high-side NMOS switch is turned on. The comparator inputs are gated off for a minimum period of time of about 150ns (LEB) after the high-side switch is turned on to allow the system to settle. The Leading Edge Blanking (LEB) period prevents the detection of erroneous voltages at the comparator inputs due to switching noise. If the inductor current exceeds the maximum current limit (I_{LMAX}) a secondary over-current comparator will terminate the high-side switch on time. If I_{LMAX} has not been reached, the feedback voltage FB derived from the regulator output voltage V_{OUT} is then compared to the internal feedback reference voltage. The resultant error voltage is summed with the current feedback and slope compensation ramp. The high-side switch remains on until all four comparator inputs have summed to zero, at which time the high-side switch is turned off and the low-side switch is turned on. However, the maximum on-duty ratio of the high-side switch is limited to 95%. In order to eliminate cross-conduction of the high-side and low-side switches a 15ns break-before-make delay is incorporated in the switch drive circuitry. The output enable (EN) input allows the regulator output to be disabled by an external logic control signal.

Output Voltage Setting

In general:

$$V_{OUT} = 0.985 \times \left(1 + \frac{R_2}{R_1}\right)$$

For V_{IN} = 5V

$$V_{OUT} = 0.975 \times \left(1 + \frac{R_2}{R_1}\right)$$

For V_{IN} = 3.3V

However, due to the relatively low open loop gain of the system, gain errors will occur as the output voltage and loop-gain is changed. This is shown in the performance curves. A 100nA pull-up current from FB to V_{DD} forces V_{OUT} to GND in the event that FB is floating.

NMOS Power FETs and Drive Circuitry

The EL7562 integrates low on-resistance (60mΩ) NMOS FETs to achieve high efficiency at 2A. In order to use an NMOS switch for the high-side drive it is necessary to drive the gate voltage above the source voltage (LX). This is accomplished by bootstrapping the V_{HI} pin above the LX voltage with an external capacitor C_{VHI} and internal switch and diode. When the low-side switch is turned on and the LX voltage is close to GND potential, capacitor C_{VHI} is charged through internal switch to V_{DRV}, typically 5V. At the beginning of the next cycle the high-side switch turns on and the LX pins begin to rise from GND to V_{IN} potential. As the LX pin rises the positive plate of capacitor C_{VHI} follows and eventually reaches a value of $V_{DRV}+V_{IN}$, typically 10V, for $V_{DRV}=V_{IN}=5V$. This voltage is then level shifted and used to drive the gate of the high-side FET, via the V_{HI} pin. A value of 0.1µF for C_{VHI} is recommended.

Reference

A 1.5% temperature compensated bandgap reference is integrated in the EL7562. The external V_{REF} capacitor acts as the dominant pole of the amplifier and can be increased in size to maximize transient noise rejection. A value of 0.1µF is recommended.

Oscillator

The system clock is generated by an internal relaxation oscillator with a maximum duty-cycle of approximately 95%. Operating frequency can be adjusted through the C_{OSC} pin or can be driven by an external source. If the oscillator is driven by an external source care must be taken in selecting the ramp amplitude. Since C_{SLOPE} value is derived from the C_{OSC} ramp, changes to C_{OSC} ramp will change the C_{SLOPE} compensation ramp which determine the open-loop gain of the system.

When external synchronization is required, always choose C_{OSC} such that the free-running frequency is at least 20% lower than that of sync source to accommodate component and temperature variations. Figure 1 shows a typical connection.

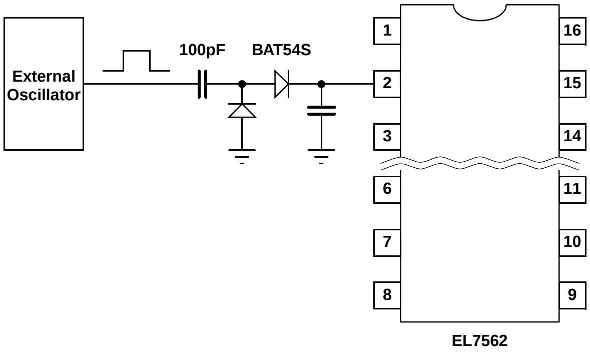


FIGURE 1. OSCILLATOR SYNCHRONIZATION

Thermal Shut-down

An internal temperature sensor continuously monitors die temperature. In the event that die temperature exceeds the thermal trip-point, the system is in fault state and will be shut down. The upper and low trip-points are set to 135°C and 115°C respectively.

Start-up Delay

A capacitor can be added to the EN pin to delay the converter start-up (Figure 2) by utilizing the pull-up current. The delay time is approximately:

$$t_d(ms) = 1200 \times C(\mu F)$$

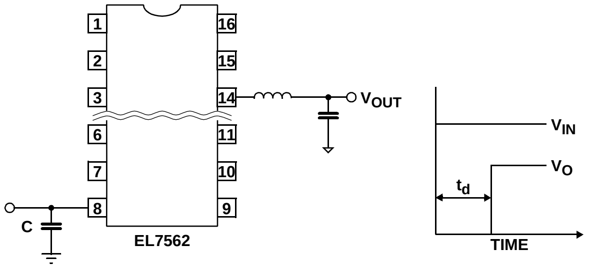


FIGURE 2. START-UP DELAY

Layout Considerations

The layout is very important for the converter to function properly. Power Ground (⏚) and Signal Ground (⏚) should be separated to ensure that the high pulse current in the Power Ground never interferes with the sensitive signals connected to Signal Ground. They should only be connected at one point (normally at the negative side of either the input or output capacitor).

The trace connected to pin 14 (FB) is the most sensitive trace. It needs to be as short as possible and in a “quiet” place, preferably between PGND or SGND traces.

In addition, the bypass capacitor connected to the V_{DD} pin needs to be as close to the pin as possible.

The heat of the chip is mainly dissipated through the PGND pins. Maximizing the copper area around these pins is preferable. In addition, a solid ground plane is always helpful for the EMI performance.

The demo board is a good example of layout based on these principles. Please refer to the EL7562 Application Brief for the layout.