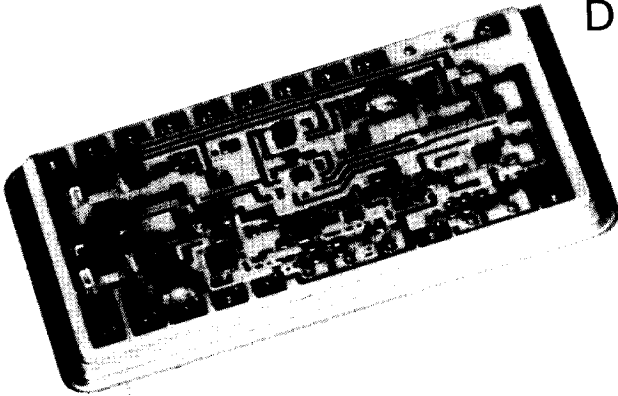


13 BIT T/H WITH CONTROLLED HOLD TIME Designed for Deglitching Applications



FEATURES

- 1000 ps APERTURE TIME UNCERTAINTY (JITTER)
- 1 mV/μs DROOP
- 1800 ns TYP SETTling TIME TO ±0.01% FOR 10V CHANGE
- 0.005% TYP LINEARITY ERROR

DESCRIPTION

The DGL-13 is a track-hold amplifier especially designed for deglitching applications. It will hold a voltage level constant during a glitch interval and then resume tracking. The hold time (50 ns minimum) is determined by an internal timing circuit and may be increased by adding an external capacitor. In normal operation the DGL-13 is strobed just before a glitch is expected to occur, and the internal switch opens 5 ns later to initiate the hold mode. The hold-pulse that opens the switch is available as an output pulse which may be used to initiate an input data change. While tracking, the DGL-13 operates as an op-amp in an

inverting mode with an output swing capability of up to ±10V.

APPLICATIONS

The DGL-13 track/hold can be used to deglitch DACs in applications such as cockpit CRT displays and transient sensitive servo systems. It can function as a gated op-amp in digitally controlled frequency synthesizers. The DGL-13 can operate well in the most stringent of industrial and military ground and avionics applications. The processing of DDC hybrids is based on MIL-STD-883 and they are suitable for remotely located and hard to access equipment where high MTBF and small size are critical.

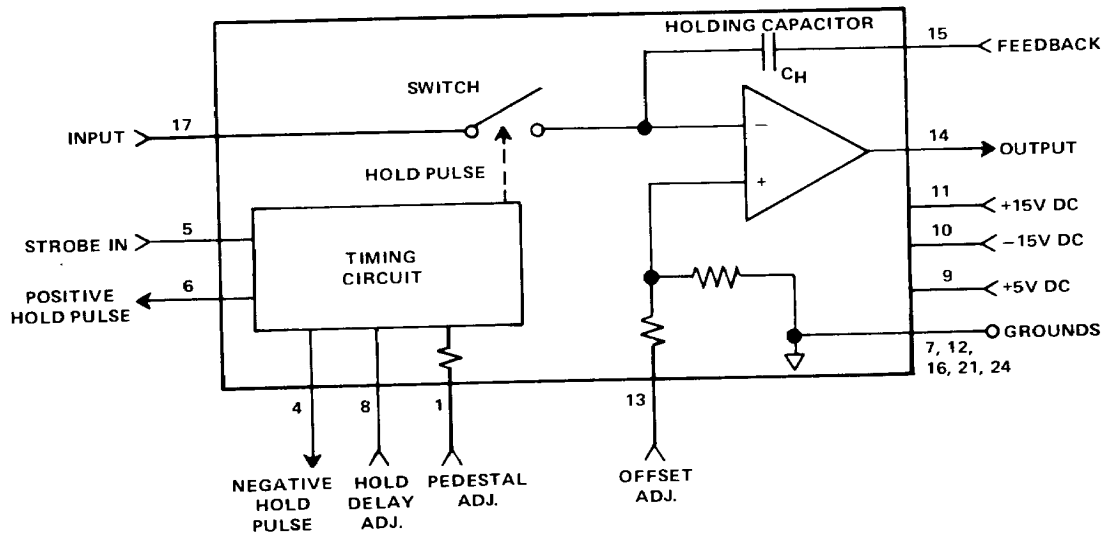


FIGURE 1. DGL-13 BLOCK DIAGRAM

SPECIFICATIONS

At 25° case temperature and at rated power supplies unless otherwise noted.

PARAMETER	UNITS	VALUE	PARAMETER	UNITS	VALUE
ACCURACY			LOGIC INPUT/OUTPUT		
Linearity Error	% FSR	0.01 max	Logic Type		TTL compatible
Linearity Tempco	ppm FSR/°C	1.0 max	Strobe Input		Positive pulse, 10 ns min
DC Offset	mV	35 max (Trimable to zero)	Positive Hold Pulse Output		Loading is 3 std TTL loads
DC Offset Tempco	μV/°C	40 max	Negative Hold Pulse Output		Delayed 5 ns nominal with respect to strobe input, pulse length equal to hold time
Pedestal	mV	±10 (Trimable to zero)			Drive capability is 5 std TTL loads
Pedestal Tempco	μV/°C	50 max			Same as positive pulse, except inverted
DYNAMIC CHARACTERISTICS			OUTPUT		
Small Signal Bandwidth (f _t)	MHZ	12 typ; 8 min	Output Voltage Swing (R _L ≥ 2KΩ)	V	12 typ; 10 min
Large Signal Voltage Gain At 25° C (Case)	V/V	25,000 typ; 15,000 min	Output Current Range	mA	+5
Full Temperature Range	V/V	10,000 min	Max Peak Output Current Without Damage	mA	50
Internal Hold Capacitance (C _H)	pF	10 ± 10%	Full Power Bandwidth for ±10V Output	kHz	330 typ; 250 min
Slew Rate	V/μs	20 typ; 15 min	Short Circuit Protection to GND	sec	5 at 25° C case temperature
Max Sampling Rate	MHZ	10			2 at 85° C case temperature
Min Cycle Time	ns	50	POWER REQUIREMENTS		
Min Hold Time	ns	50 (may be increased by external capacitor)	Supply Voltages	V	+15 ± 2% -15 ± 2% +5 ± 1%
Acquisition Turn-On Delay	ns	5 typ; 10 max	Absolute Max Voltage	V	+18 -18 +5.5
Acquisition Time	ns	Equal to settling time — see text	Current	mA	25 typ 40 typ 50 typ
Aperature Time Delay	ns	5 typ; 10 max	Power Dissipation	W	+ load + load + load
Aperature Time Uncertainty (Jitter)	ns	1.0 typ			0.85 typ + load
Feedthrough Attenuation in Hold Mode	dB	60 typ	TEMPERATURE RANGE (CASE)		
Settling Time		Depends on feedback resistor — see text	Operating	°C	-55 to +85
Droop Rate	mV/μs	1.0 typ; 10 max	-1 Option	°C	0 to +70
Droop Rate Tempco		Double every 10° C	-3 Option	°C	-55 to +125
ANALOG INPUT			PHYSICAL CHARACTERISTICS		
Offset Voltage	mV	50 max	Size (24 Pin DDIP)	inch	0.8 x 1.4 x 0.2 (2 x 3.6 x 0.5 cm)
Offset Voltage Average Drift	μV/°C	40	Weight	oz	0.38 typ (10.8 g)
Bias Current at 25°	μA	1 typ; 5 max			
Max Input Voltage Without Damage	V	±15			

TECHNICAL INFORMATION

INTRODUCTION

As shown in the block diagram, Figure 1, the main components of the DGL-13 are an amplifier connected in an inverting mode, a holding capacitor, and a switch controlled by a timing circuit. If the timing circuit is not strobed, the switch remains closed and the output will track the input. When a strobe pulse is applied, its leading edge triggers a one-shot in the timing circuit which, 5 ns later, generates a hold pulse. The leading edge of the hold pulse in turn opens the switch to initiate the hold mode. The output voltage then remains at the voltage stored on the holding capacitor. The hold mode time, which is determined by the timing circuit, is 50 ns typical. The hold time may be increased by adding an external capacitor between pins 4 and 8 (see Figure 4).

The hold pulse is also available as an output strobe at pin 6 to indicate when the switch begins to open. The hold mode output may be used to initiate an input data change.

The five ground pins, 5, 12, 16, 21, and 24, should be connected together externally with a ground plane.

The DGL-13 was designed as a component for the DDAC, a 10 MHz, 13 bit hybrid D/A converter. The DDAC Technical Information section shows how the DGL-13 can be used in a high speed deglitching application.

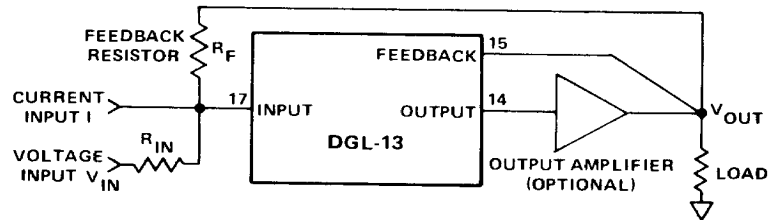


FIGURE 2. SIGNAL INPUT/OUTPUT CONNECTIONS

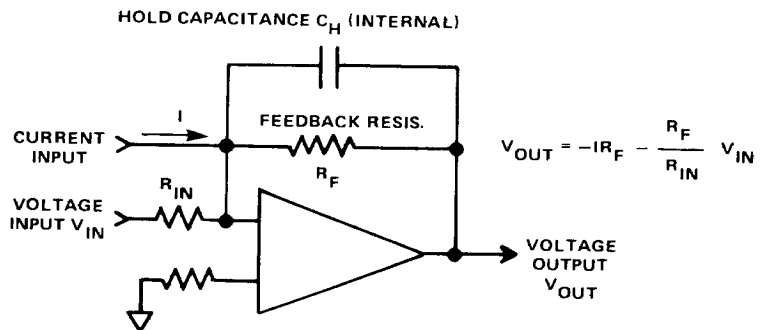


FIGURE 3. EQUIVALENT CIRCUIT IN TRACK MODE

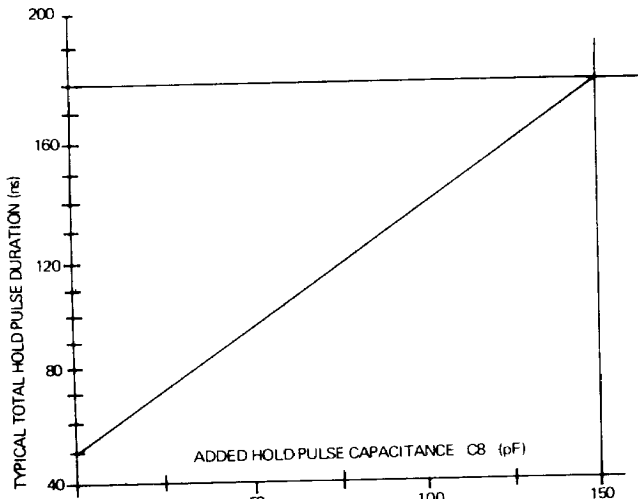


FIGURE 4. HOLD PULSE DURATION VS ADDED CAPACITANCE

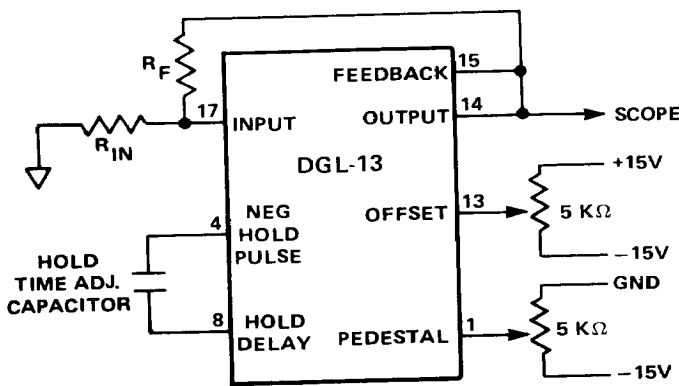


FIGURE 5. ADJUSTMENTS FOR HOLD TIME AND TRIM

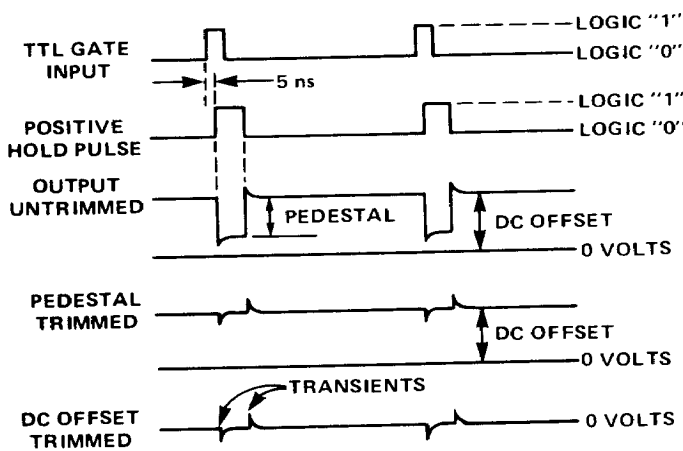


FIGURE 6. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

INPUT/OUTPUT CONNECTIONS AND SETTLING TIME

Figure 2 shows proper signal input and output connections. The feedback pin 15 and the external feedback resistor R_F should be connected to the output as close to the load as possible to minimize the effects of line resistance. In the tracking mode, the equivalent circuit is that of an inverting amplifier, as shown in Figure 3. The feedback resistor is used to adjust the output scaling. If it is relatively large, it may reduce the bandwidth below the intrinsic bandwidth of the amplifier.

The analog output pin may be grounded for 5 sec at $+25^\circ\text{C}$ and 2 sec at $+85^\circ\text{C}$ case temperature. It must not be connected to any of the three supplies or damage to the converter will occur.

The DGL-13 output can provide ± 5 mA and a voltage range of $\pm 10\text{V}$. An optional external current booster amplifier may be added, as shown in Figure 2. DDC's coax cable driver, the HCD-13, will provide up to 500 mA at $\pm 10\text{V}$ for this application, as discussed in the DDAC data sheet.

When switched into the track mode, the DGL-13 output tends to overshoot slightly before settling out. With large voltage changes, the output transition is limited by the $20\text{V}/\mu\text{s}$ slew rate of the amplifier. For 10V changes, the output will settle to within $\pm 0.01\%$ of final value in 1800 ns. The settling time for small signal changes (not limited by slew) is limited by the bandwidth of the internal amplifier, the internal capacitance, and the external resistors. The settling time can be calculated from the following chart and formula:

Number of Time Constants	Output Settles to Within
2.3	10%
4.6	1%
6.9	0.1%
9.2	0.01%

Time Constant (in ns)

$$= \frac{(R_F + R_{IN}) \times 10^3}{2\pi f_t R_{IN}} + C_H R_F$$

where:

f_t = small signal bandwidth in MHz
 R_F, R_{IN} = feedback and input resistors in $\text{K}\Omega$
 C_H = internal hold capacitance in pF.

The acquisition time of the DGL-13 will always be identical to its output settling time. This is because the DGL-13 can be used only in an inverting mode with a feedback capacitor.

TIMING

The minimum hold pulse duration is 50 ns typical, but this interval may be increased to 180 ns or more. The relationship between hold pulse duration and any additional capacitance added between pins 4 and 8 is shown in Figure 4.

The maximum cycling rate of the DGL-13 depends on the settling time after switching to the tracking mode, on the delay, and on the hold time in the hold mode. For instance, assume a time constant of 90 ns and that settling is required to $\pm 10\%$. The table in the previous section shows that $\pm 10\%$ settling requires 2.3 time constants so the settling time is $2.3 \times 90 = 207$ ns. If the hold time has not been increased beyond 50 ns, the total time is:

207 ns	for Settling
50 ns	for Hold Time
5 ns	for Delay
262 ns	Total Interval

The maximum cycling rate will then be $1/262$ ns = 3.82 MHz. A slower rate is acceptable, but a faster rate will not allow sufficient time for settling.

TRIM ADJUSTMENTS

The DC offset and pedestal are trimmed at the factory to within the limits listed in the specifications table. Further adjustments may be made after installation using the trim adjustment circuit shown in Figure 5. Connect the output (pin 14) to an oscilloscope and ground the input (pin 17) through an input resistor R_{IN} . The trim settings will depend on the values of R_{IN} and R_F . Apply an approximately 30 ns positive TTL pulse at a rate of about 1 MHz to the strobe input (pin 5). Vary the pedestal adjust potentiometer to minimize the pedestal and the DC offset potentiometer to trim the offset as depicted in Figure 6.

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All DDC hybrids are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5004/5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number.

ORDERING INFORMATION

DGL - 13 - 1 - 883B

MIL-STD-883 Processing:
 883B = Conforms to MIL-STD-883B, DDC procedures
 Blank = Same, except pre-burn in test and burn in are omitted.

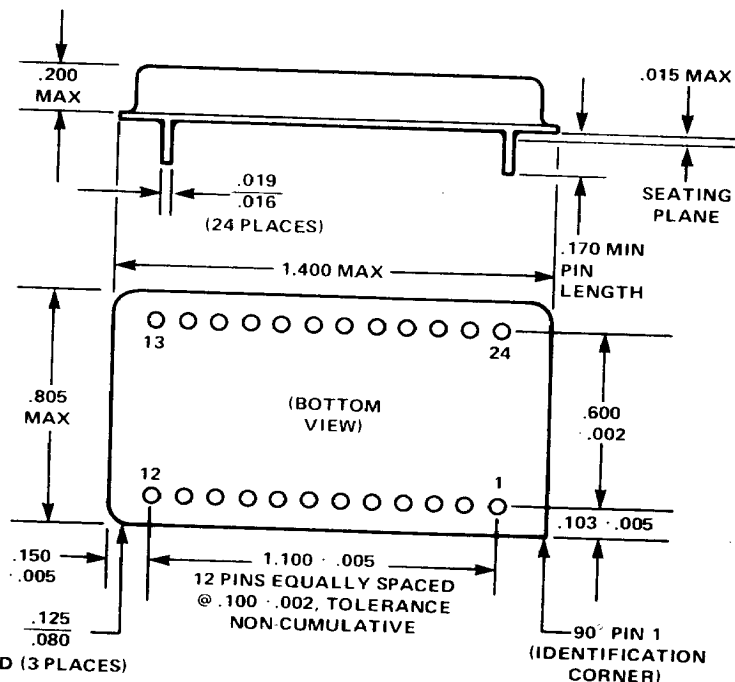
Operating Temperature Range (Case):
 -1 = -55°C to $+85^{\circ}\text{C}$
 -3 = 0°C to $+70^{\circ}\text{C}$

PIN CONNECTION TABLE

PIN	FUNCTION
1	Pedestal Adjust
2	N.C.
3	N.C.
4	Negative hold pulse
5	Strobe input
6	Positive hold pulse
7	Ground (To Case)
8	Delay adjust
9	+5VDC
10	-15VDC
11	+15VDC
12	Ground (To Case)
13	Offset adjust
14	Analog output
15	Feedback
16	Ground (To Case)
17	Analog input
18	N.C.
19	N.C.
20	N.C.
21	Ground (To Case)
22	N.C.
23	N.C.
24	Ground (To Case)

MECHANICAL OUTLINE

24 PIN DOUBLE DIP



NOTES

1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead cluster shall be centered within ± 0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C