DAC-608, DAC-610, DAC-612
Microprocessor-Compatible, Double-Buffered D/A Converters

FEATURES

- **Microprocessor-compatible**
- **Double-buffered inputs**
- **8-, 10- and 12-Bit resolution**
- **500 Nanoseconds settling time—DAC-610**
- **4-Quadrant multiplication**

GENERAL DESCRIPTION

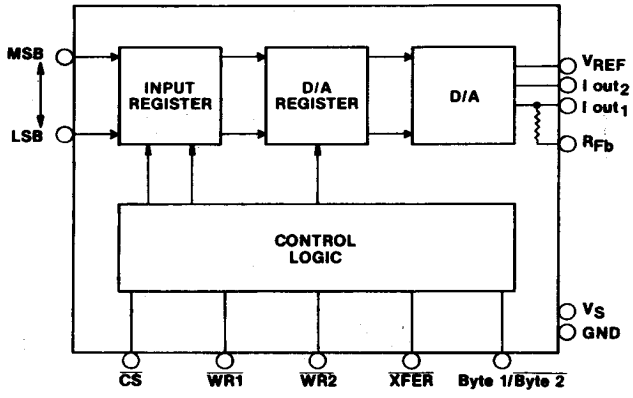
DATEL's DAC-608, DAC-610 and DAC-612 are low cost monolithic 8-, 10-and 12-bit multiplying D/A converters designed to operate directly with most popular microprocessors. Double-buffered inputs allow the converters to output an analog voltage corresponding to one digital word while holding the next, permitting simultaneous updating of multiple D/A's via a common strobe signal. The converters appear as a memory location or I/O port to the microprocessor and thus do not require interfacing logic. All models will operate as normal D/A's for non-microprocessor based applications.

Excellent temperature tracking characteristics are provided by precision silicon-chromium R-2R resistor ladder networks. Output settling time for a full-scale change to ½ LSB, is as low as 500 nanoseconds and the maximum linearity error on all models is ±½ LSB. Monotonicity is guaranteed over the full operating temperature range.

Other features include a low, 3 mV peak-to-peak, digital feedthrough error, 30 mW power dissipation and single supply operation. The reference input is selectable over a range of ±10V and may also be used as the analog input for four quadrant multiplication applications.

The DAC-612C is packaged in a 24-pin ceramic DIP. Models DAC-608 and DAC-610 are packaged in a 20-pin plastic DIP. All units are specified to operate over the commerical 0° C to +70° C temperature range. These devices are an ideal choice for innumerable applications involving industrial process control, programmable attenuators, audio signal processing and low frequency sine wave generation.

CAUTION: These devices contain CMOS circuits and should be handled with standard anti-static procedures.



INPUT/OUTPUT CONNECTIONS

DAC-608

PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)
2	$\overline{WR1}$ (WRITE 1)
3	ANALOG GROUND
4	DI3
5	DI2
6	DI1
7	DI0 (LSB)
8	REFERENCE IN
9	FEEDBACK
10	DIGITAL GROUND
11	OUTPUT 1
12	OUTPUT 2
13	DI7 (MSB)
14	DI6
15	DI5
16	DI4
17	$\overline{XFER}$ (Trans. Contl.)
18	$\overline{WR2}$ (Write 2)
19	ILE (In. Latch ENB)
20	V_S

DAC-610

PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)
2	$\overline{WR}$ (WRITE)
3	BYTE 1/$\overline{BYTE\ 2}$
4	$\overline{XFER}$
5	DI5
6	DI6
7	DI7
8	DI8
9	DI9 (MSB)
10	GROUND
11	OUTPUT 2
12	OUTPUT 1
13	REFERENCE IN
14	FEEDBACK
15	DI0 (LSB)
16	DI1
17	DI2
18	DI3
19	DI4
20	V_S

DAC-612

PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)
2	$\overline{WR1}$
3	ANALOG GROUND
4	DI5
5	DI4
6	DI3
7	DI2
8	DI1
9	DI0 (LSB)
10	REFERENCE IN
11	FEEDBACK
12	DIGITAL GROUND
13	OUTPUT 1
14	OUTPUT 2
15	DI11 (MSB)
16	DI10
17	DI9
18	DI8
19	DI7
20	DI6
21	$\overline{XFER}$ (Trans. Contl.)
22	$\overline{WR2}$ (Write 2)
23	BYTE 1/$\overline{BYTE\ 2}$
24	V_S

ABSOLUTE MAXIMUM RATINGS	DAC-608	DAC-610	DAC-612C
Power Supply Voltage		+17V dc	
Logic Input Voltage		V_S to ground	
Reference Input Voltage		±25V	
Output Voltage		V_S to 100 mV	
Package Dissipation		500 mW	

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, 15V Supply, Reference In = +10V unless otherwise noted.

INPUTS	DAC-608	DAC-610	DAC-612
Resolution	8 bits	10 bits	12 bits
Coding, Unipolar operation		Straight Binary	
Bipolar operation		Offset Binary	
Input Logic Level, bit ON ("1")		+2.2V minimum at + 10 µA maximum	
Input Logic Level, bit OFF ("0")		+0.8V maximum at −200 µA maximum	
CS (Chip Select)	Active low state in combination with ILE enables the D/A for Write 1 operation. Minimum pulse duration is 320 nsec.. CS must remain low an additional 10 nsec. after Write Pulse returns high.		
ILE (Input Latch Enable)[1]	Active high state in combination with CS enables the D/A for Write 1 operation. Minimum Pulse duration is 320 nsec. ILE must remain high an additional 10 nsec. after Write Pulse returns high.		
WR1 (Write 1)	Active low state is used to load the digital data bits into the input latch. A high ON WR1, and a high on ILE will update the input latch. Minimum Pulse duration is 320 nsec.		
WR2 (Write 2)	Active low in combination with XFER transfers available data in the input latch to the D/A register. The data in the D/A register is latched when WR2 is high. Minimum Pulse Duration is 320 nsec.		
Byte 1/Byte 2 (Byte Sequence Control)[2]	All locations of the input latch are enabled when this control is high. When low, only least significant bits are enabled. Pulse Duration is 320 nsec.		
XFER (Transfer Control Signal)	Active low in combination with WR2, will transfer the data available in the input latch to the D/A register.		
OUTPUTS			
Output Capacitance, Output 1[3]	70 pF	60 pF	70 pF
Output 2[3]	200 pF	250 pF	200 pF
Output 1[4]	200 pF	250 pF	200 pF
Output 2[4]	70 pF	60 pF	70 pF
Output 1, Current Range[5]	$\frac{V_{REF}}{15\ k\Omega}$ $\frac{D}{256}$	$\frac{V_{REF}}{15\ k\Omega}$ $\frac{D}{1024}$	$\frac{V_{REF}}{15\ k\Omega}$ $\frac{D}{4096}$
Output 2, Current Range[5]	$\frac{V_{REF}}{15\ k\Omega}$ $\frac{256-D}{256}$	$\frac{V_{REF}}{15\ k\Omega}$ $\frac{1024-D}{1024}$	$\frac{V_{REF}}{15\ k\Omega}$ $\frac{4096-D}{4096}$
Feedthrough Error[3]	3 mV P-P	90 mV P-P	3 mV P-P
PERFORMANCE			
Linearity Error Maximum		± ½ LSB	
Differential Linearity Error Maximum		±0.018% FSR	
Monotonicity		Over operating temperature range	
Gain Error[6]		Adjustable to Zero	
Zero Error[6]		Adjustable to Zero	
Gain Tempco Maximum	±6 ppm/°C	±10 ppm/°C	±6 ppm/°C
Settling Time, Full Scale change to ± ¼ LSB	1 µsec.	500 nsec.	1 µsec.
Power Supply Rejection[4]	±2 ppm/V	±30 ppm/V	±3 ppm/V
POWER REQUIREMENTS			
Rated Power Supply Voltage		+15V dc	
Power Supply Voltage Range		+4.7V dc to +15.75V dc	
Supply Current Maximum		2 mA	

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Package Type:	
DAC-608/610	20-pin plastic DIP
DAC-612	24-pin ceramic DIP

FOOTNOTES:

1. DAC-608 only.
2. DAC-610/612 only.
3. All data inputs latched low. To achieve this low feedthrough on the DAC-612, the metal lid must be grounded. If the lid is left floating the feedthrough is typically 8 mV.
4. All data inputs latched high.
5. "D" stands for digital input.
6. Using internal feedback resistor.

TECHNICAL NOTES

1. The output operational amplifier to be used should have as low a value of input bias current as possible. DATEL's AM-410 operational amplifiers are highly recommended for use with these devices.

   In order to maintain the specified temperature tracking specifications, the D/A's internal feedback resistor should be used in the operational amplifier feedback loop.

2. The voltage at the current outputs must be as close to ground potential as possible so that the changes in the applied digital codes do not affect the output current linearity.

3. In fast data acquisition applications, the addition of a 10 to 22 pF capacitor (Cc) in parallel with the feedback resistor of the operational amplifier may be required to minimize overshoot and ringing at the output.

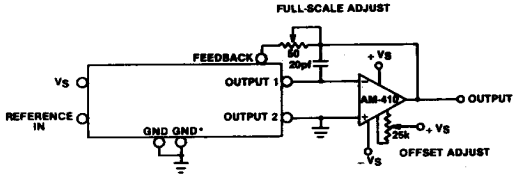
4. Due to the rapid switching of internal logic gates that respond to the input changes, a narrow spike could flow out from the current output terminals. In order to minimize this effect, the input register must always be used as the data latch. Reducing V_S from +15V to +5V offers a factor of 5 improvement in the magnitude of the feedthrough, however, this causes a loss of internal switching speed. Also, increasing capacitor Cc (if being used) to a value consistent with the actual circuit bandwidth requirements, can provide a substantial damping effect on any output spikes.

5. For flow through operation, (operation with the buffers continuously enabled) CS, WR1, WR2 and XFER must be tied to ground and Byte 1/Byte 2 (ILE for DAC-608) must be high. This will allow

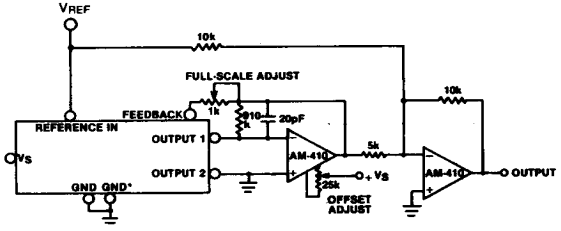
both internal registers to follow the applied digital inputs, directly affecting the device output.

6. For stand alone operation where control signals are generated by discrete logic, double buffering can be controlled by applying a logic "0" to $\overline{CS}$ and $\overline{XFER}$ and a logic "1" to ILE and pulling $\overline{WR1}$ low to load data in the input latch. Pulling $\overline{WR2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.
7. All unused digital inputs should be tied to V_S or ground in order to prevent damage to the chip from static discharge. If any of the digital inputs are inadvertently left floating, the D/A will interpret the pin as a logic "1".
8. The input registers of the DAC-610 and DAC-612 are arranged to accept a left justified data word from the microprocessor with 8 bits coming first and the lower bits second. Left-justified means that the binary point is assumed to be located to the left of the most significant bit.
9. The use of good circuit board layout techniques are required for rated performance. Minimization of lead lengths around analog circuitry is recommended. It is important that a good ground be used. A single point ground distribution technique for analog signals and supply returns will prevent other devices in the system from affecting the output of the D/A's. V_S should be bypassed as close to the V_S pin as possible with a low inductance 1 μF tantalum capacitor.

CODING AND CALIBRATION



UNIPOLAR CONFIGURATION



BIPOLAR CONFIGURATION

*ONE GROUND ON DAC-610

CALIBRATION PROCEDURE

UNIPOLAR

Zero Adjust—Set all data bits to logic "0" (logic "1" if using output 2) and adjust the OFFSET ADJUST pot on the external operational amplifier for 0.000V.

Full Scale—Set all data bits to logic "1" (logic "0" if using output 2) and set the FULL Scale ADJUST for an output equal to: Vout = −Vref (N − 1)/N, where "N" is equal to: 256 (DAC-608), 1024 (DAC-610) or 4096 (DAC-612).

BIPOLAR

Zero Adjust—Set all data bits to logic "0" and adjust the OFFSET ADJUST for an output voltage equal to Vref.

Full Scale—Set all data bits to logic "1" and adjust the FULL SCALE ADJUST for an output voltage equal to: Vout = Vref (N-X)/X where "N" is equal to: 255 (DAC-608), 1023 (DAC-610) or 4095 (DAC-612); and "X" is equal to: 128 (DAC-608), 512 (DAC-610) or 2048 (DAC-612).

OUTPUT CODING TABLES

UNIPOLAR OPERATION

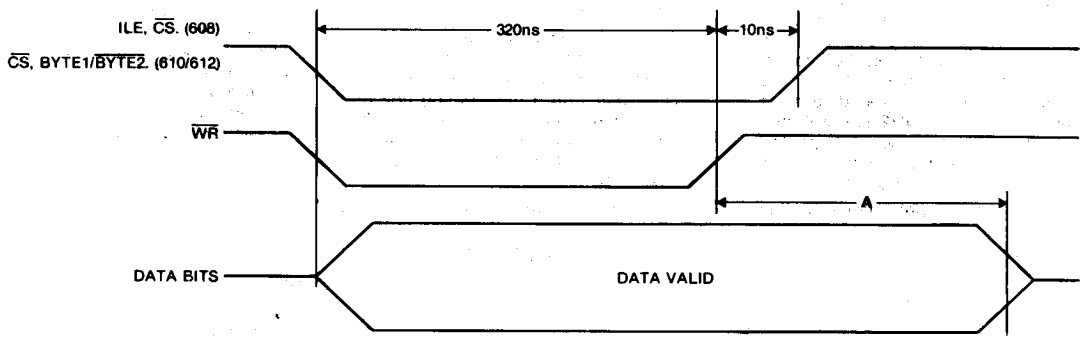
INPUT CODE MSB ..... LSB	IDEAL OUTPUT
111.....111	−(VREF + 1 LSB)
110.....000	−0.75 (VREF)
100.....000	−0.5 (VREF)
010.....000	−0.25 (VREF)
000.....000	0

BIPOLAR OPERATION

INPUT CODE MSB ..... LSB	IDEAL OUTPUT +VREF	IDEAL OUTPUT −VREF
111.....111	+VREF −1 LSB	−VREF + 1 LSB
110.....000	0.5 (+VREF)	0.5 (−VREF)
100.....000	0	0
010.....000	0.5 (−VREF)	0.5 (+VREF)
000.....000	−VREF	+VREF

TIMING AND PERFORMANCE

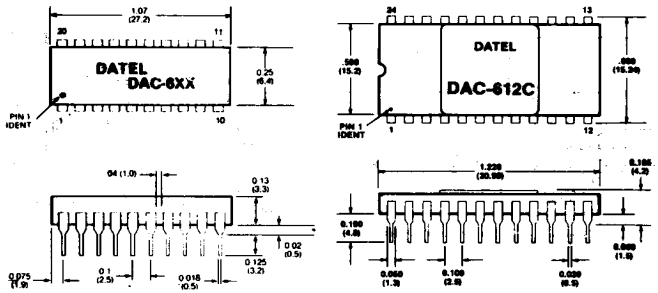
TIMING DIAGRAM



MODEL	A
DAC-608	90ns
DAC-610	200ns
DAC-612	90ns

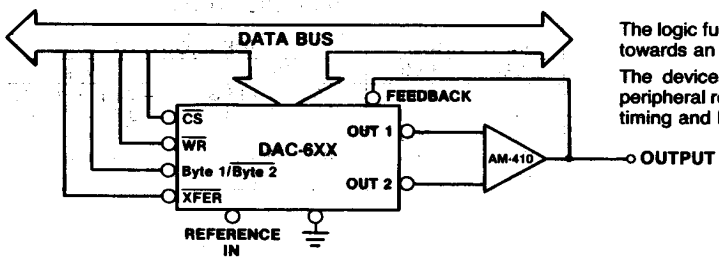
NOTE:
1. Settling time is measured from the leading edge of the WR pulse.
2. All digital controls are level actuated.

MECHANICAL DIMENSIONS
INCHES (MM)



APPLICATIONS

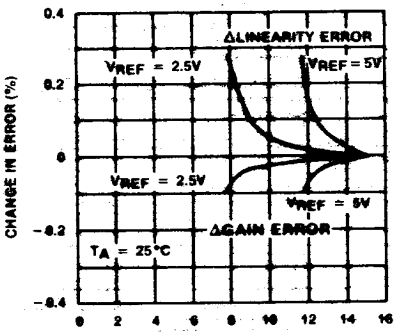
Typical Connection to Popular Microprocessor Data Bus



The logic functions of the DAC-608/610/612 have been oriented towards an ease of interface with all popular microprocessors.

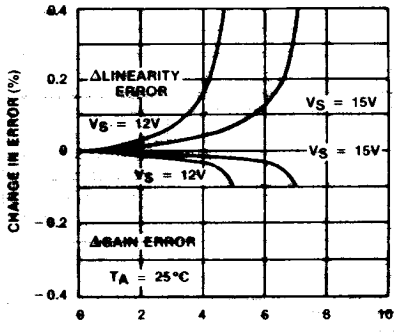
The devices are treated as a typical memory device or I/O peripheral requiring no external logic in most systems due to the timing and logic level convention of the input control signals.

DAC-608 Gain and Linearity Error Variation vs. Supply Voltage



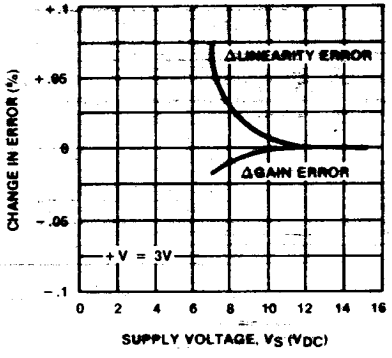
VOLTAGE MODE OPERATION

DAC-608 Gain and Linearity Error Variation vs. Reference Voltage

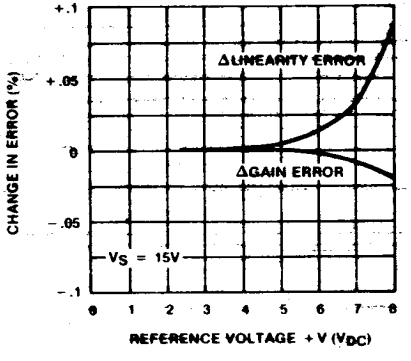


VOLTAGE MODE OPERATION

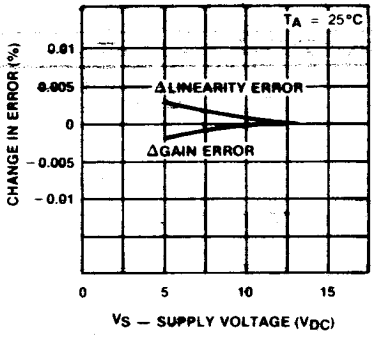
DAC-610 Gain and Linearity Error Variation vs. Supply Voltage



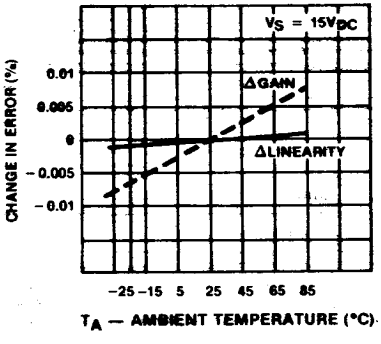
DAC-610 Gain and Linearity Error Variation vs. Reference Voltage



DAC-612 Gain and Linearity Error Variation vs. Supply Voltage

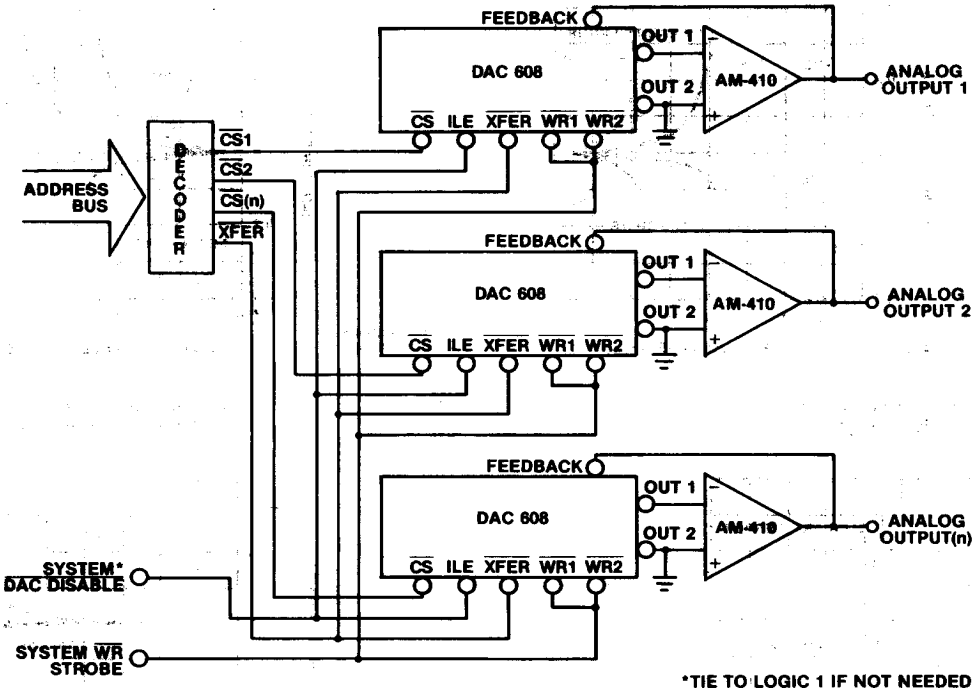


DAC-612 Gain and Linearity Error Variation vs. Temperature



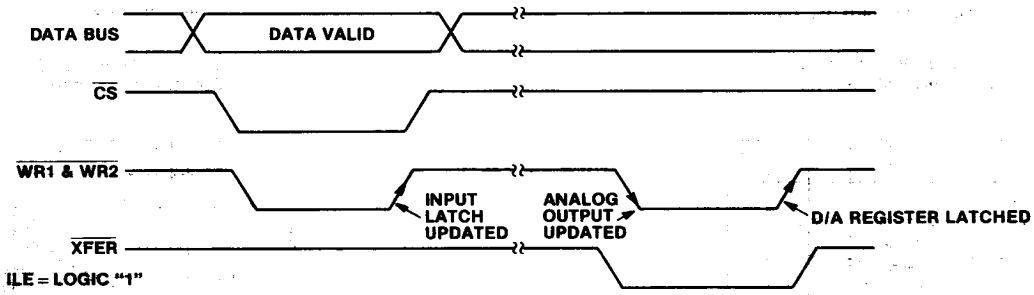
APPLICATIONS

MULTIPLE D/A SYSTEM



*TIE TO LOGIC 1 IF NOT NEEDED

TIMING DIAGRAM



For simultaneous updating of multiple D/A's, the $\overline{CS}$ line of each device is decoded individually. However, the converter can share a common $\overline{XFER}$.

The ILE function is very useful in applications where more than one processor is being used. If another processor took control of the data bus and control lines using the same addresses as the first, a low on the ILE pin would latch the data in the input register holding the outputs at their present state.

ORDERING INFORMATION

MODEL NO.	RESOLUTION	OPERATING TEMP. RANGE
DAC-608C	8 Bits	0°C to +70°C
DAC-610C	10 Bits	0°C to +70°C
DAC-612C	12 Bits	