SONY

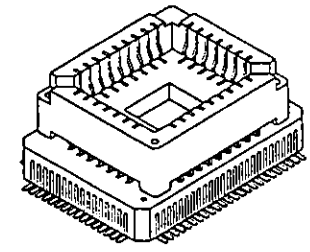
# CXP50700

## CMOS 4-bit Single Chip Microcomputer — Piggyback type

### Description

The CXP50700 is a CMOS 4-bit 1 chip microcomputer of piggyback/evaluator combined type which has been developed for functional evaluation of the CXP50712/CXP50716.

80 pin PQFP (Ceramic)



### Features

- Instruction cycle 1.9 µs/4.19MHz
  122 µs/32kHz
  (Selectable by program)
- ROM capacity Maximum 32K bytes
  (EPROM 27C256 LCC)
- RAM capacity 544 × 4 bits
  (Stack area not included)
  (32 × 4 bits is used in combination with the LCD display memory)
- 43 general purpose I/O ports
  (When all combined ports are used as ports)
- LCD controller/driver(Direct drive possible)
  — 16 to 32 segment outputs selectable through program
  — 1/2, 1/3, 1/4 duty static selectable through program
  — 1/2, 1/3 bias selectable through program
- 14-bit PWM output for D/A conversion
- Remote control receiving circuit
- 3-bit A/D converter (8 channels)
- 32kHz timer/event counter
- Power supply voltage detection reset circuit
- Low voltage operation (2.5V)
  ... during 122 µs/32kHz operation
- 8 large current output ports
- Rich wake up function
- 8-bit timer, 8-bit timer/event counter, 18-bit time base timer
- 8-bit/4-bit variable serial I/O
- 2 types of power down modes, sleep and stop
- Power on reset circuit (Mask option)
- 80 pin piggyback QFP

**Note)** Mask options are determined according to the CXP50700 category.
For details refer to the product list.

### Structure

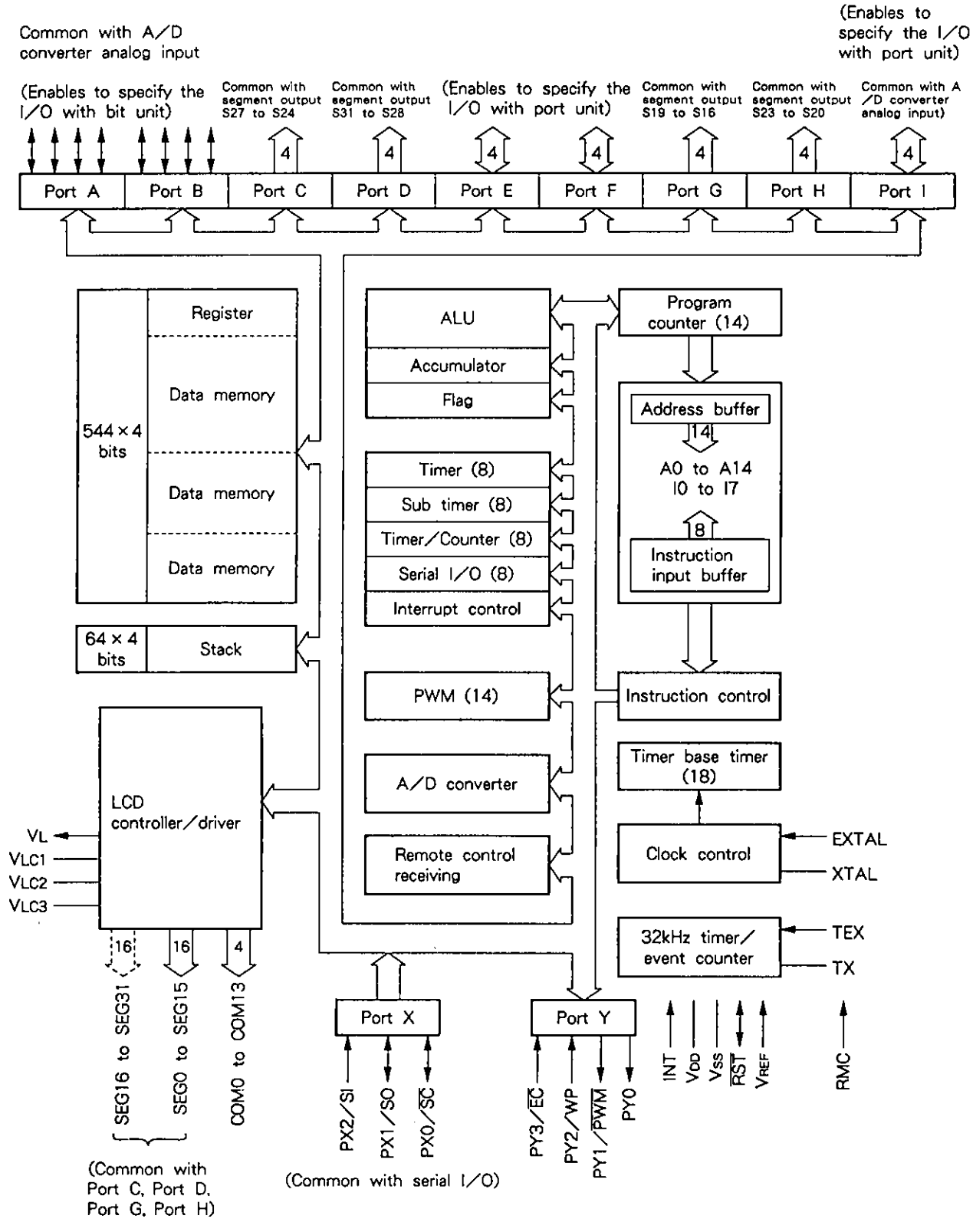
Silicon gate CMOS IC





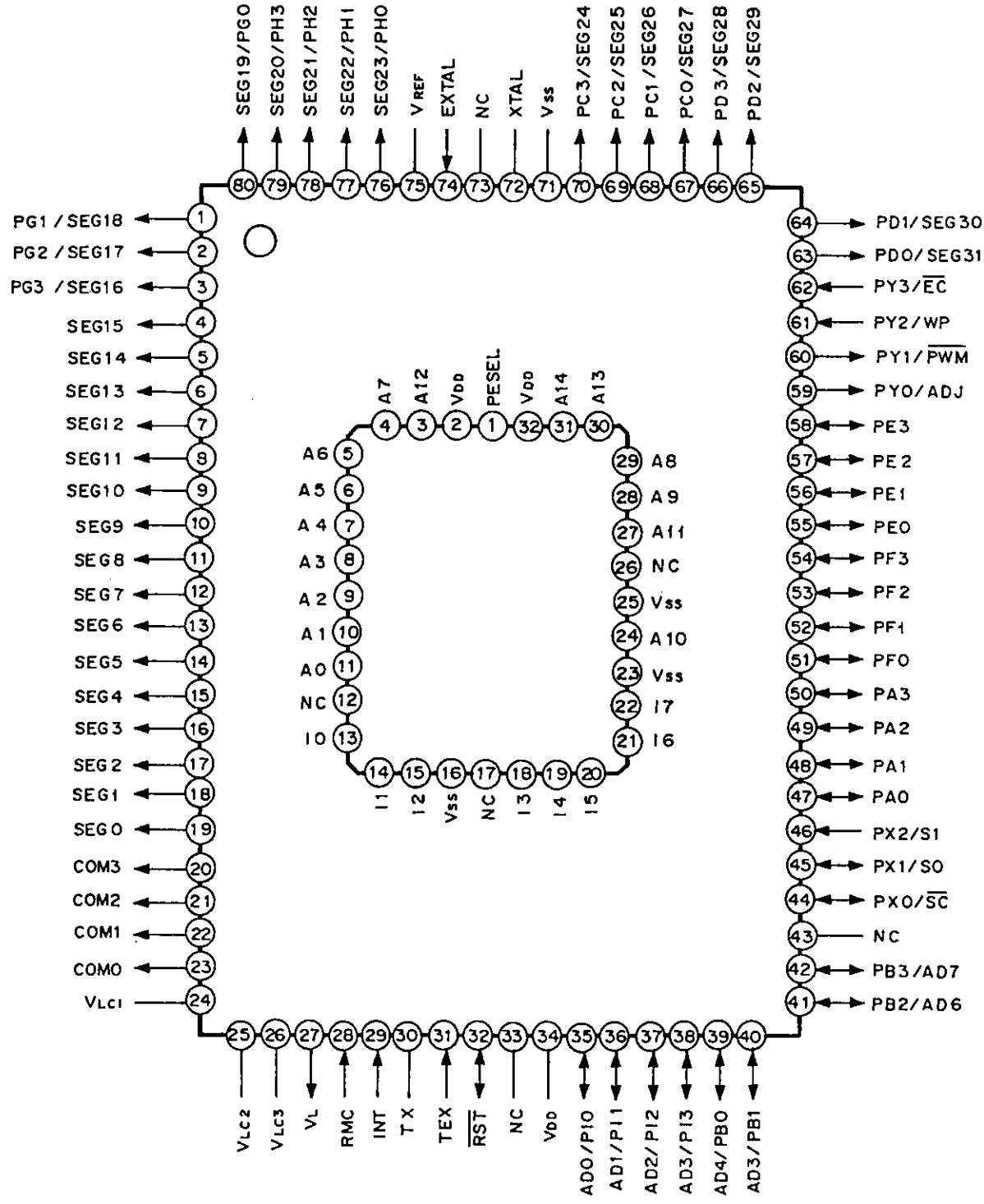
E90378 – ST

## Block Diagram

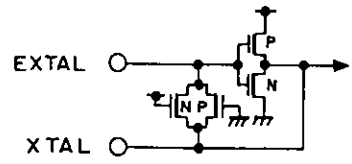
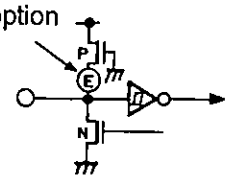
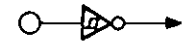
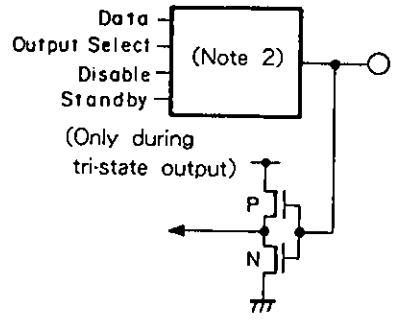


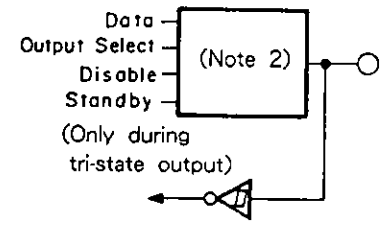
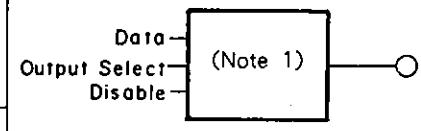
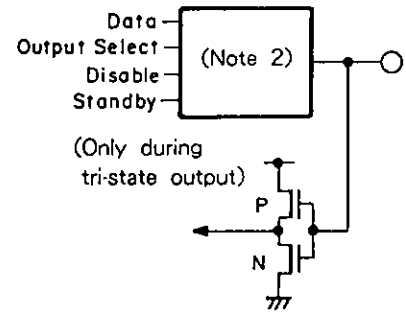
## Pin Configuration (Top View)

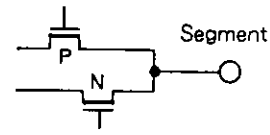
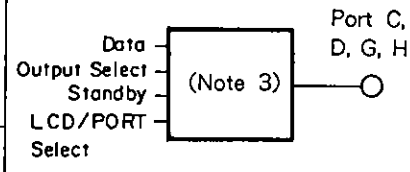
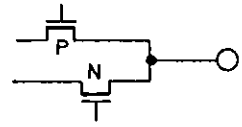
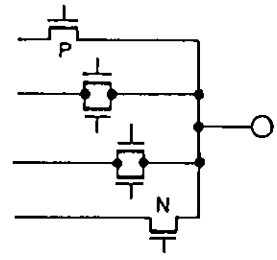
**Note** 1) Do not make any connections to NC pins.
2) Use 27C256 for EPROM.

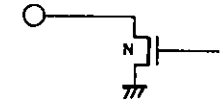
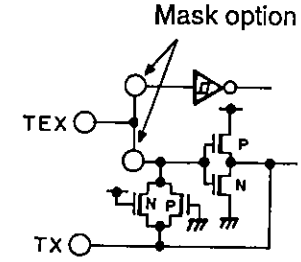


## Pin Description

| Symbol | Name | I/O | Description | Equivalent Circuit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | I | Positive voltage supply pin | |
| $V_{SS}$ | Grounding voltage | I | GND pin | |
| EXTAL | Clock input | I | Clock generating circuit input pin. Connect the crystal oscillator or ceramic resonator between the EXTAL and XTAL. To use an external clock input, connect the clock oscillation source to the EXTAL pin and open the XTAL pin. |   |
| XTAL | Clock output | O | Clock generating circuit output pin | |
| $\overline{RST}$ | Reset | I/O | Serves as the incorporated power-on reset circuit output pin. When inputting a reset signal from the outside, provide 2 instruction cycles or longer of an "L" level (0V). | Mask option   Output pull-up resistor (P-ch Tr) N-ch Tr output Schmitt inverter input |
| INT | External interrupt | I | Serves as interrupt input pin. Permits the selection with a program of the edge and the level modes. |  Schmitt inverter input |
| RMC | Remote control input | I | Remote control receiver input pin | |
| PX2/SI | Port X2/ Serial input | I | Doubles as a serial interface (8 bits) input pin and as bit "2" (input) of port X. | |
| PX1/SO | Port X1/ Serial output | I/O | Doubles as a serial data output pin for the serial interface and as bit "1" (input) of port X. (SO output possible to inhibit with the program.) |   See Note 2) for the output circuit format. Inverter input |

| Symbol | Name | I/O | Description | Equivalent Circuit |
|---|---|---|---|---|
| PX0/$\overline{SC}$ | Port X0/ Serial clock | I/O | Doubles as shift clock input/output pin for the serial I/O and as bit "0" (input) of port X. |   See Note 2) for the output circuit format. Schmitt inverter input |
| PY3/$\overline{EC}$ | Port Y3/ Event count input | I | Doubles as event counter (8 bits) input pin and as bit "3" (input) of port Y. |  Schmitt inverter input |
| PY2/WP | Port Y2/ Wake-up input | I | Doubles as wake-up input pin to reset the standby state and as bit "2" (input) of port Y. | |
| PY1/$\overline{PWM}$ | Port Y1/ PWM generator output | O | Doubles as PWM generator (14 bits) output pin and as bit "1" (output) of port Y. |   See Note 1) for the output circuit format. |
| PY0/ADJ | Port Y0/Frequency adjustment | O | Doubles as output pin for bit "0" of port Y and as 32kHz T/C prescalar output | |
| PA0 to PA3 | Port A | I/O | This 4-bit input/output port permits its each individual bit to be programmed to serve either as input or output. For the output format, a tri-state and pull-up resistor possible to be programmed, and it is also used as the standby resetting pin. |   See Note 2) for the output circuit format. Inverter input |
| PB0/AD4 to PB3/AD7 | Port B/ Analog voltage input | I/O | This 4-bit input/output port has the functions that are equivalent to those of port A. It is also used for A/D converter input. | |
| PE0 to PE3 | Port E | I/O | This 4-bit input/output port permits its each individual port to be programmed to serve either as input or output. For the output format, a tri-state and pull-up resistor possible to be programmed. | |
| PF0 to PF3 | Port F | I/O | This 4-bit input/output port has the functions that are equivalent to those of port E. | |
| PI0/AD0 to PI3/AD3 | Port I/ Analog voltage input | I/O | This 4-bit input/output port has the functions that are equivalent to those of port E. It is also used for A/D converter input. | |

| Symbol | Name | I/O | Description | Equivalent Circuit |
|---|---|---|---|---|
| PD0/ SEG31 to PD3/ SEG28 | Port D/ Segment output | O | Doubles as a 4-bit output port (For the output format, the inverter and pull-up resistor possible to be programmed.) and as the segment signal output pin for LCD. |   The transfer gate input signal is controlled based on 1/2, 1/3 bias methods in advance. |
| PC0/ SEG27 to PC3/ SEG24 | Port C/ Segment output | O | Doubles as a 4-bit output port (The output format is equivalent to port D.) and as the segment signal output pin for LCD. | |
| PH0/ SEG23 to PH3/ SEG20 | Port H/ Segment output | O | Doubles as a 4-bit output port (The output format is equivalent to port D.) and as the segment signal output pin for LCD. (Possible to designate in bit units.) |   |
| PG0/ SEG19 to PG3/ SEG16 | Port G/ Segment output | O | Doubles as a 4-bit output port (The output format is equivalent to port D.) and as the segment signal output pin for LCD. | See Note 3) for the output circuit format. |
| SEG0 to SEG15 | Segment output | O | Segment signal output pin for LCD |   The transfer gate input signal is controlled based on respective bias methods in advance. |
| COM0 to COM3 | Common output | O | Common signal output pin for LCD |   Transfer gate output |

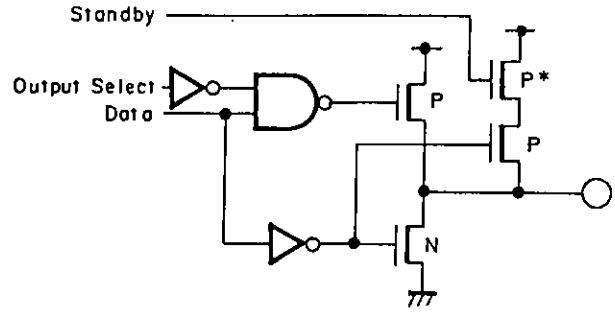
| Symbol | Name | I/O | Description | Equivalent Circuit |
|---|---|---|---|---|
| $V_{LC1}$ to $V_{LC3}$ | Power supply for LCD | — | Bias power supply pin for LCD | |
| $V_L$ | Cut-off output | O | Control pin which cuts off the current input to the bias resistor for the external LCD during standby. |   |
| TEX | 32kHz T/C clock input | I | Input pin for 32kHz timer clock generating circuit. Connect the 32.768kHz crystal oscillator between the TEX and TX. When using as the event clock input, connect the clock oscillation source to the TEX pin and open the TX pin. |   |
| TX | 32kHz T/C clock output | O | Output of clock generating circuit | |
| $V_{REF}$ | Reference voltage input | I | Reference voltage input for power supply voltage resetting circuit. Connect the zener diode normally. | |

For all output ports, the output states of ports during standby possible to be programmed the state holding before standby or the change to the high impedance.

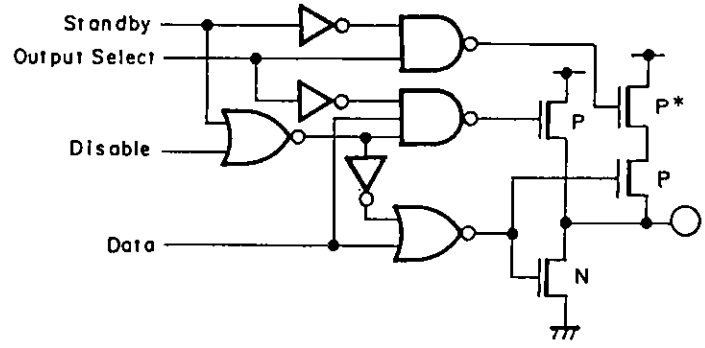
When the pull-up resistor is selected, it becomes a pulled-up state even it is input port.

During standby, it is impossible to change to the high impedance of PY0 and PY1 in the inverter output state. To change to the high impedance, select the pull-up resistor output, and then set to the high level output ("1" state).

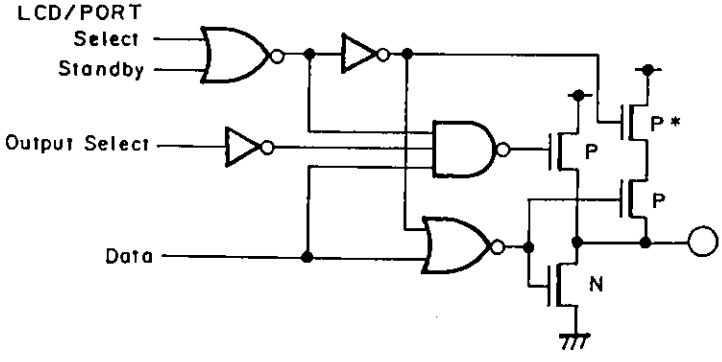
**Note 1)** Possible to select out of the following two ways for the output circuit format. (port units:programmable)
(a) Inverter output
(b) Pull-up resistor output




**Note 2)** Possible to select out of the following two ways for the output circuit format. (port units:programmable)
(a) Tri-state output
(b) Pull-up resistor output




**Note 3)** Possible to select out of the following two ways for the output circuit format. (port units:programmable)
(a) Inverter output
(b) Pull-up resistor output




* As the output pull-up resistor is CMOS pull-up output of about 10kΩ , the pull-up resistor becomes OFF state during "L" output.

## Absolute Maximum Ratings

| Item | Symbol | Rating | Unit | Remarks |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | − 0.3 to +7.0 | V | |
| LCD bias voltage | $V_{LC1}$, $V_{LC2}$, $V_{LC3}$ | − 0.3 to +7.0 *1 | V | |
| Input voltage | $V_{IN}$ | − 0.3 to +7.0 *1 | V | |
| Output voltage | $V_{OUT}$ | − 0.3 to +7.0 *1 | V | |
| High level output current | $I_{OH}$ | − 5 | mA | General purpose port *2: per pin |
| High level total output current | $\Sigma I_{OH}$ | − 50 | mA | Entire pins total |
| Low level output current | $I_{OL}$ | 15 | mA | General purpose port *2 : per pin |
| | $I_{OLC}$ | 20 | mA | High current port *3: per pin |
| Low level total output current | $\Sigma I_{OL}$ | 100 | mA | Entire pins total |
| Operating temperature | Topr | − 20 to +75 | °C | |
| Storage temperature | Tstg | − 55 to +150 | °C | |
| Allowable power dissipation *4 | $P_D$ | 600 | mW | QFP |

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1) $V_{LC1}$, $V_{LC2}$, $V_{LC3}$, $V_{IN}$ and $V_{OUT}$ should not exceed $V_{DD}$+0.3V.
*2) Specifies the output current of the general purpose I/O port PA to PI, SO, $\overline{SC}$, PY0 and PY1.
*3) The high current operation transistors are the N-CH transistors of the PC and PD ports.
*4) Except for EPROM allowable power dissipation

## Recommended Operating Conditions

(Vss=0V)

| Item | Symbol | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | 4.5 | 5.5 | V | Guaranteed range of operation by EXTAL clock |
| | | 2.5 | 5.5 | V | Guaranteed range of operation by TEX clock, guaranteed range of data hold during STOP. |
| LCD bias voltage | $V_{LC1}$, $V_{LC2}$, $V_{LC3}$ | $V_{SS}$ | $V_{DD}$ | V | Liquid crystal power supply range *1 |
| High level input voltage | $V_{IH}$ | 0.7$V_{DD}$ | $V_{DD}$ | V | |
| | $V_{IHS}$ | 0.8$V_{DD}$ | $V_{DD}$ | V | Hysteresis input *2 |
| | $V_{IHEX}$ | $V_{DD}$–0.4 | $V_{DD}$+0.3 | V | EXTAL pin *3 |
| Low level input voltage | $V_{IL}$ | 0 | 0.3$V_{DD}$ | V | |
| | $V_{ILS}$ | 0 | 0.2$V_{DD}$ | V | Hysteresis input *2 |
| | $V_{ILEX}$ | − 0.3 | 0.4 | V | EXTAL pin *3 |
| Operating temperature | Topr | − 20 | +75 | °C | |

*1) The optimum value is determined by the characteristics of the liquid crystal display element used.
*2) The TEX pin when the counter mode is selected by each of INT, RMC, PX0, PX2, PY2, PY3, $\overline{RST}$ pins and mask option.
*3) Specified only during external clock input.

## Electrical Characteristics
## DC Characteristics

(Ta= − 20 to +75 °C, Vss=0V)

| Item | Symbol | Pin | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| High level output voltage | $V_{OH}$ | PA to PI*1, PX0, PX1, PY0, PY1, $V_L$ ($V_{OL}$ only), $\overline{RST}$ ($V_{OL}$ only), PC*1, PD*1 | $V_{DD}$=4.5V, $I_{OH}$= −0.5mA*2 | 4.0 | | | V |
| | | | $V_{DD}$=4.5V, $I_{OH}$= −1.0mA*2 | 3.5 | | | V |
| | | | $V_{DD}$=4.5V, $I_{OH}$= −10 µA*3 | 4.0 | | | V |
| | | | $V_{DD}$=4.5V, $I_{OH}$= −200 µA*3 | 2.4 | | | V |
| Low level output voltage | $V_{OL}$ | | $V_{DD}$=4.5V, $I_{OL}$=1.8mA | | | 0.4 | V |
| | | | $V_{DD}$=4.5V, $I_{OL}$=3.6mA | | | 0.6 | V |
| | | | $V_{DD}$=4.5V, $I_{OL}$=12mA | | | 1.5 | V |
| Input current | $I_{IHE}$ | EXTAL | $V_{DD}$=5.5V, $V_{IH}$=5.5V | 0.5 | | 40 | µA |
| | $I_{ILE}$ | | $V_{DD}$=5.5V, $V_{IL}$=0.4V | −0.5 | | −40 | µA |
| | $I_{IHT}$ | TEX*4 | $V_{DD}$=5.5V, $V_{IH}$=5.5V | 0.1 | | 10 | µA |
| | $I_{ILT}$ | | $V_{DD}$=5.5V, $V_{IL}$=0.4V | −0.1 | | −10 | µA |
| | $I_{ILR}$ | $\overline{RST}$*5 | | −1.5 | | −400 | µA |
| | $I_{IL}$ | PA*6, PB*6, PE*6, PF*6, PI*6, PX0*6, PX1*6, PX2*8, PY0*7, PY1*7, PY2*8, PY3*8, INT*8, RMC*8, $\overline{RST}$*5, TEX*4 | | | | ±10 | µA |
| High impedance I/O leakage current | $I_{IZ}$ | | $V_{DD}$=5.5V | | | ±10 | µA |
| Common output impedance | $R_{COM}$ | COM0 to COM3 | $V_{DD}$=5V, $V_{LC1}$=3.75V, $V_{LC2}$=2.5V, $V_{LC3}$=1.25V | | 3 | 5 | kΩ |
| Segment output impedance | $R_{SEG}$ | SEG0 to SEG15, SEG16 to SEG3*1 | | | 5 | 15 | kΩ |
| Supply current*9 | $I_{DD1}$ | $V_{DD}$ | Entire output pins open; $V_{DD}$=5.5V, 4.19MHz Crystal oscillation (C1=C2=22pF) | | 7 | 20 | mA |
| | $I_{DD2}$ | | $V_{DD}$=3V, 32kHz Crystal oscillation (C1=C2=18pF) | | 50 | 250 | µA |
| | $I_{DDSP1}$ | | SLEEP mode; $V_{DD}$=5.5V, 4.19MHz oscillation | | 5 | 12 | mA |
| | $I_{DDSP2}$ | | $V_{DD}$=3V, 32kHz oscillation | | 40 | 200 | µA |
| | $I_{DDS1}$ | | STOP mode; $V_{DD}$=3V, with 32kHz T/C | | 7 | 40 | µA |
| | $I_{DDS2}$ | | $V_{DD}$=3V, without 32kHz T/C (For mask option select counter) | | | 10 | µA |
| Input capacity | $C_{IN}$ | Other than $V_{LC1}$ to $V_{LC3}$, COM0 to COM3, SEG0 to SEG15, SEG16 to SEG31, *1 $V_{DD}$, Vss pins | Clock 1MHz, 0V other than the measured pins | | 10 | 20 | pF |

*1) The PC, PD, PG and PH show when the combined pins are selected as the port, and SEG16 to SEG31 show when the combined pins are selected as the segment output.
*2) It is when the respective pins of PA to PI, PX0 and PX1 select the tri-state output circuit, and PY0 and PY1 are when the inverter output circuit is selected.
*3) It is when the respective pins of PA to PI, PX0, PX1, PY0 and PY1 select the pull-up resistor.
*4) The TEX pin specifies the input current when the crystal oscillation is selected by the mask option, and specifies the leakage current when the schmitt input is selected.
*5) The $\overline{RST}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.
*6) The respective pins of PA, PB, PE, PF, PI, PX0 and PX1 specify the input current when the pull-up resistor is selected, and specify the leakage current when the port state during using the tri-state output circuit or standby is selected at high impedance.
*7) The respective pins of PY0 and PY1 specify the input current when the pull-up resistor is selected, and specify the leakage current when the port state during standby is selected at high impedance.
*8) The respective pins of PX2, PY2, PY3, INT and RMC only specify the leakage current.
*9) Except for EPROM power supply current.

## AC characteristics

(1) Clock timing (Ta= − 20 to +75 °C, $V_{DD}$=4.5 to 5.5V, Vss=0V)

| Item | Symbol | Pin | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| System clock frequency | fc | XTAL<br>EXTAL | Fig. 1, Fig. 2 | 1 | | 5 | MHz |
| System clock input pulse width | $t_{XL}$<br>$t_{XH}$ | EXTAL | Fig. 1, Fig. 2<br>(External clock drive) | 90 | | | ns |
| System clock input rising and falling times | $t_{CR}$<br>$t_{CF}$ | | | | | 200 | ns |
| System clock frequency | fcs | TEX*2<br>TX | $V_{DD}$=2.5 to 5.5V<br>Fig. 3 | | 32.768 | | kHz |
| Event count clock input pulse width | $t_{EL}$<br>$t_{EH}$ | $\overline{EC}$ | Fig. 4 | tsys*1<br>+0.05 | | | µs |
| Event count clock input rising and falling times | $t_{ER}$<br>$t_{EF}$ | $\overline{EC}$ | Fig. 4 | | | 20 | ms |
| Event count input clock input pulse width | $t_{TL}$<br>$t_{TH}$ | TEX*3 | Fig. 4 | 10 | | | µs |
| Event count input clock rising and falling times | $t_{TR}$<br>$t_{TF}$ | TEX*3 | Fig. 4 | | | 20 | ms |

*1) tsys in the EXTAL input clock is 8/fc
tsys in the TEX input clock is 4/fcs
*2) Specified when the crystal oscillation mode is selected by the mask option.
*3) Specified when the counter mode is selected by the mask option.

**Note)** When adjusting the frequency accurately, there may be cases in which they may differ from Fig. 2.

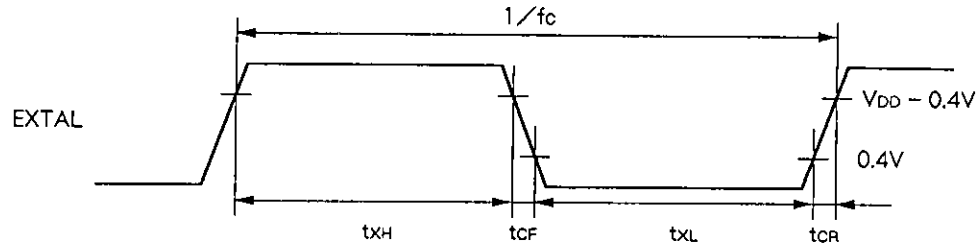



**Fig. 1 Clock timing**

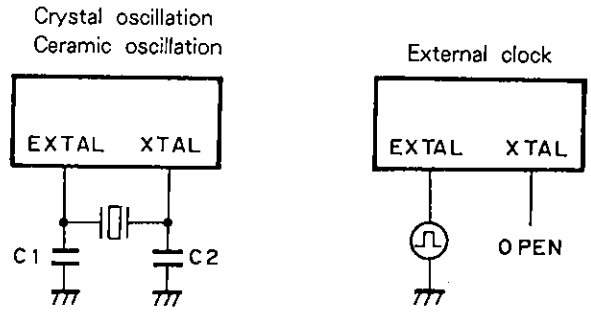



**Fig. 2 Clock applying condition**

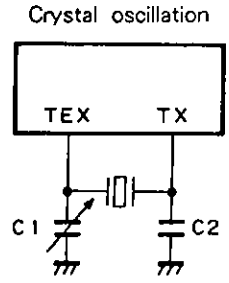



**Fig. 3 32kHz clock applying condition**

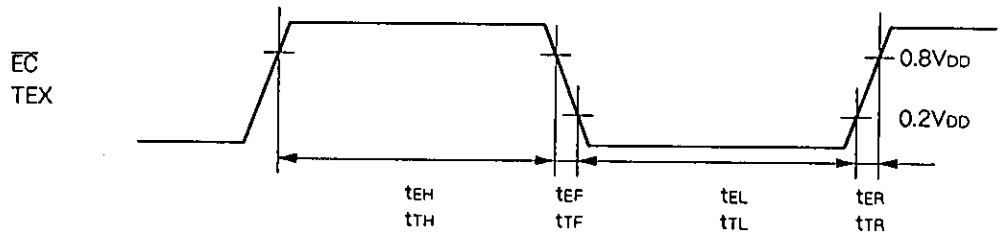



**Fig. 4 Event count clock timing**

(2) Serial transfer (Ta= − 20 to +75 °C , $V_{DD}$=4.5 to 5.5V, $V_{SS}$=0V)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Serial transfer clock ($\overline{SC}$) cycle time | $t_{KCY}$ | $\overline{SC}$ | Input mode | tsys/4+1.42 | | µs |
| | | | Output mode | 2tsys | | µs |
| Serial transfer clock ($\overline{SC}$) high and low level widths | $t_{KH}$ $t_{KL}$ | $\overline{SC}$ | Input mode | tsys/8+0.7 | | µs |
| | | | Output mode *1 | tsys − 0.1 | | µs |
| | | | Output mode *2 | tsys − 1.6 | | µs |
| Serial data input setup time (against $\overline{SC}$ ↑ ) | $t_{SIK}$ | SI | $\overline{SC}$ input mode | 0.1 | | µs |
| | | | $\overline{SC}$ output mode | 0.2 | | µs |
| Serial data input hold time (against $\overline{SC}$ ↑ ) | $t_{KSI}$ | SI | $\overline{SC}$ input mode | tsys/8+0.5 | | µs |
| | | | $\overline{SC}$ output mode | 0.1 | | µs |
| High data delay time from $\overline{SC}$ falling *3 | $t_{KSO}$ | SO | | | tsys/8+0.5 | µs |
| High data delay time from $\overline{SC}$ falling *4 | $t_{KSO}$ | SO | | | tsys/8+1.6 | µs |
| Low data delay time from $\overline{SC}$ falling | $t_{KSO}$ | SO | | | tsys/8+0.5 | µs |

**Note)** tsys in the EXTAL input clock is 8/fc. (It is impossible to use in TEX input clock.)

*1) It is specified when $\overline{SC}$ pin is selected to the tri-state output by the program.

*2) It is specified when $\overline{SC}$ pin is selected to the pull-up resistance by the program.
As the tsys receives restriction by this item, take notice that it limits the upper limit of the system clock frequency fc.

*3) It is specified when SO pin is selected to the tri-state output by the program.

*4) It is specified when SO pin is selected to the pull-up resistance by the program.

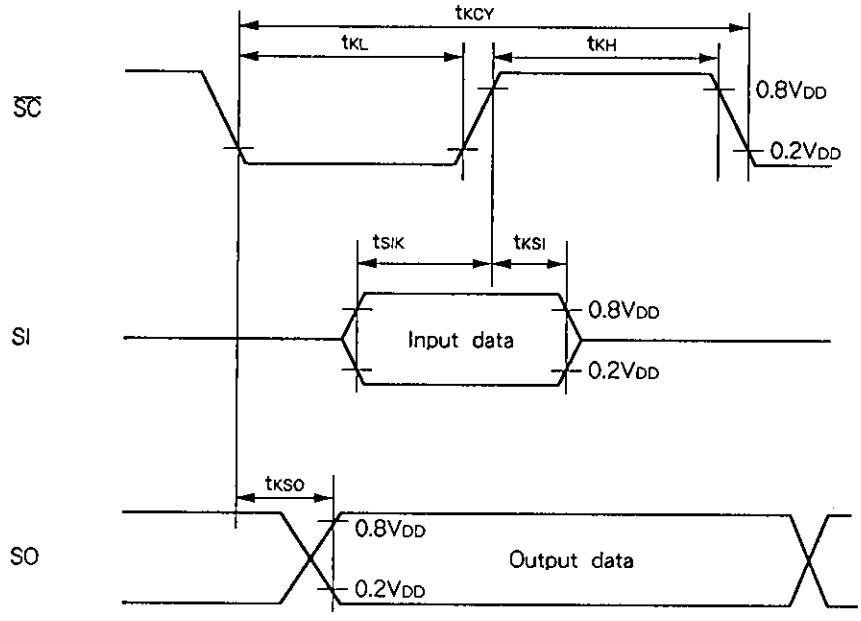



**Fig. 5 Serial transfer timing**

(3) A/D converter (Ta= − 20 to +75 °C, Vss=0V)

| Analog input voltage | Pin | Condition | Digital conversion value |
|---|---|---|---|
| 0.0 to 0.33V | AD0 to AD7 | $V_{DD}$=5V | 000 |
| 0.82 to 1.29V | | | 001 |
| 1.78 to 2.21V | | | 010 |
| 2.69 to 3.06V | | | 011 |
| 3.56 to 4.06V | | | 100 |
| 4.62 to 5.0V | | | 101 |

**Note)** The digital conversion value are the values when C9H address in the program are read.

(4) Power supply voltage detection reset function (Ta= − 20 to +75 °C, Vss=0V)

| Item | Symbol | Pin | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Power supply voltage detection reset function of operation voltage range | $V_{LPOP}$ | $V_{DD}$ | Voltage range allowing system operation (32kHz system operation below $V_{DD}$=4.5V) | 2.5 | | 5.5 | V |
| Power supply voltage drop detection function | $V_{POP}$ | $V_{DD}$ | When $V_{REF}$ pin voltage is 3.3V<br>Flag set when voltage drops<br>System reset when voltage rises | 3.8 | 4.0 | 4.2 | V |

The graph in Fig. 6 shows the relationship between the power supply voltage $V_{DD}$ and reference voltage $V_{REF}$ of the power supply voltage detection reset function.

**Note)** The graph in Fig. 6 serves as guide to the function operation area obtained using average devices. Individual adjustment is needed when Zener diodes, etc., are connected to the $V_{REF}$ pin.

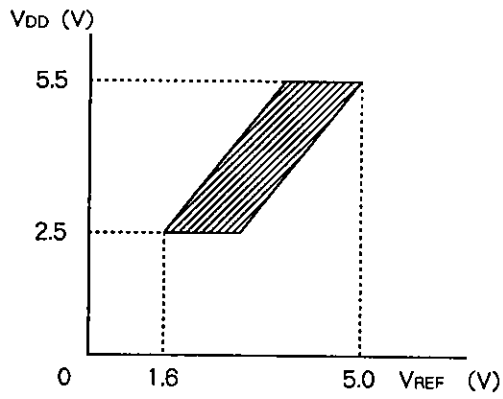



**Fig. 6 Power supply voltage detection reset function chart**

(5) Others

(Ta= − 20 to +75 °C, $V_{DD}$=4.5 to 5.5V, Vss=0V)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| External interruption high and low level widths | $t_{IH}$, $t_{IL}$ | INT | During edge detection mode | tsys+0.05 | | µs |
| Reset input low level width | $t_{RSL}$ | $\overline{RST}$ | | 2tsys * | | µs |
| Wake-up input high level width | $t_{WPH}$ | WP | STOP mode | 500 | | ns |
| | | | SLEEP mode | tsys+0.05 | | µs |
| Wake-up input low level width | $t_{WPL}$ | PA | STOP mode | 500 | | ns |
| | | | SLEEP mode | tsys+0.05 | | µs |

**Note)** tsys in the EXTAL input clock is 8/fc
tsys in the TEX input clock is 4/fcs

* For resetting when operating in TEX input clock, hold the low level more than the oscillation stabilizing time of EXTAL input clock.

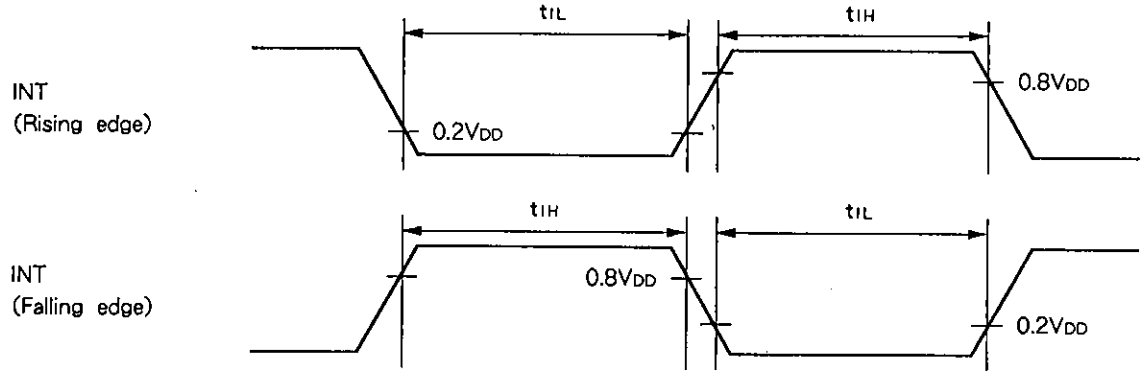



**Fig. 7 Interruption input timing**

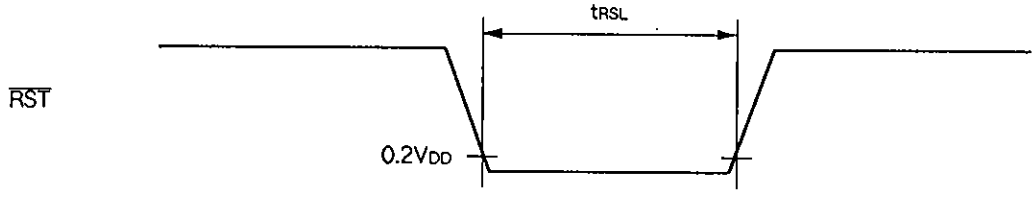



**Fig. 8 Reset input timing**

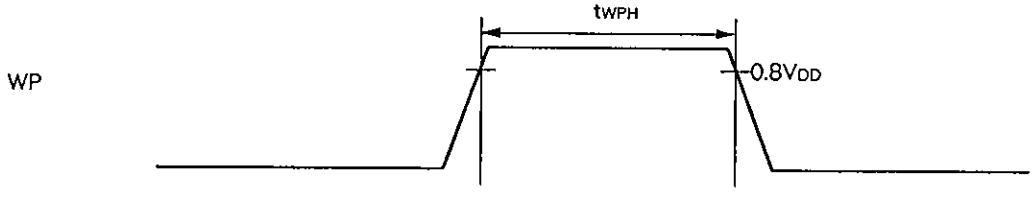



**Fig. 9 Wake-up input timing**

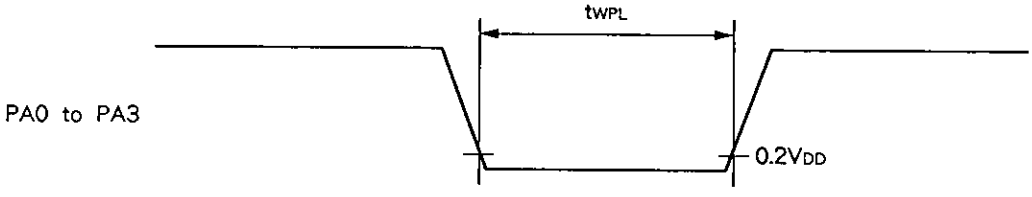



**Fig. 10 Wake-up input timing**

**Power on reset ***

(Ta= − 20 to +75 °C, Vss=0V)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power supply rising time | $t_R$ | $V_{DD}$ | Power on reset | 0.05 | 50 | ms |
| Power supply cut-off time | $t_{OFF}$ | | Repetitive power on reset | 1 | | ms |

* Specifies only when power on reset function is selected.

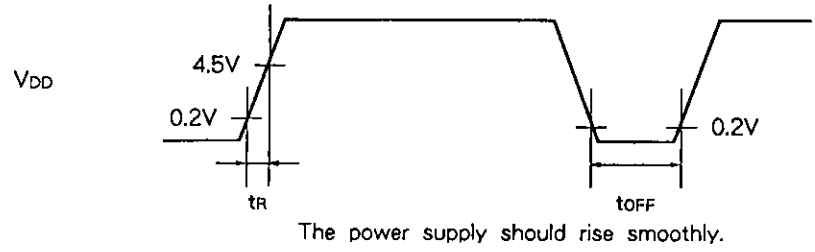



**Fig. 11 Power on reset**

## Notes on Operation

See Fig. 12, Additive capacity calculation chart, when using the crystal oscillator and select the appropriate capacity.

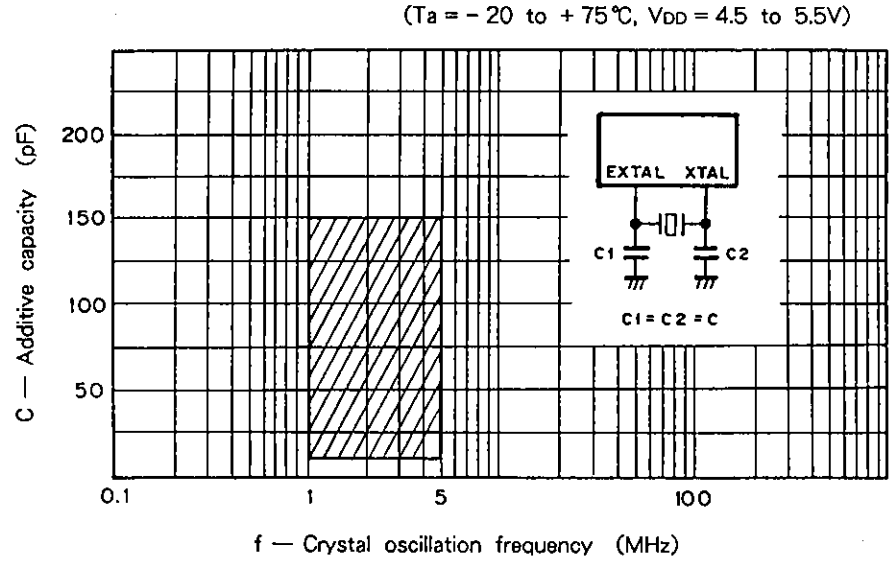
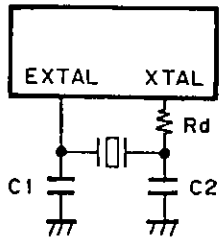



**Fig. 12 Crystal oscillation circuit additive capacity calculation chart**

**Note)** The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

Fig. 13 shows recommended circuits and oscillators. Use the trimmer capacitor to C1, in the case of accurate adjustment of the oscillation frequency.

(i) Main clock (4.19MHz)

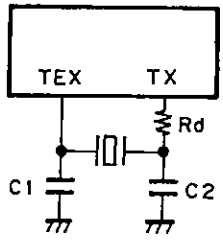



(i)

| Manufacturer | Model | Frequency range | C1 | C2 | Rd |
|---|---|---|---|---|---|
| MURATA MFG CO., LTD. | CSA4.19MG040 | 4.19 MHz | 100pF | 100pF | — |
| | CST4.19MGW040 | 4.19 MHz | — (built in) | — (built in) | — |

| Manufacturer | Model | Frequency range | C1 | C2 | Rd |
|---|---|---|---|---|---|
| CITIZEN WATCH CO., LTD. | CSA-309 | 4.19 MHz | 10pF (20pF trimmer) | 10pF | — |
| NIHON DEMPA KOGYO CO., LTD. | AT-51 | 4.19 MHz | 15pF (20pF trimmer) | 15pF | 6.8kΩ |
| KINSEKI LTD. | HC-49/U-S | 4.19 MHz | 22pF | 22pF | 3.3kΩ |

(ii) Sub clock (32kHz)

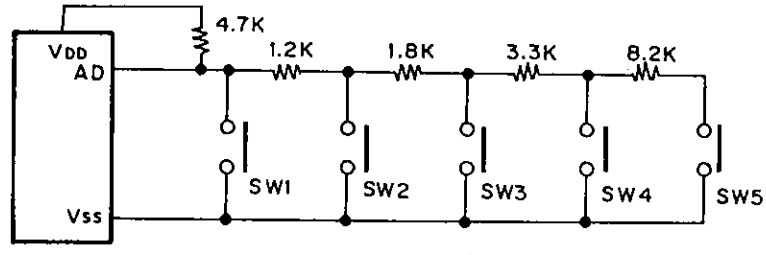



(ii)

| Manufacturer | Model | Frequency range | C1 | C2 | Rd |
|---|---|---|---|---|---|
| CITIZEN WATCH CO., LTD. | CFS-308 | 32.768 kHz | 18pF (20pF trimmer) | 18pF | — |
| NIHON DEMPA KOGYO CO., LTD. | MX-38T | 32.768 kHz | 22pF (20pF trimmer) | 22pF | 470kΩ |
| KINSEKI LTD. | P3 | 32.768 kHz | 22pF (20pF trimmer) | 22pF | 330kΩ |

**Fig. 13 Recommended oscillation circuit**

When using the A/D converter as the key input, it is recommended that the circuit structure shown in Fig. 14 be used.




(Resistance is all E12 series)

**Fig. 14 Recommended example of key circuit by A/D converter**

## EPROM read timing

(Ta=–20 to +75 °C, $V_{DD}$=4.5 to 5.5V, Vss=0V)

| Item | Symbol | Pin | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Address → data input delay time | $t_{ACC}$ | A0 to A14, I0 to I7 | | 300 | ns |
| Address → input holding time | $t_{IH}$ | A0 to A14, I0 to I7 | 0 | | ns |

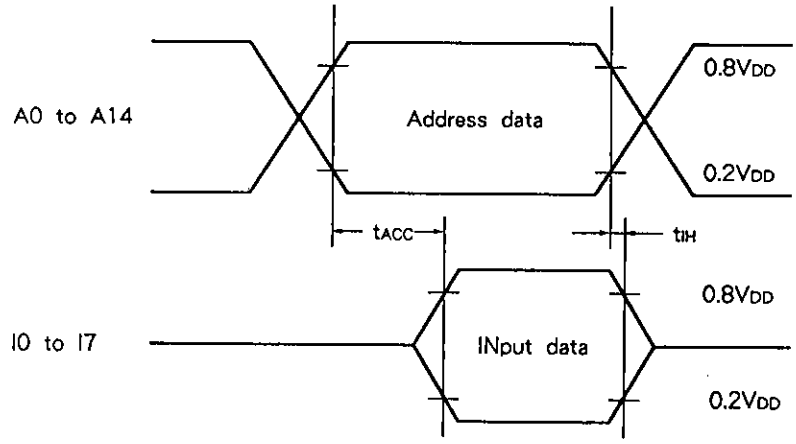
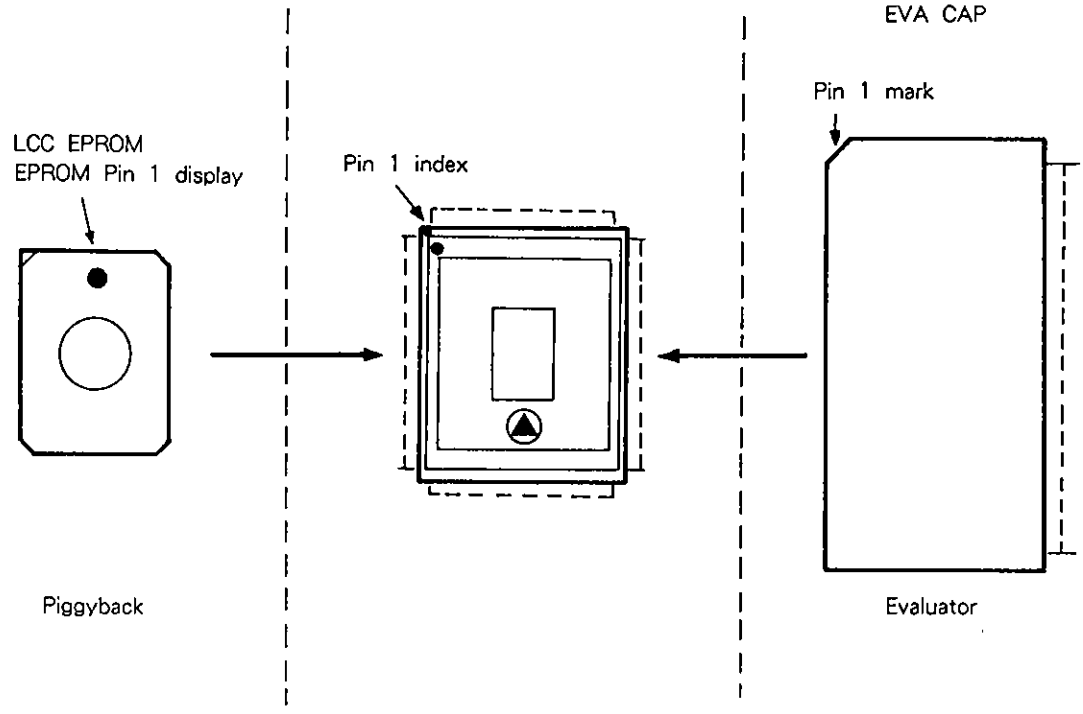



**Fig. 15 EPROM timing**

CXP50700's piggyback/evaluator switching is executed as shown in the diagram below.



## Products List

| Optional item | Mass product | CXP50700-U01 |
|---|---|---|
| Package | 80-pin plastic QFP | 80-pin ceramic QFP |
| ROM capacity | 12K-byte/16K-byte | EPROM 32K-byte |
| Pull-up resistance of reset pin | Existent/non-existent | Existent |
| Incorporated power on reset circuit | Existent/non-existent | Existent |
| 32kHz timer/counter | Timer/Counter | Timer mode |

**Note)** All the piggyback/evaluator is combined chips.

## Package Outline Unit : mm

80pin PQFP (Ceramic) 5.7g