

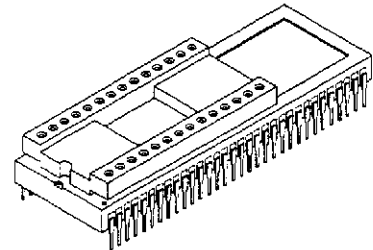
**Description**

The CXP50200 is a CMOS 4-bit microcomputer common with piggyback/evaluation chip which are developed for CXP50212/CXP50216 function evaluation.

**Features**

- Instruction cycle 1.9 $\mu$ s/4.19 MHz
- ROM capacity Maximum 32k bytes  
(EPROM 27C256 equipped)
- RAM capacity 544 $\times$ 4 bits  
(Including display area)
- 40 general purpose I/O ports
- 8 high current ports (Ports C, D)
- Fluorescent display panel controller/driver  
(Able to display maximum 256 segments)
  - 1 to 16 digits dynamic scan display  
(1 to 8 digits at 24 segments)
  - Page mode/variable mode
  - Dimmer function
  - High tension proof output (40 V)
  - Selection possible for incorporating pull-down resistance (mask option)
- 14-bit PWM output for D/A conversion
- Remote control receiving circuit (Be independent of the timer/counter)
- 3-bit A/D converter (1 channel per circuit)
- 8-bit/4-bit variable prescaler serial I/O
- 8-bit prescaler timer, 8-bit prescaler timer/event counter, 18-bit time base timer and 8-bit reload type timer with prescaler, independently controlled

64pin SDIP (Ceramic)



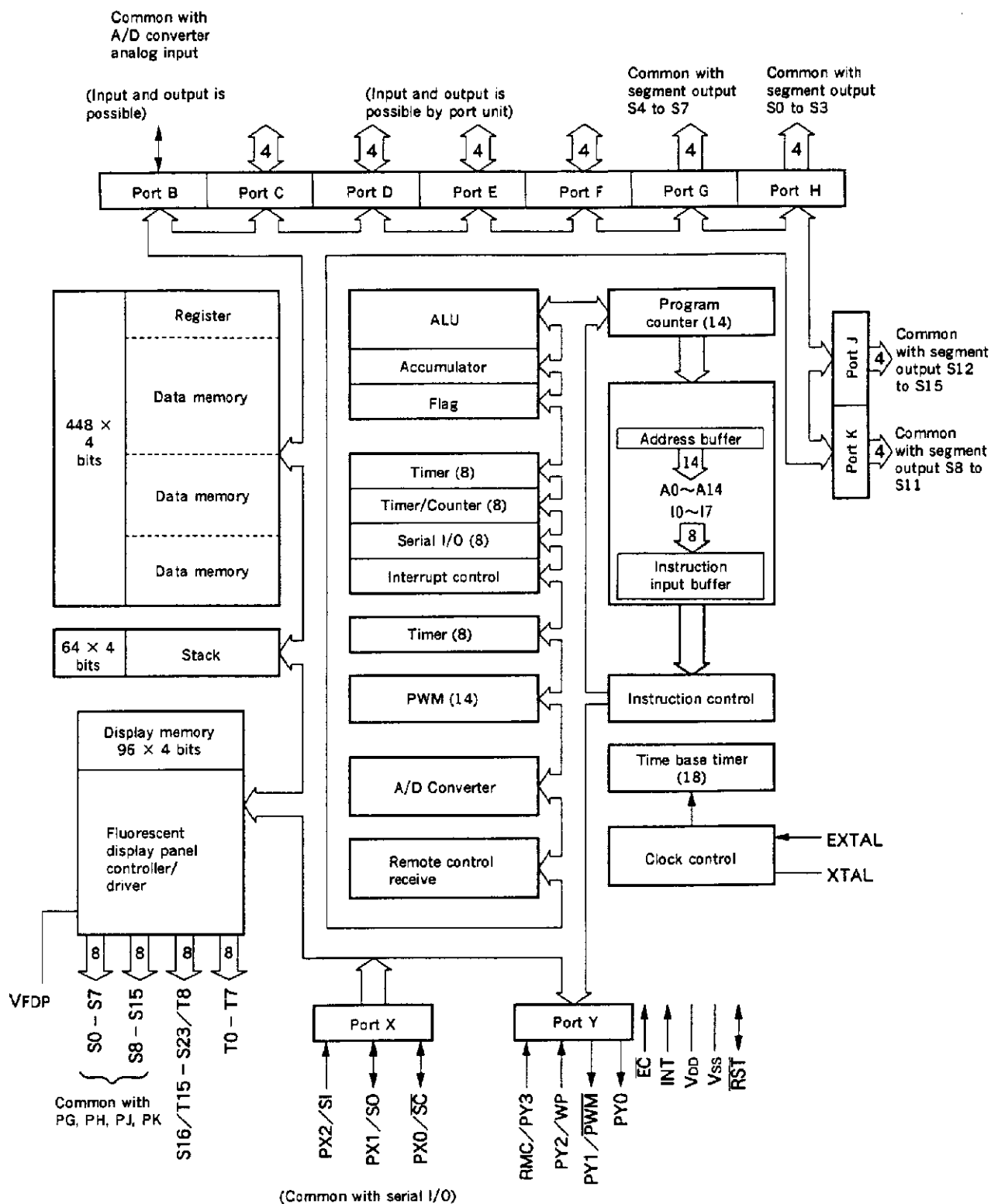
- Arithmetic and logical operations possible between the entire ROM area, I/O area and the accumulator by means of memory mapped I/O
- Reference to the entire ROM area is possible with the table look-up instruction
- 2 kinds of power down modes, sleep and stop
- Power on reset circuit (mask option)
- Provided with 64 pin ceramic SDIP

Note) The mask option is fixed according to a kind of CXP50200.  
See the List of Products for details.

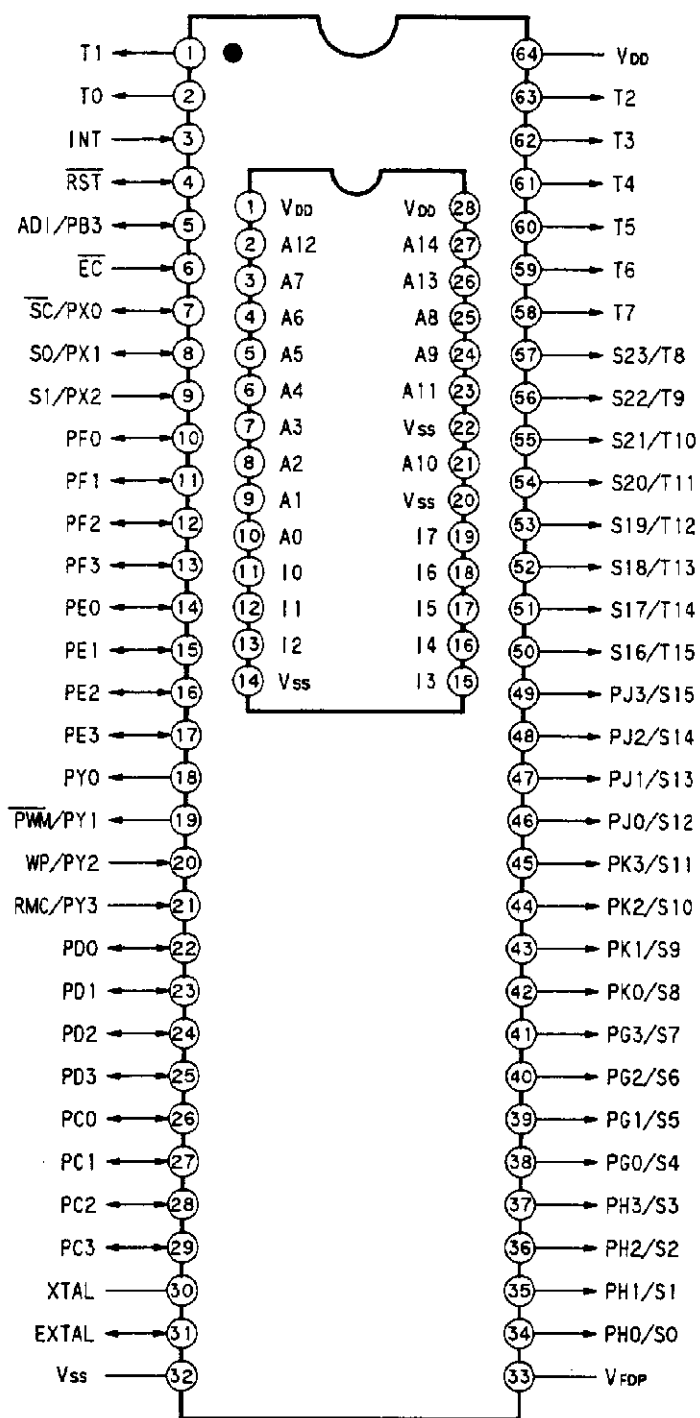
**Structure**

Silicon gate CMOS IC

## Block Diagram

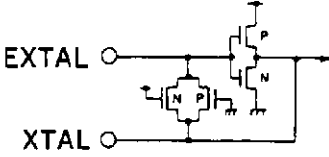
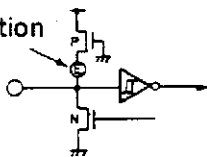
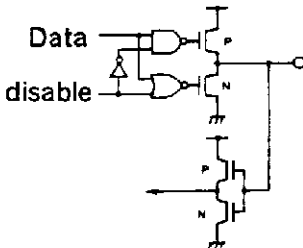
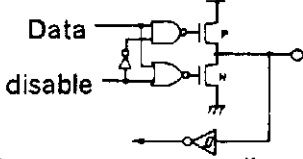


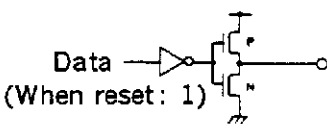
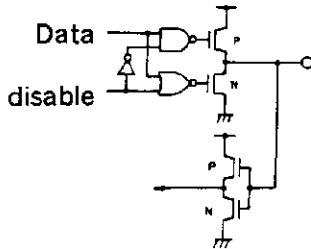
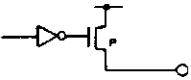
## Pin Configuration (Top View)



Note) Use 27C256 type for EPROM.

## Pin Description

| Symbol           | Name                | I/O | Description                                                                                                                                                                                                                        | Equivalent circuit                                                                                                                                                                            |
|------------------|---------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{DD}$         | Supply voltage      | I   | Positive voltage supply pin                                                                                                                                                                                                        |                                                                                                                                                                                               |
| $V_{SS}$         | Grounding voltage   | I   | GND pin                                                                                                                                                                                                                            |                                                                                                                                                                                               |
| EXTAL            | Clock input         | I   | Clock oscillation circuit input pin. Connect the crystal oscillator or ceramic oscillator between the EXTAL and XTAL. To use an external clock input, connect the clock oscillation source to the EXTAL pin and open the XTAL pin. |                                                                                                            |
| XTAL             | Clock output        | O   | Clock oscillation circuit output pin                                                                                                                                                                                               |                                                                                                                                                                                               |
| $\overline{RST}$ | Reset               | I/O | Serves as the incorporated power on reset circuit output pin. When inputting a reset signal from the outside, provide 2 instruction cycles or longer of an "L" level (0 V).                                                        | <p>Mask option</p>  <p>Output pull-up resistor (P-ch Tr)<br/>N-ch Tr output<br/>Schmitt inverter input</p> |
| INT              | External interrupt  | I   | Serves as interrupt input pin. Permits the selection with a program of the edge and the level modes.                                                                                                                               |  <p>Schmitt inverter input</p>                                                                           |
| EC               | Event counter input | I   | Event counter input pin.                                                                                                                                                                                                           |                                                                                                                                                                                               |
| SI/PX2           | Serial input Port X | I   | Combination pin of a serial interface (8 bits) input pin and bit "2" (input) of port X.                                                                                                                                            |  <p>3-state output or pull-up resistor<br/>output possible Inverter input</p>                            |
| SO/PX1           | Serial input Port X | I/O | Combination pin of a serial interface (8 bits) output pin and bit "1" (input) of port X.                                                                                                                                           |                                                                                                                                                                                               |
| SC/PX0           | Serial clock Port X | I/O | Combination pin of clock input/output pin for the serial interface and bit "0" (input) of port X.                                                                                                                                  |  <p>3-state output or pull-up resistor<br/>output possible Inverter input</p>                            |

| Symbol             | Name                               | I/O | Description                                                                                                                                                                                                      | Equivalent circuit                                                                                                                                           |
|--------------------|------------------------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RMC/PY3            | Remote control signal input Port Y | I   | Combination pin of remote control receiver input pin and bit "3" (input) of port Y.                                                                                                                              | <br>Schmitt inverter input                                                |
| WP/PY2             | Wake-up input Port Y               | I   | Combination pin of a wake-up input pin to release the standby state and bit "2" (input) of port Y.                                                                                                               |                                                                                                                                                              |
| PWM/PY1            | PWM output Port Y                  | O   | Combination pin of a PWM generator (14 bits) output and bit "1" (output) of port Y.                                                                                                                              | <br>Inverter output                                                       |
| PY0                | Port Y                             | O   | Output pin for bit "0" of port Y.                                                                                                                                                                                |                                                                                                                                                              |
| PB3/ADI            | Analog input Port B                | I/O | This 1-bit input/output port permits its each individual port to be programmed to serve for input or output. Its output format is a 3-state or pull-up resistor output. It is also used for A/D converter input. | <br>3-state output or pull-up resistor output possible<br>Inverter input |
| PC to PC3          | Port C                             | I/O | This 4-bit input/output port permits its each individual port to be programmed to serve for input or output. Its output format is a 3-state or pull-up resistor output.                                          |                                                                                                                                                              |
| PD0 to PD3         | Port D                             | I/O | The same as port C.                                                                                                                                                                                              |                                                                                                                                                              |
| PE0 to PE3         | Port E                             | I/O | The same as port C.                                                                                                                                                                                              |                                                                                                                                                              |
| PF0 to PF3         | Port F                             | I/O | The same as port C.                                                                                                                                                                                              | <br>P-ch open drain output<br>Pull-down resistance (Mask option)        |
| V <sub>FDP</sub>   | Power supply for FDP               | I   | Load current supply pin needed when load resistance is built in to output driver for FDP (Fluorescent Display Panel).                                                                                            |                                                                                                                                                              |
| T0 to T7           | Timing                             | O   | Lower 8-digit output pin of the FDP timing signal.                                                                                                                                                               |                                                                                                                                                              |
| T8/S23 to T15/S16  | Timing/segment                     | O   | Combination output pin of higher 8-digit of the FDP timing signal and the segment signal.                                                                                                                        |                                                                                                                                                              |
| PG0/S4 to PG3/S7   | Port G/segment                     | O   | Combination pin of the 4-bit output port and FDP segment signal output.                                                                                                                                          |                                                                                                                                                              |
| PH0/S0 to PH3/S3   | Port H/segment                     | O   | The same as port G.                                                                                                                                                                                              |                                                                                                                                                              |
| PJ0/S12 to PJ3/S15 | Port J/segment                     | O   | The same as port G.                                                                                                                                                                                              |                                                                                                                                                              |
| PK0/S8 to PK3/S11  | Port K/segment                     | O   | The same as port G.                                                                                                                                                                                              |                                                                                                                                                              |

**Absolute Maximum Ratings** ( $T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

| Item                                      | Symbol           | Ratings                     | Unit             | Remarks                                                                            |
|-------------------------------------------|------------------|-----------------------------|------------------|------------------------------------------------------------------------------------|
| Power supply voltage                      | $V_{DD}$         | $-0.3$ to $+7.0$            | V                |                                                                                    |
| Input voltage                             | $V_{IN}$         | $-0.3$ to $+7.0^{*1}$       | V                |                                                                                    |
| Output voltage                            | $V_{OUT}$        | $-0.3$ to $+7.0^{*1}$       | V                |                                                                                    |
| Display output voltage                    | $V_{OD}$         | $V_{DD}-40$ to $V_{DD}+0.3$ | V                | As P channel transistor is open drain, $V_{DD}$ voltage is determined as standard. |
| High level output current                 | $I_{OH}$         | $-5$                        | mA               | Other than display output pin <sup>*2</sup> : per pin                              |
|                                           | $I_{ODH1}$       | $-15$                       | mA               | Display output S0 to S15: per pin                                                  |
|                                           | $I_{ODH2}$       | $-35$                       | mA               | Display output T0 to T7, T8/S23 to T15/S16: per pin                                |
| High level total output current           | $\Sigma I_{OH}$  | $-40$                       | mA               | Total of other than display output pins                                            |
|                                           | $\Sigma I_{ODH}$ | $-100$                      | mA               | Total of display output pins                                                       |
| Low level output current                  | $I_{OL}$         | $15$                        | mA               | Port 1 pin                                                                         |
|                                           | $I_{OLC}$        | $20$                        | mA               | High current port 1 pin <sup>*3</sup>                                              |
| Low level total output current            | $\Sigma I_{OL}$  | $100$                       | mA               | Entire pin total                                                                   |
| Operating temperature                     | $T_{opr}$        | $-20$ to $+75$              | $^\circ\text{C}$ |                                                                                    |
| Storage temperature                       | $T_{stg}$        | $-55$ to $+150$             | $^\circ\text{C}$ |                                                                                    |
| Allowable power dissipation <sup>*4</sup> | $P_D$            | $600$                       | mW               |                                                                                    |

\*1)  $V_{IN}$  and  $V_{OUT}$  should not exceed  $V_{DD}+0.3\text{V}$ .

\*2) Specifies the output current of PB to PF, S0,  $\overline{SC}$  (the general purpose I/O ports) and PY0, PY1 (Output ports).

\*3) The high current drive transistors are the N channel transistors of the PC and PD ports.

\*4) Allowable power dissipation of EPROM excluded.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

**Recommended Operating Conditions** ( $V_{SS} = 0\text{ V}$ )

| Item                     | Symbol     | Min.         | Max.         | Unit             | Remarks                                      |
|--------------------------|------------|--------------|--------------|------------------|----------------------------------------------|
| Power supply voltage     | $V_{DD}$   | 4.5          | 5.5          | V                | Guaranteed range of operation by EXTAL clock |
|                          |            | 2.5          | 5.5          | V                | Guaranteed range of data hold during STOP    |
| High level input voltage | $V_{IH}$   | $0.7V_{DD}$  | $V_{DD}$     | V                |                                              |
|                          | $V_{IHS}$  | $0.8V_{DD}$  | $V_{DD}$     | V                | Hysteresis input <sup>*1</sup>               |
|                          | $V_{IHEX}$ | $V_{DD}-0.4$ | $V_{DD}+0.3$ | V                | EXTAL pin <sup>*2</sup>                      |
| Low level input voltage  | $V_{IL}$   | 0            | $0.3V_{DD}$  | V                |                                              |
|                          | $V_{ILS}$  | 0            | $0.2V_{DD}$  | V                | Hysteresis input <sup>*1</sup>               |
|                          | $V_{ILEX}$ | $-0.3$       | 0.4          | V                | EXTAL pin <sup>*2</sup>                      |
| Operating temperature    | $T_{opr}$  | $-20$        | $+75$        | $^\circ\text{C}$ |                                              |

\*1) Each of INT,  $\overline{EC}$ , PX0, PX2, PY2, PY3 and  $\overline{RST}$  pin.

\*2) Specified only during external clock input.

## Electrical Characteristics

DC characteristics (Ta = -20°C to +75°C, V<sub>SS</sub> = 0 V)

| Item                                                     | Symbol            | Pin                                                              | Condition                                                                                       | Min. | Typ. | Max. | Unit |
|----------------------------------------------------------|-------------------|------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|------|------|------|------|
| High level output voltage                                | V <sub>OH</sub>   | PB to PF, PX0, PX1<br>PY0, PY1                                   | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA                                                | 4.0  |      |      | V    |
|                                                          |                   |                                                                  | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.0mA                                                | 3.5  |      |      | V    |
| Low level output voltage                                 | V <sub>OL</sub>   | RST (V <sub>OL</sub> only)                                       | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA                                                 |      |      | 0.4  | V    |
|                                                          |                   |                                                                  | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA                                                 |      |      | 0.6  | V    |
|                                                          |                   | PC, PD                                                           | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12mA                                                  |      |      | 1.5  | V    |
| Input current                                            | I <sub>IHE</sub>  | EXTAL                                                            | V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V                                                  | 0.5  |      | 40   | μA   |
|                                                          | I <sub>IIE</sub>  |                                                                  | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V                                                  | -0.5 |      | -40  | μA   |
|                                                          | I <sub>ILR</sub>  | RST*2                                                            | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V                                                  | -1.5 |      | -400 | μA   |
| Display output current                                   | I <sub>OH</sub>   | S0 to S15                                                        |                                                                                                 | -7   |      |      | mA   |
|                                                          |                   | S16/T15 to S23/T8<br>T0 to T7                                    | V <sub>DD</sub> = 4.5V<br>V <sub>OH</sub> = V <sub>DD</sub> - 2.5V                              | -18  |      |      | mA   |
| Open drain output leakage current (P-CH Tr OFF in state) | I <sub>LOL</sub>  | S0 to S15<br>S16/T15 to S23/T8<br>T0 to T7                       | V <sub>DD</sub> = 5.5V<br>V <sub>OL</sub> = V <sub>DD</sub> - 35V                               |      |      | -20  | μA   |
| Pull-down resistance*1                                   | R <sub>L</sub>    | S0 to S15<br>S16/T15 to S23/T8<br>T0 to T7                       | V <sub>DD</sub> = 5V<br>V <sub>FDP</sub> = V <sub>DD</sub> - 35V                                | 60   | 100  | 270  | kΩ   |
| High impedance I/O leakage current                       | I <sub>IZ</sub>   | PB to PF, PX0 to PX2,<br>PY2, PY3, $\overline{EC}$<br>INT, RST*2 | V <sub>DD</sub> = 5.5V<br>V <sub>I</sub> = 0, 5.5V                                              |      |      | ±10  | μA   |
| Current supply*3                                         | I <sub>DD</sub>   | V <sub>DD</sub>                                                  | V <sub>DD</sub> = 5.5V, 4.19MHz crystal oscillation (C1 = C2 = 22pF)<br>Entire output pins open |      | 7    | 20   | mA   |
|                                                          | I <sub>DDSP</sub> |                                                                  | SLEEP mode                                                                                      |      | 5    | 12   | mA   |
|                                                          | I <sub>DDS</sub>  |                                                                  | STOP mode                                                                                       |      |      | 10   | μA   |
| Input capacity                                           | C <sub>IN</sub>   | PB to PF, PX<br>PY2, PY3,<br>EXTAL,<br>RST, INT, $\overline{EC}$ | f <sub>c</sub> = 1MHz<br>0V other than the measured pins                                        |      | 10   | 20   | pF   |

\*1) In case the incorporated pull-down resistance has been selected with mask option.

\*2) RST pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when nonresistance is selected.

\*3) Current supply of EPROM excluded.

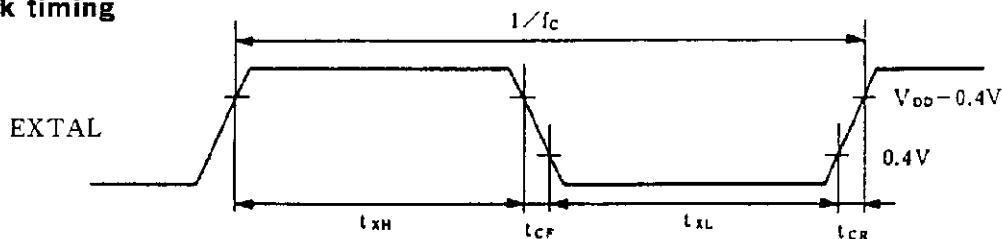
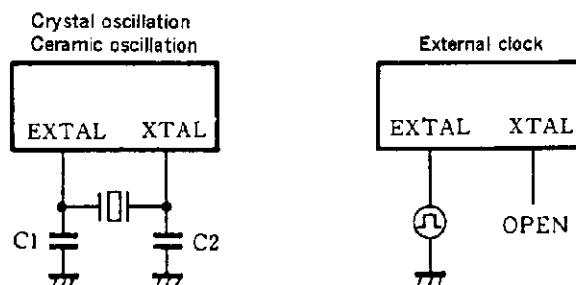
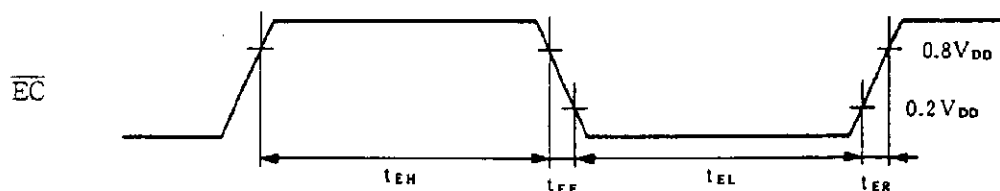
**AC characteristics**(1) Clock timing ( $T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Item                                             | Symbol               | Pin             | Condition                              | Min.                      | Typ. | Max. | Unit          |
|--------------------------------------------------|----------------------|-----------------|----------------------------------------|---------------------------|------|------|---------------|
| System clock frequency                           | $f_c$                | XTAL<br>EXTAL   | Fig. 1, Fig. 2                         | 1                         |      | 5    | MHz           |
| System clock input pulse width                   | $t_{XL}$<br>$t_{XH}$ | EXTAL           | Fig. 1, Fig. 2<br>External clock drive | 90                        |      |      | ns            |
| System clock input rising and falling times      | $t_{CR}$<br>$t_{CF}$ | EXTAL           | Fig.1, Fig.2<br>External clock drive   |                           |      | 200  | ns            |
| Event count clock input pulse width              | $t_{EL}$<br>$t_{EH}$ | $\overline{EC}$ | Fig. 3                                 | $t_{sys}^{*1}$<br>$+0.05$ |      |      | $\mu\text{s}$ |
| Event count clock input rising and falling times | $t_{ER}$<br>$t_{EF}$ | $\overline{EC}$ | Fig. 3                                 |                           |      | 20   | ms            |

\*1)  $t_{sys}$  is  $t_{sys} = 8/f_c$ 

\*2) Specified when the crystal oscillation mode is selected by the mask option.

Note) When adjusting the frequency accurately, there may be cases in which they may differ from Fig. 2.

**Fig. 1 Clock timing****Fig. 2 Clock applying condition****Fig. 3 Event count clock timing**



(2) Serial transfer ( $T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

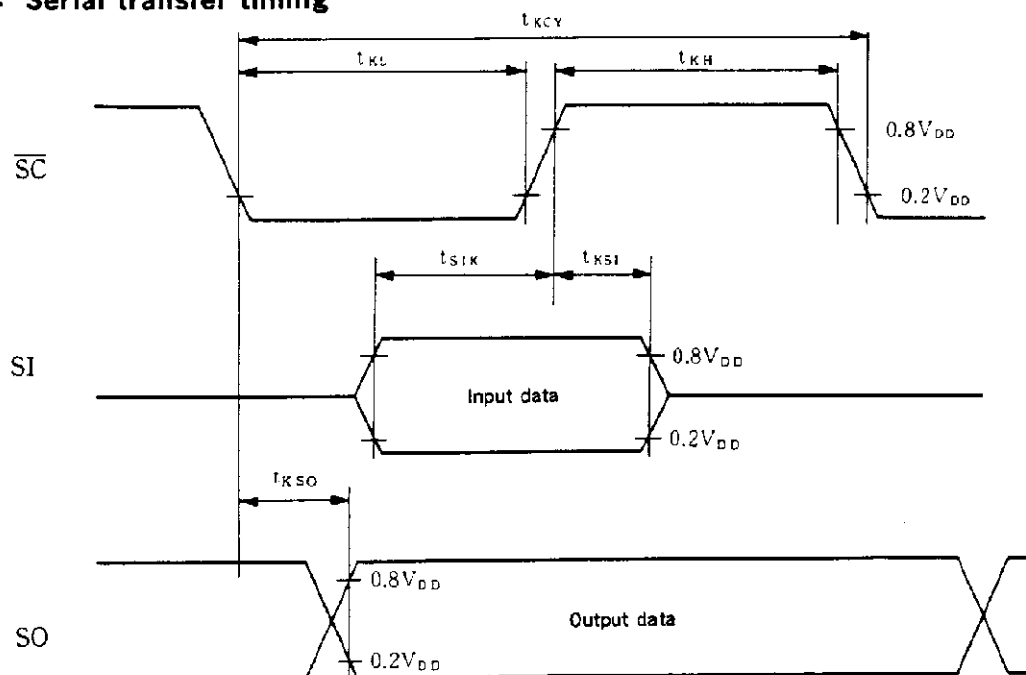
| Item                                                                       | Symbol                             | Pin                    | Condition                          | Min.                      | Max.                     | Unit          |
|----------------------------------------------------------------------------|------------------------------------|------------------------|------------------------------------|---------------------------|--------------------------|---------------|
| Serial transfer clock ( $\overline{\text{SC}}$ ) cycle time                | $t_{\text{KCY}}$                   | $\overline{\text{SC}}$ | Input mode                         | $t_{\text{sys}}/4 + 1.42$ |                          | $\mu\text{s}$ |
|                                                                            |                                    |                        | Output mode                        | $t_{\text{SIO}}$          |                          | $\mu\text{s}$ |
| Serial transfer clock ( $\overline{\text{SC}}$ ) high and low level widths | $t_{\text{KH}}$<br>$t_{\text{KL}}$ | $\overline{\text{SC}}$ | Input mode                         | $t_{\text{sys}}/8 + 0.7$  |                          | $\mu\text{s}$ |
|                                                                            |                                    |                        | Output mode                        | $t_{\text{SIO}}/2 - 0.1$  |                          | $\mu\text{s}$ |
| Serial data input setup time (against $\overline{\text{SC}} \uparrow$ )    | $t_{\text{SIK}}$                   | SI                     | $\overline{\text{SC}}$ input mode  | 0.1                       |                          | $\mu\text{s}$ |
|                                                                            |                                    |                        | $\overline{\text{SC}}$ output mode | 0.2                       |                          | $\mu\text{s}$ |
| Serial data input hold time (against $\overline{\text{SC}} \uparrow$ )     | $t_{\text{KSI}}$                   | SI                     | $\overline{\text{SC}}$ input mode  | $t_{\text{sys}}/8 + 0.5$  |                          | $\mu\text{s}$ |
|                                                                            |                                    |                        | $\overline{\text{SC}}$ output mode | 0.1                       |                          | $\mu\text{s}$ |
| Data output delay time from $\overline{\text{SC}}$ falling                 | $t_{\text{KSO}}$                   | SO                     |                                    |                           | $t_{\text{sys}}/8 + 0.5$ | $\mu\text{s}$ |

Note 1)  $t_{\text{sys}}$  is  $t_{\text{sys}} = 8/f_c$

$t_{\text{SIO}}$  is turned into either  $2t_{\text{sys}}$ ,  $4t_{\text{sys}}$  or  $16t_{\text{sys}}$  by means of a program.

2) The load of data output delay time is  $50\text{ pF} + 1\text{ TTL}$ .

Fig. 4 Serial transfer timing



(3) A/D converter ( $T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

| Analog input voltage | Pin | Condition             | Digital conversion value |
|----------------------|-----|-----------------------|--------------------------|
| 0.0 to 0.33V         | ADI | $V_{DD} = 5\text{ V}$ | 000                      |
| 0.82 to 1.29V        |     |                       | 001                      |
| 1.78 to 2.21V        |     |                       | 010                      |
| 2.69 to 3.06V        |     |                       | 011                      |
| 3.56 to 4.06V        |     |                       | 100                      |
| 4.62 to 5.0V         |     |                       | 101                      |

Note) The digital conversion values are the values when  $\text{FF}_H$  address in the program are read.

(4) Others ( $T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Item                                            | Symbol                | Pin | Condition           | Min.             | Max. | Unit          |
|-------------------------------------------------|-----------------------|-----|---------------------|------------------|------|---------------|
| External interruption high and low level widths | $t_{I1H}$ , $t_{I1L}$ | INT | Edge detection mode | $t_{sys} + 0.05$ |      | $\mu\text{s}$ |
| Reset input low level width                     | $t_{RSL}$             | RST |                     | $2t_{sys}$       |      | $\mu\text{s}$ |
| Wake-up input high level width                  | $t_{WPH}$             | WP  | STOP mode           | 500              |      | $\mu\text{s}$ |
|                                                 |                       |     | SLEEP mode          | $t_{sys} + 0.05$ |      | $\mu\text{s}$ |

Note)  $t_{sys}$  is  $t_{sys} = 8/f_c$

Fig. 5 Interruption input timing

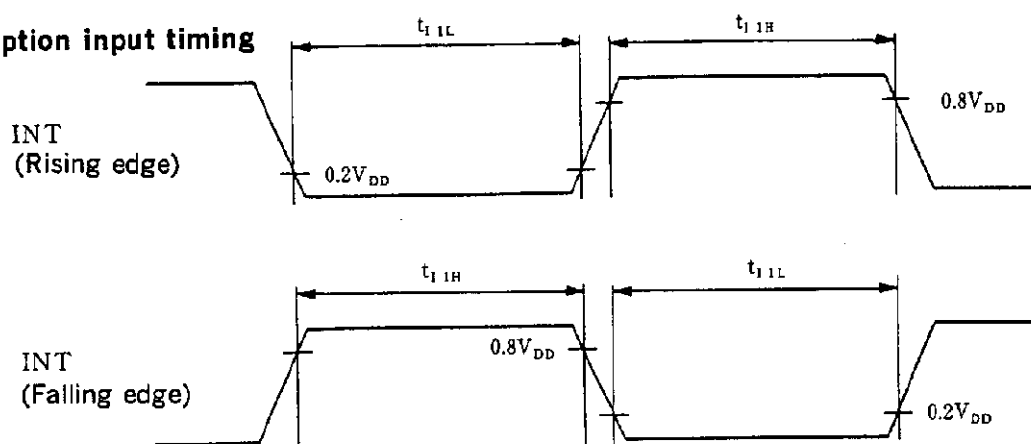


Fig. 6 RST input timing

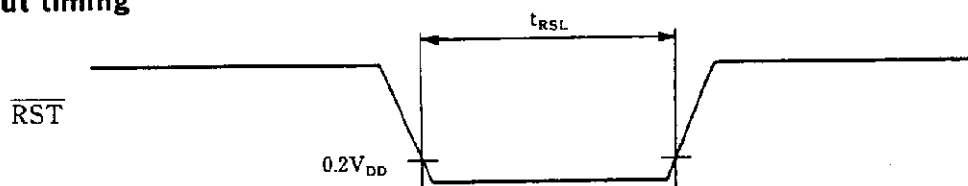


Fig. 7 Wake-up input timing

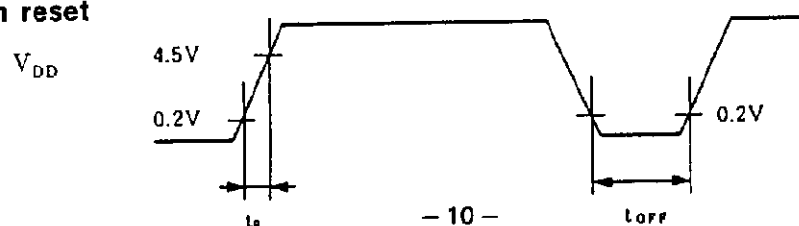


Power on reset\* ( $T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

| Item                      | Symbol    | Pin      | Condition                 | Min. | Max. | Unit |
|---------------------------|-----------|----------|---------------------------|------|------|------|
| Power supply rising time  | $t_R$     | $V_{DD}$ | Power on reset            | 0.05 | 50   | ms   |
| Power supply cut-off time | $t_{OFF}$ |          | Repetitive power on reset | 1    |      | ms   |

\* Specifies only when power on reset function is selected.

Fig. 8 Power on reset

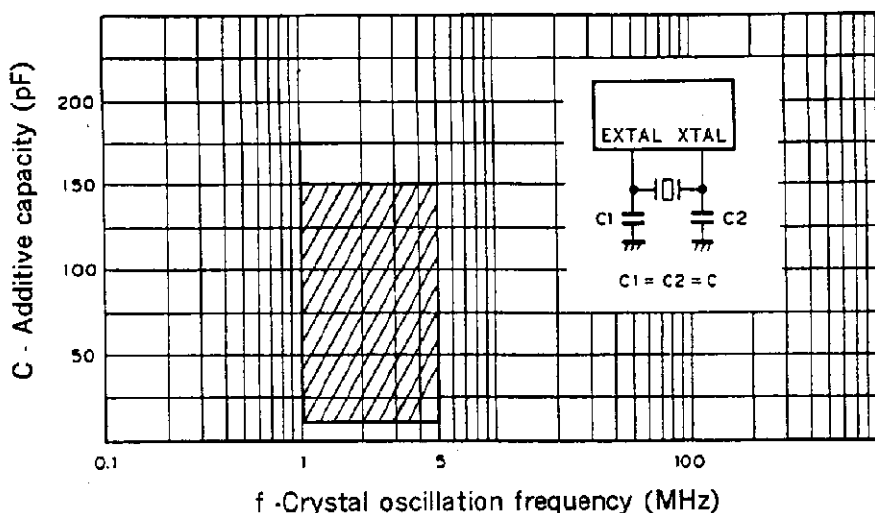


The power supply should rise smoothly.

## Notes on Operation

See Fig. 9, additive capacity calculation chart, when using the crystal oscillator and select the appropriate capacity.

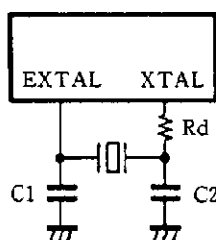
**Fig. 9 Crystal oscillation circuit additive capacity calculation chart**  
( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5$  V)



Note) The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

Fig. 10 shows recommended circuits and oscillators. Use the trimmer capacitor to C1, in the case of accurate adjustment of the oscillation frequency.

**Fig. 10 Recommended oscillation circuit**

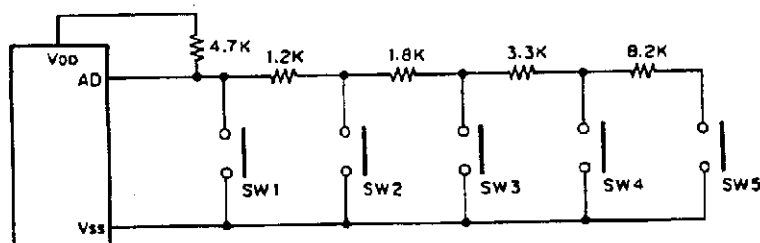


| Manufacturer         | Model         | Frequency | C1              | C2              | Rd |
|----------------------|---------------|-----------|-----------------|-----------------|----|
| MURATA MFG CO., LTD. | CSA4.19MG040  | 4.19 MHz  | 100pF           | 100pF           | —  |
|                      | CST4.19MGW040 | 4.19 MHz  | —<br>(built in) | —<br>(built in) | —  |

| Manufacturer                | Model     | Frequency | C1                     | C2   | Rd    |
|-----------------------------|-----------|-----------|------------------------|------|-------|
| CITIZEN WATCH CO., LTD.     | CSA-309   | 4.19 MHz  | 10pF<br>(20pF trimmer) | 10pF | —     |
| NIHON DENPA KOGYO CO., LTD. | AT-51     | 4.19 MHz  | 15pF<br>(20pF trimmer) | 15pF | 6.8kΩ |
| KINSEKI LTD.                | HC-49/U-S | 4.19 MHz  | 22pF                   | 22pF | 3.3kΩ |

When using the A/D converter as the key input, it is recommended that the circuit structure shown in Fig. 11 be used.

Fig. 11 Recommended example of key circuit by A/D converter



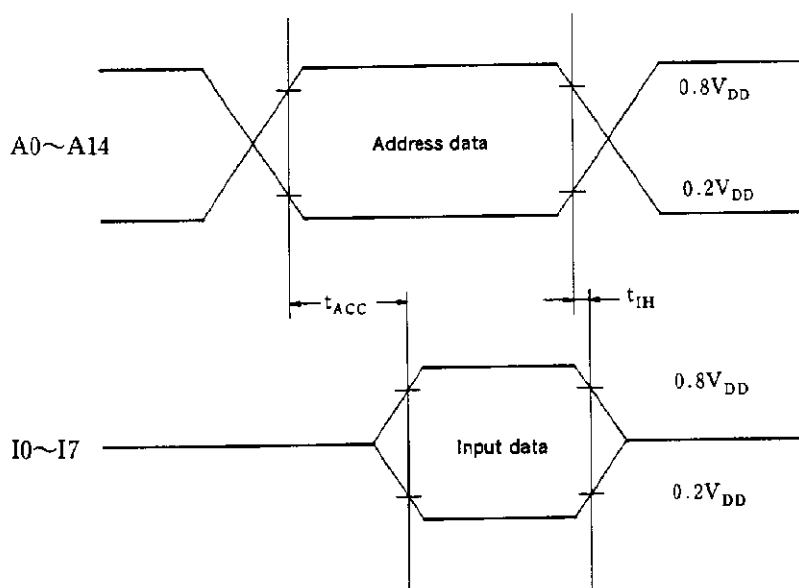
(Precision of resistance is all within  $\pm 5\%$ )

### EPROM Read Timing

$T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$

| Item                                           | Symbol    | Pin                   | Min. | Max. | Unit |
|------------------------------------------------|-----------|-----------------------|------|------|------|
| Address $\rightarrow$ Data<br>input delay time | $t_{ACC}$ | A0 to A14<br>I0 to I7 |      | 300  | ns   |
| Address $\rightarrow$ Data<br>hold time        | $t_{IH}$  | A0 to A14<br>I0 to I7 | 0    |      | ns   |

### EPROM Timing



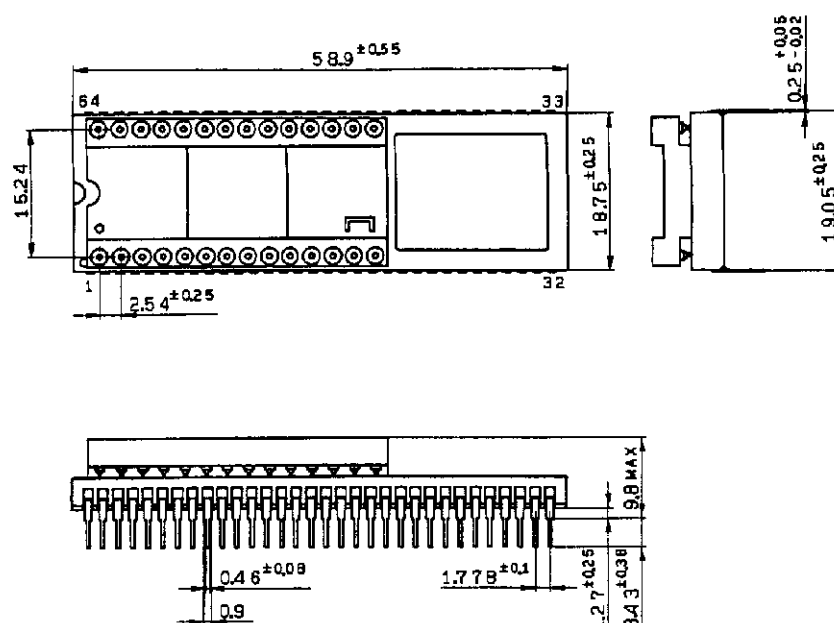
### List of Products

| Option item                       | Product             | CXP50200-U01Q       |
|-----------------------------------|---------------------|---------------------|
| Package                           | 64-pin plastic SDIP | 64-pin ceramic SDIP |
| ROM capacity                      | 12k bytes/16k bytes | EPROM 32k bytes     |
| Pull-up resistance of reset pin   | Mask/Non-mask       | Mask                |
| Power on reset circuit            | Mask/Non-mask       | Mask                |
| 32kHz timer/counter               | Timer/counter       | Timer mode          |
| High tension pull-down resistance | Mask/Non-mask       | Non-mask            |

Note) Chip for both piggy and evaluation.

## Package Outline Unit: mm

## 64pin SDIP (Ceramic)



PSDIP-64C-01