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ADVANCED PWM DC-DC CONVERTER WITH INTERNAL SWITCH AND SOFT-START

FEATURES

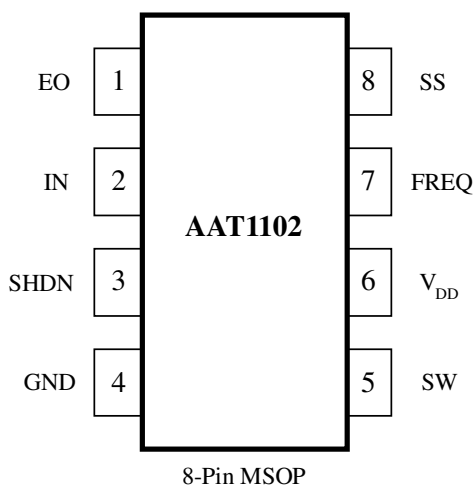
- 1.6A, 0.23Ω, Internal Switch
- High Efficiency: 90%
- Adjustable Output: V_{DD} to 12.5V
- Adjustable Frequency: 640kHz or 1.3MHz
- Wide Input Range: +2.6V to +5.5V
- Low Shutdown Current: 0.1μA
- Programmable Soft-Start
- Small 8-Pin MSOP Package

GENERAL DESCRIPTION

The AAT1102 is a step-up DC-DC converter with a 1.6A, 0.23Ω internal switch. Equipped with an external compensation pin, this device offers user flexibility in determining loop dynamic and adjusting operating frequency. AAT1102 also allows the use of small, low equivalent resistance (ESR) ceramic output capacitor, and it's capable of converting a standard input of 3.3V to multiple outputs of 8V, -8V, and 23V. Furthermore, filtering and loop performance are facilitated and enhanced by a high switching frequency of either 640 kHz or 1.3MHz.

PIN CONFIGURATION

TOP VIEW



The AAT1102's versatility comes with a power-smart design. A soft-start programmed with an external capacitor that sets the input current ramp rate, reduces the current consumption to 0.1μA in shutdown mode. When operating, a mere 2.6V input yields an impressive output voltage as high as 12.5V.

High switching frequency and economical design allow AAT1102 to be less than 1.1mm high. Its compact 8-pin MSOP package and superior performance make it an ideal part for biasing TFT displays.



PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	EO	Compensation Pin for Error Amplifier
2	IN	Feedback Pin with a Typical Reference Voltage of 1.24V, $V_{OUT} = IN(1 + \frac{R1}{R2})$
3	SHDN	Shutdown Control Pin. The Device Will Turn Off When SHDN is Low
4	GND	Ground
5	SW	Switch Pin
6	V _{DD}	Power Supply Pin
7	FREQ	Frequency Select Pin. Switch Oscillator Frequency to 640kHz When FREQ is Low, and 1.3MHz When FREQ is High
8	SS	Soft-Start Control Pin. No Soft-Start When the Pin is Left Open

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
SW to GND		-0.3 to +18	V
IN, SHDN, V _{DD} , FREQ to GND		-0.3 to +6	V
SS, EO to GND		-0.3 V to (V _{DD} + 0.3V)	V
RMS SW Pin Current	I _{SW}	1.2	A
Continuous Power Dissipation (T _C = +70 °C) 8-Pin MSOP (De-Rate 4.1 mW / °C above +70 °C)	P _d	330	mW
Operation Temperature Range	T _C	-20 to +85	°C
Storage Temperature Range	T _{storage}	-45 to +125	°C
Lead Temperature (Soldering for 10 seconds)	T _L	+300	°C

Note:

1. Absolute Maximum Ratings are threshold limit values that must not be exceeded.
2. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device.
3. These are stress ratings only and do not necessarily imply functional operation below these limits.



ELECTRICAL CHARACTERISTICS

$V_{DD} = \overline{\text{SHDN}} = 3\text{V}$, $\text{FREQ} = \text{GND}$, unless otherwise specified. Typical values are at $T_c = +25^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage Range	V_{DD}		2.6		5.5	V
V_{DD} Under Voltage Lockout	UVLO	When V_{DD} is rising, typical hysteresis is 40mV; SW remains off below this level	2.25	2.38	2.52	V
Quiescent Current	I_{DD}	$V_{IN} = 1.3\text{V}$, not switching		0.21	0.35	mA
		$V_{IN} = 1.0\text{V}$, switching		1.2	5.0	
Shutdown Current	I_{SC}	$\overline{\text{SHDN}} = \text{GND}$		0.1	10.0	μA

ERROR AMPLIFIER

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Feedback Voltage	V_{IN}	Level to produce $V_{EO} = 1.24\text{V}$	1.222	1.240	1.258	V
V_{DD} Input Bias Current	I_{IN}	$V_{IN} = 1.24\text{V}$		0	40	nA
Feedback-Voltage Line Regulation		Level to produce $V_{EO} = 1.24\text{V}$, $2.6\text{V} < V_{DD} < 5.5\text{V}$		0.05	0.15	$\%/V$
Transconductance	g_m	$\Delta I = 5 \mu\text{A}$	70	105	240	$\mu\text{A} /V$
Voltage Gain	A_V			1,500		V/V

OSCILLATOR

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	f_{OSC}	FREQ = GND	540	640	740	kHz
		FREQ = V_{DD}	1,100	1,320	1,600	
Maximum Duty Cycle	D_{MAX}	FREQ = GND	79	85	92	%
		FREQ = V_{DD}		85		

**ELECTRICAL CHARACTERISTICS**

$V_{DD} = \overline{\text{SHDN}} = 3\text{V}$, $\text{FREQ} = \text{GND}$, unless otherwise specified. Typical values are at $T_C = +25^\circ\text{C}$)

N-CHANNEL SWITCH

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit	I_{LIM}	$V_{DD} = 1\text{V}$, Duty Cycle = 65%	1.2	1.6	2.3	A
On-Resistance	R_{ON}	$I_{SW} = 1.2\text{A}$		0.23	0.50	Ω
Leakage Current	I_{SWOFF}	$V_{SW} = 12\text{V}$		0.01	20.00	μA

SOFT-START

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Switch Resistance					300	Ω
Charge Current		$V_{SS} = 1.2\text{V}$	1.5	4.0	7.0	μA

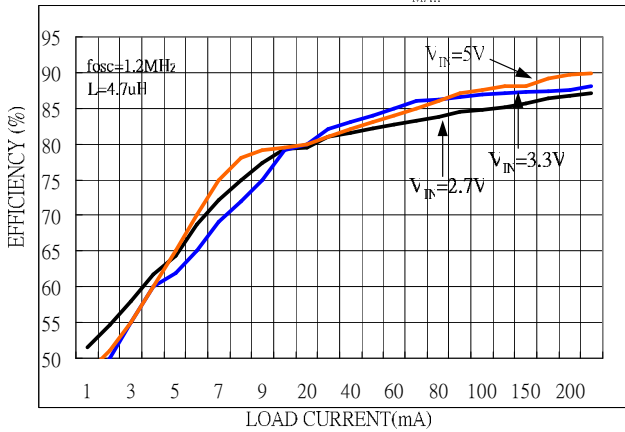
CONTROL INPUTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	SHDN, FREQ; $V_{DD} = 2.6\text{V}$ to 5.5V			$0.3 \cdot V_{DD}$	V
Input High Voltage	V_{IH}	SHDN, FREQ; $V_{DD} = 2.6\text{V}$ to 5.5V	$0.7 \cdot V_{DD}$			V
Hysteresis		SHDN, FREQ		$0.1 \cdot V_{DD}$		V
FREQ Pull-Down Current	I_{FREQ}		1.8	5.0	9.0	μA
SHDN Input Current	$I_{\overline{\text{SHDN}}}$			0.001	1.000	μA

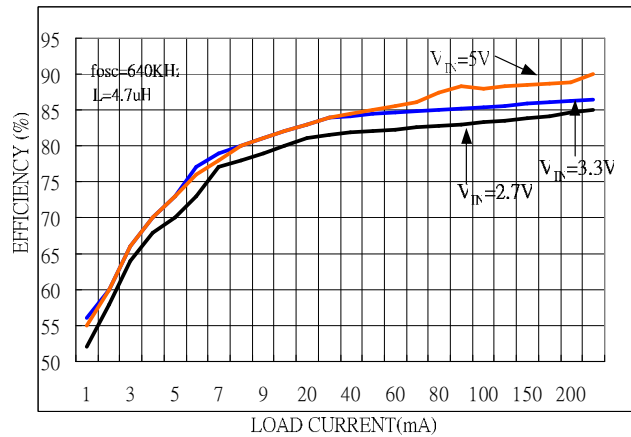


Typical Operating Characteristics

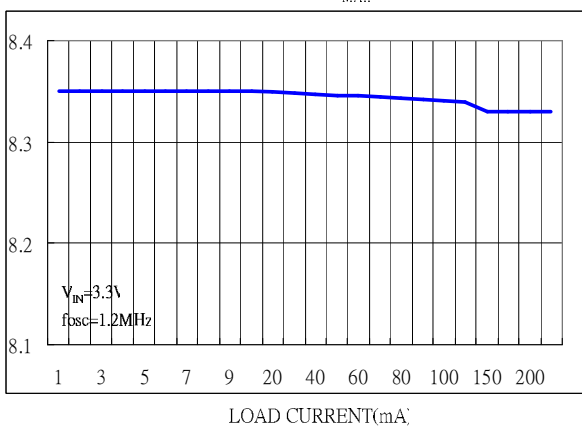
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT ($V_{MAIN}=8.3V$)



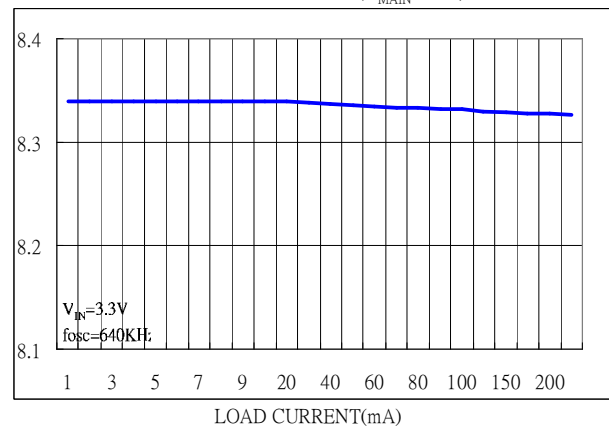
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT ($V_{MAIN}=8.3V$)



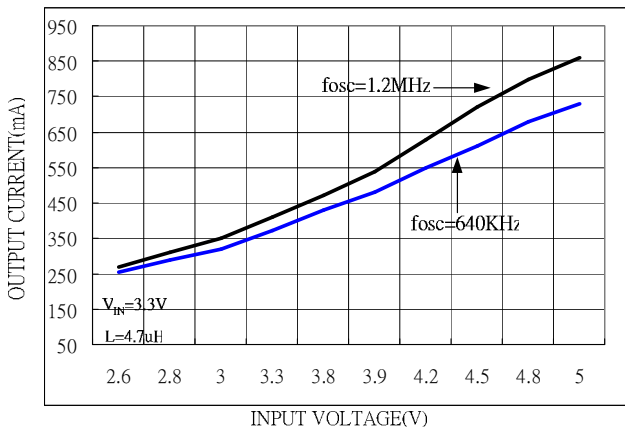
STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{MAIN}=8.3V$)



STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{MAIN}=8.3V$)



MAXIMUM LOAD CURRENT ($V_{MAIN}=8.3V$) vs. INPUT VOLTAGE



MAXIMUM INDUCTOR CURRENT ($V_{MAIN}=8.3V$) vs. INPUT VOLTAGE

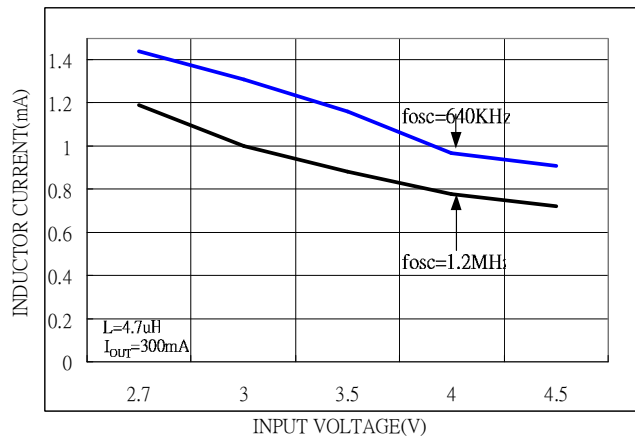




Fig. 1 TYPICAL APPLICATION CIRCUIT

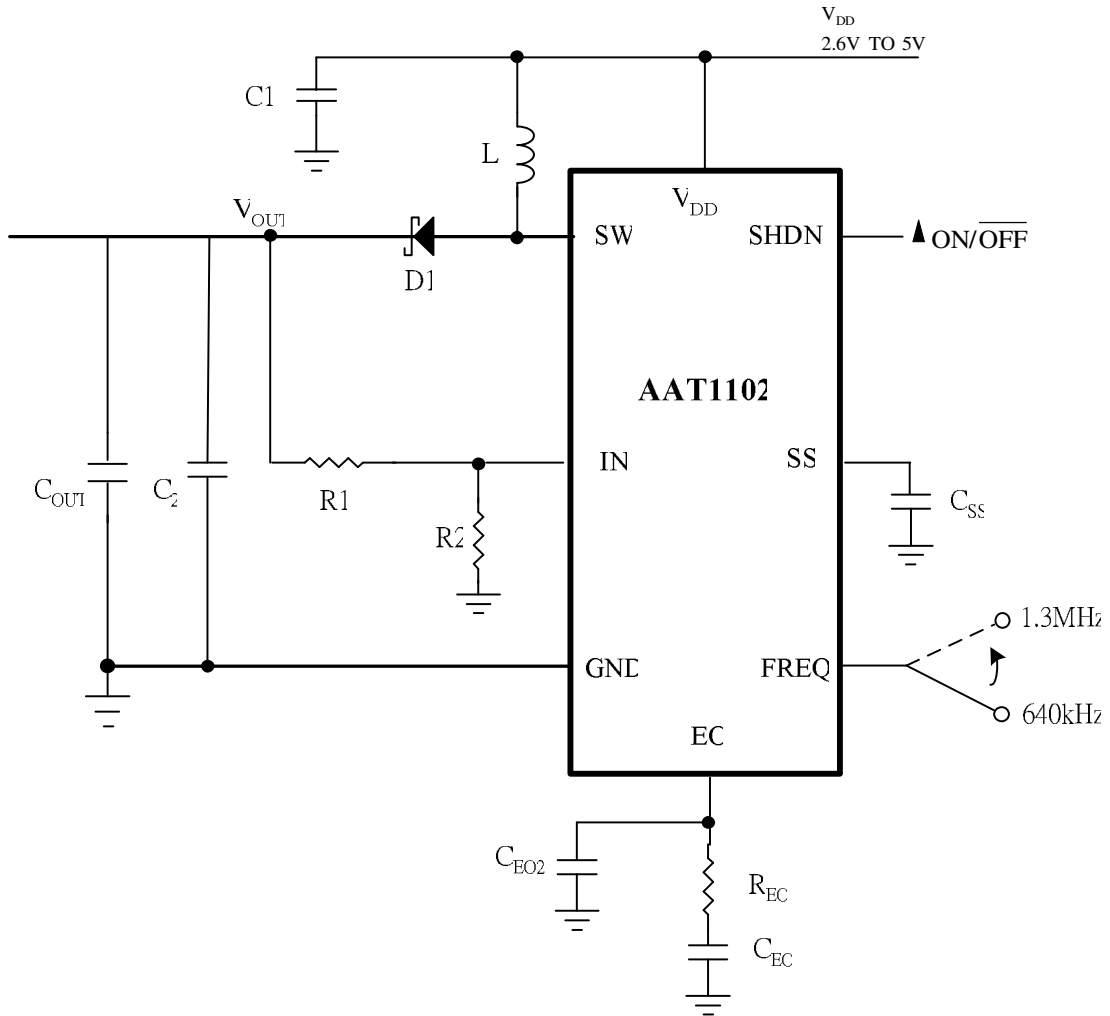




Fig. 2 BLOCK DIAGRAM

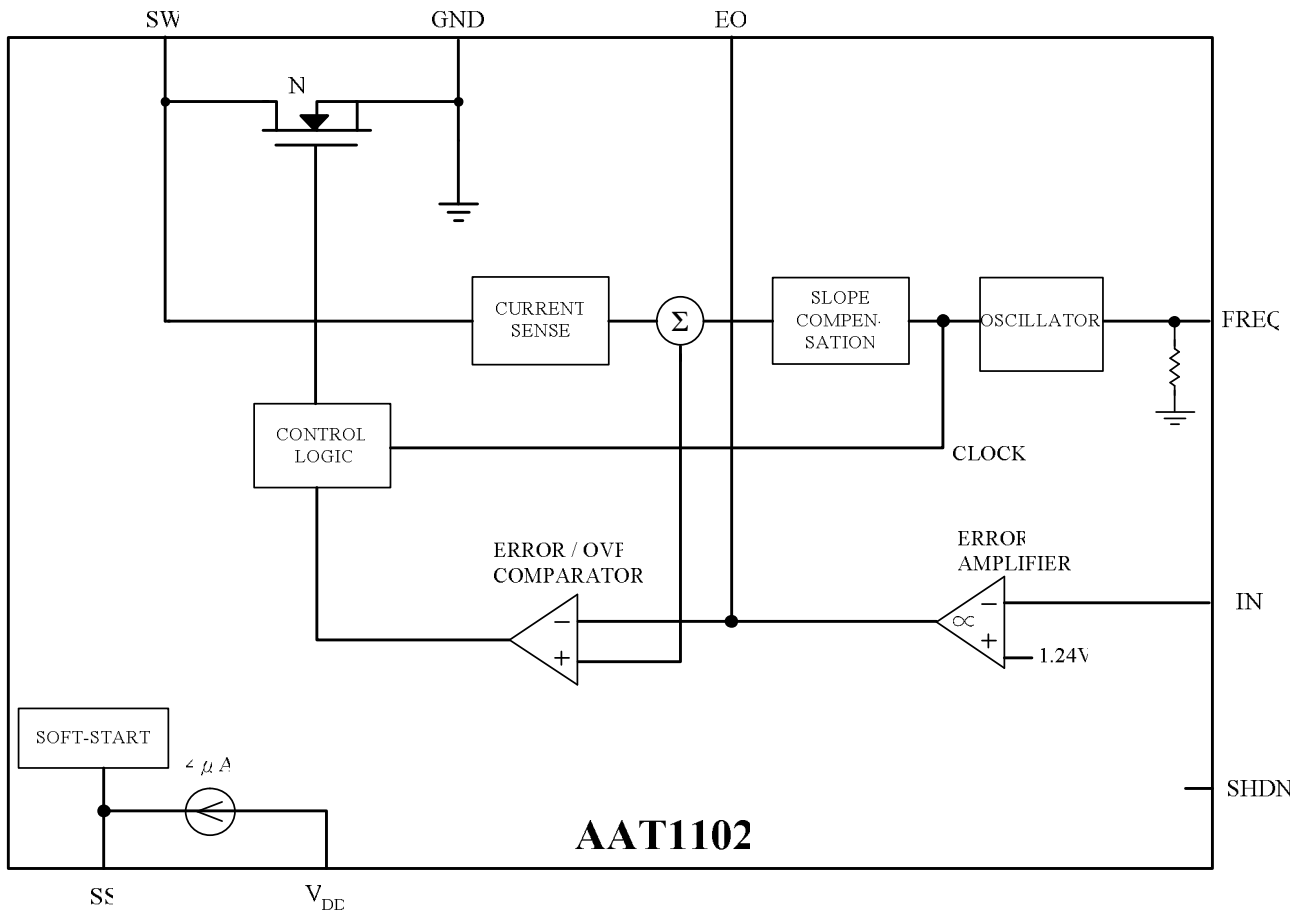




Fig. 3 AAT1102 IN A SEPIC CONFIGURATION

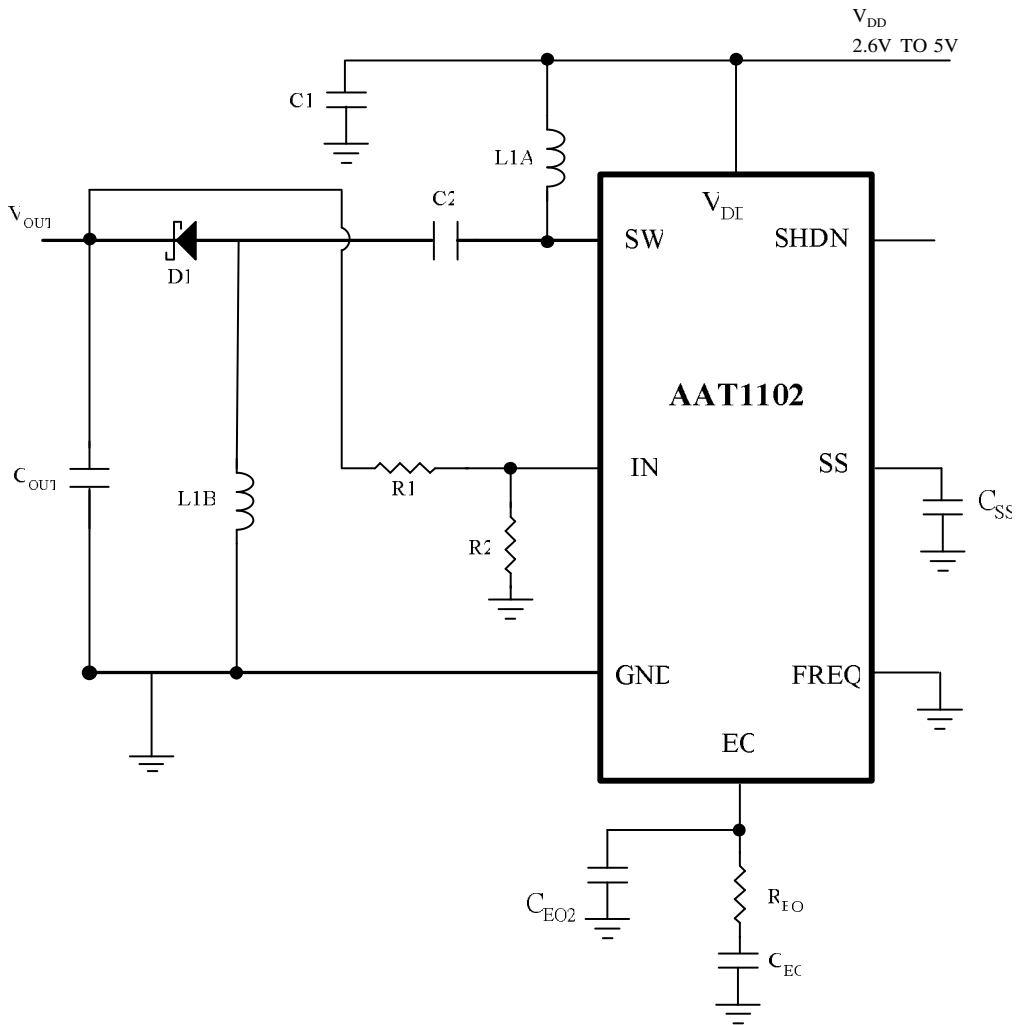
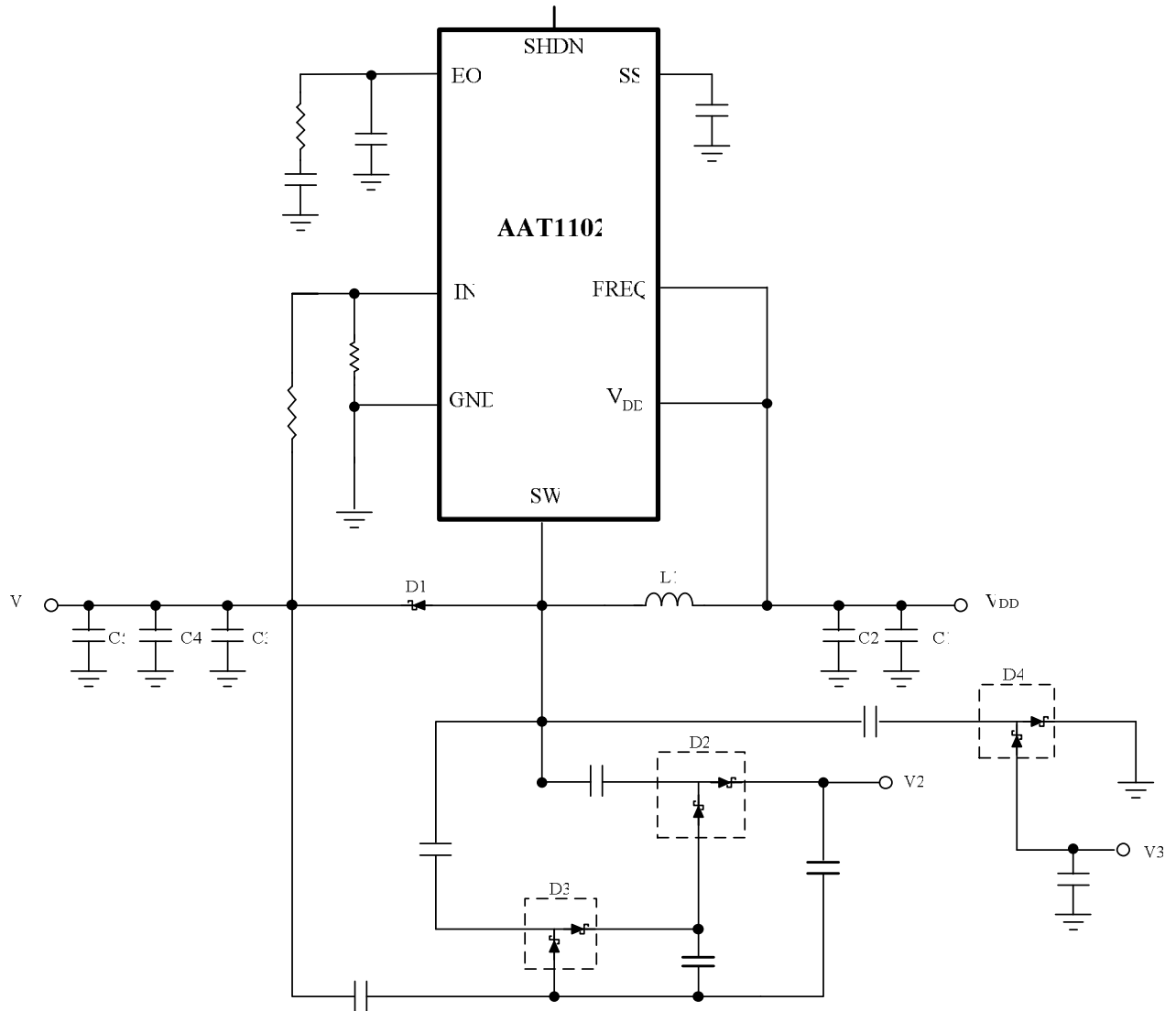




Fig. 4 MULTIPLE-OUTPUT TFT LCD POWER SUPPLY





Inductor selection

$$I_{L(peak)} = I_{IN} + \frac{V_{IN}D}{2Lf_s}, \text{ where } D \text{ is duty cycle}$$

$$\text{And } I_{IN} = \frac{I_o}{1-D}, D = 1 - \frac{V_{IN}}{V_o}$$

The inductor current rating must be greater than $I_{L(peak)}$.

Loop Compensation Design

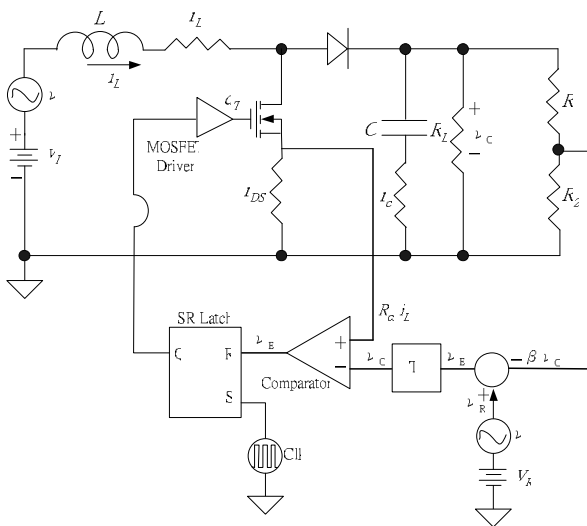


Fig.1. Closed-current loop for boost with PCM

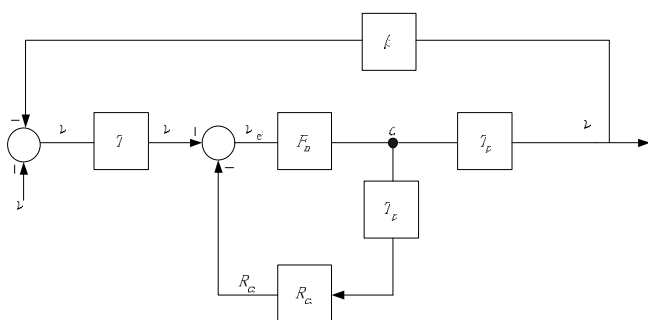


Fig.2. Block diagram of boost converter with PCM

Power Stage Transfer Functions

The duty to output voltage transfer function T_p is:

$$T_p(s) = \frac{v_o}{d} = T_{p0} \frac{(s + w_{esr})(s - w_{z2})}{s^2 + 2\zeta w_n s + w_n^2}$$

$$\text{Where } T_{p0} = V_o \frac{-r_c}{(1-D)(R_L + r_c)}, w_{esr} = \frac{1}{Cr_c}$$

And

$$w_{z2} = \frac{R_L(1-D)^2 - r}{L}, w_n = \sqrt{\frac{(1-D)^2 R_L + r}{LC(R_L + r_c)}}$$

$$\zeta = \frac{C[r(R_L + r_c) + R_L r_c(1-D)^2] + L}{2\sqrt{LC(R_L + r_c)[r + (1-D)^2 R_L]}}$$

$$r = r_L + Dr_{DS} + (1-D)R_F$$

r_L is the inductor equivalent series resistance, r_c is capacitor ESR, R_L is the converter load resistance, C is output filter capacitor, r_{DS} is the transistor on-resistance, and R_F is the diode forward resistance.

The duty to inductor current transfer function T_{pi} is:

$$T_{pi}(s) = \frac{i_l}{d} = T_{pi0} \frac{s + w_{zi}}{s^2 + 2\zeta w_n s + w_n^2}$$

$$\text{Where } T_{pi0} = \frac{V_o(R_L + 2r_c)}{L(R_L + r_c)}, w_{zi} = \frac{1}{C(R_L/2 + r_c)}$$



Current Sampling Transfer Function

Error voltage to duty transfer function F_m is:

$$F_m(s) = \frac{d}{v_{ei}} = \frac{2f_s^2(s^2 + 2\xi w_n s + w_n^2)}{T_{pi0} R_{cs} s(s + w_{zi})(s + w_{sh})}$$

Where $w_{sh} = \frac{3w_s}{\pi} \left(\frac{1-\alpha}{1+\alpha} \right)$, $\alpha = \frac{M_2 - M_a}{M_1 + M_a}$,

$$w_s = 2\pi \cdot f_s$$

Therefore, F_m depends on duty to inductor current transfer function T_{pi} , and f_s is the clock switching frequency; R_{cs} is the current-sense amplifier

transresistance. For the boost converter $M_1 = V_{IN}/L$ and $M_2 = (V_O - V_{IN})/L$

For AAT1102, $R_{cs} = 0.275 \text{ V/A}$, M_a is slope compensation, $M_a = 0.8 \times 10^6$.

The closed-current loop transfer function T_{icl} is:

$$T_{icl}(s) = \frac{12f_s^2}{R_{cs} T_{pi0}} \times \frac{(s^2 + 2\xi w_n s + w_n^2)}{(s + w_{zi})(s^2 + w_{sh} s + 12f_s^2)}$$

The Voltage-Loop Gain With Current Loop Closed

The control to output voltage transfer function T_d is:

$$T_d(s) = \frac{v_o(s)}{v_c(s)} = T_{icl}(s) T_p(s)$$

The voltage-loop gain with current loop closed is:

$$L_{vi}(s) = \beta T_c(s) T_d(s)$$

$$= \beta g_m R_c \frac{s + w_c}{s} \frac{12f_s^2 T_{p0}}{R_{cs} T_{pi0}} \times \frac{(s + w_{z1})(s - w_{z2})}{(s + w_{zi})(s^2 + sw_{sh} + 12f_s^2)}$$

Where $\beta = \frac{V_{FB}}{V_O}$,

The compensator transfer function

$$T_c(s) = \frac{v_c}{v_{fb}} = g_m R_c \frac{s + w_c}{s}, \text{ where } w_c = \frac{1}{R_c C_c}$$

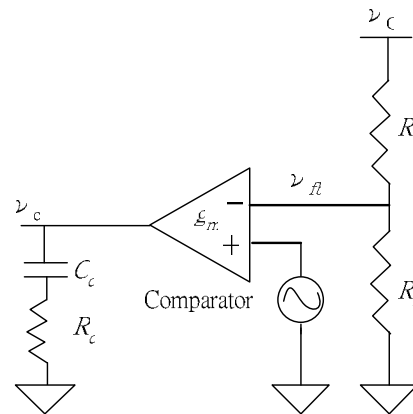


Fig.3. Voltage loop compensator

Compensator design guide:

1. Crossover frequency $f_{ci} < \frac{1}{2} f_s$
2. Gain margin > 10dB
3. Phase margin > 40°
4. The $|L_{vi}(s)| = 1$ at crossover frequency, Therefore, the compensator resistance, R_c is determined by:



$$R_c = \frac{V_o}{V_{FB}} \frac{2\pi f_{ci} C R_{cs}}{k g_m} \frac{(R_L + 2r_c)}{\left[(1-D)R_L - \frac{r}{(1-D)} \right]}$$

V_{FB} is equal to reference voltage, V_{REF} .
 $V_{REF}=1.24V$, k is the correct factor, and
 $k = (6-8)$

5. The output filter capacitor is chosen so C .
 R_L pole cancels $R_c \cdot C_c$ zero

$$R_c C_c = \frac{C}{(1-3)} \left(\frac{R_L}{2} + r_c \right), \text{ and}$$

$$C_c = \frac{C}{(1-3)R_c} \left(\frac{R_L}{2} + r_c \right)$$

Example:

$V_{IN}=5V$, $V_o=9.6V$, $I_o=250mA$, $f_s=600\text{ kHz}$,
 $V_{FB}=1.25V$, $L = 6.8\mu H$, $g_m = 105\mu S$, $R_{cs} = 0.275$
 V/A , $r_L = 0.1\Omega$, $r_{DS} = 0.23\Omega$, $r_c = 50m\Omega$, $k=7$
 $R_F = 1.4\Omega$, $f_{ci} = 21.4\text{ kHz}$, $C_c = 1.3nF$, $R_c = 27k$
 Ω , $C = 4.7\mu F$

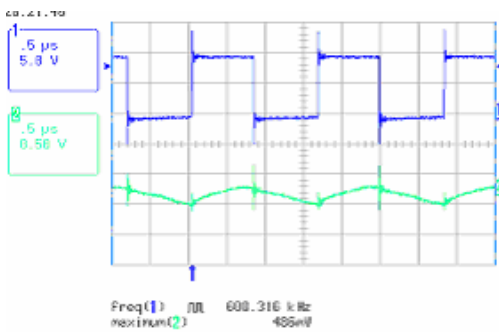


Fig.4. CH1: PWM waveform, CH2, v_{p-p} for V_o

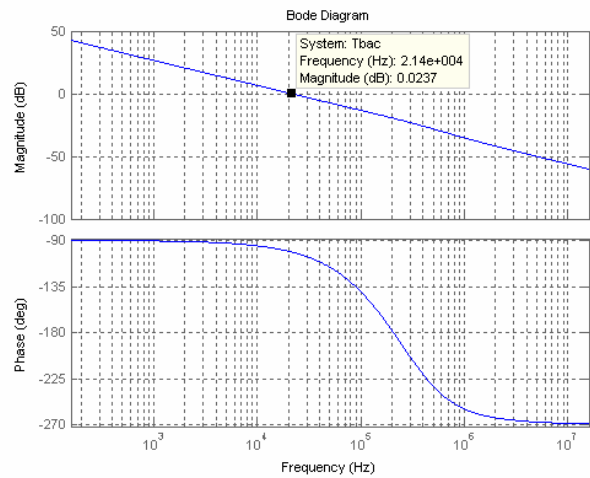
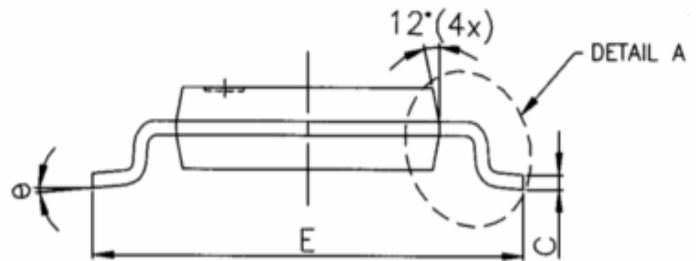
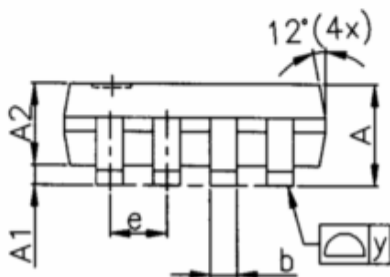
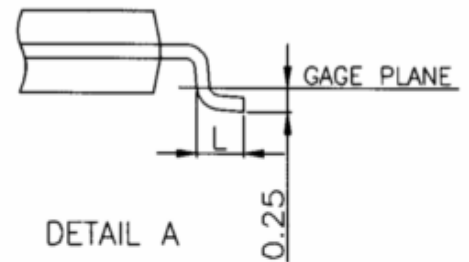
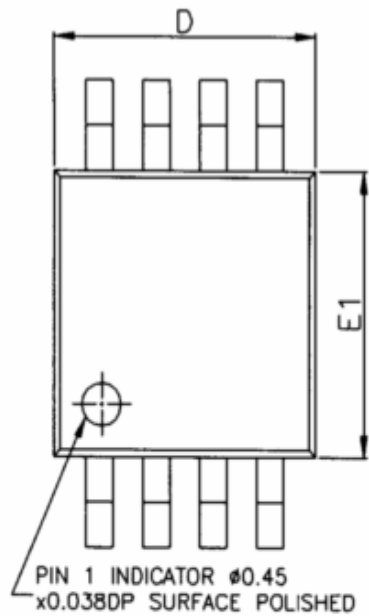


Fig.5. Bode diagram using Matlab simulation



**PACKAGE DIMENSION
MSOP-8**





PACKAGE DIMENSION (CONT.)
MSOP-8

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.81	1.02	1.22	0.032	0.040	0.043
△ A1	0.05	—	0.15	0.002	—	0.006
A2	0.76	0.86	0.97	0.030	0.034	0.038
b	0.28	0.30	0.38	0.011	0.012	0.015
c	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	—	0.65	—	—	0.0256	—
L	0.40	0.53	0.66	0.016	0.021	0.026
y	—	—	0.076	—	—	0.003
Ø	0'	3'	6'	0'	3'	6'

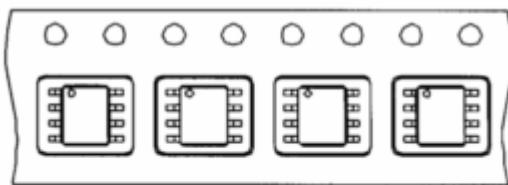
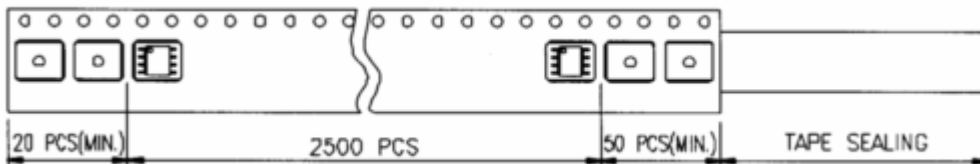
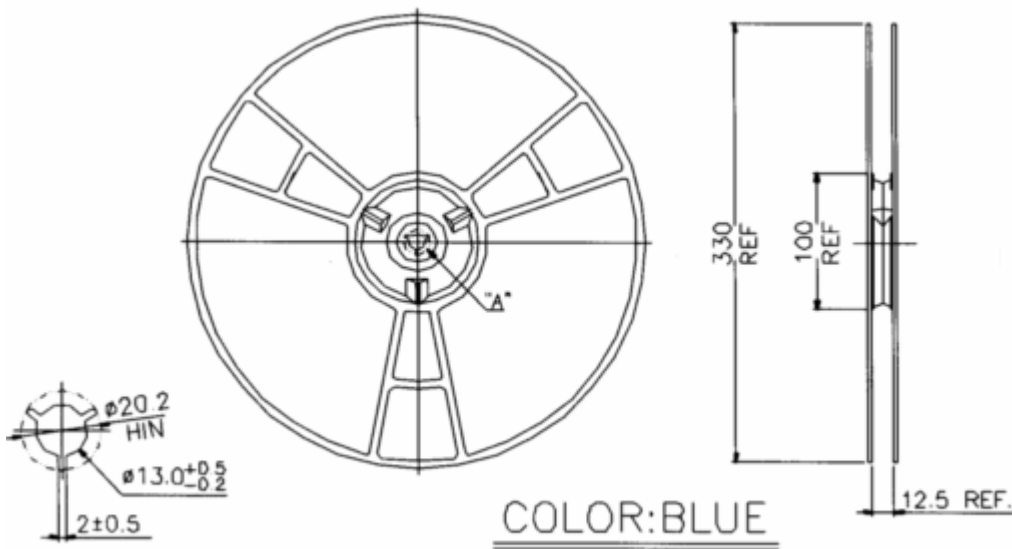
NOTE :

1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : OLIN C7025
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCEED OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm].
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.



TAPE AND REEL

PACKING METHOD: 2,500PCS/REEL, 1 REEL/BOX



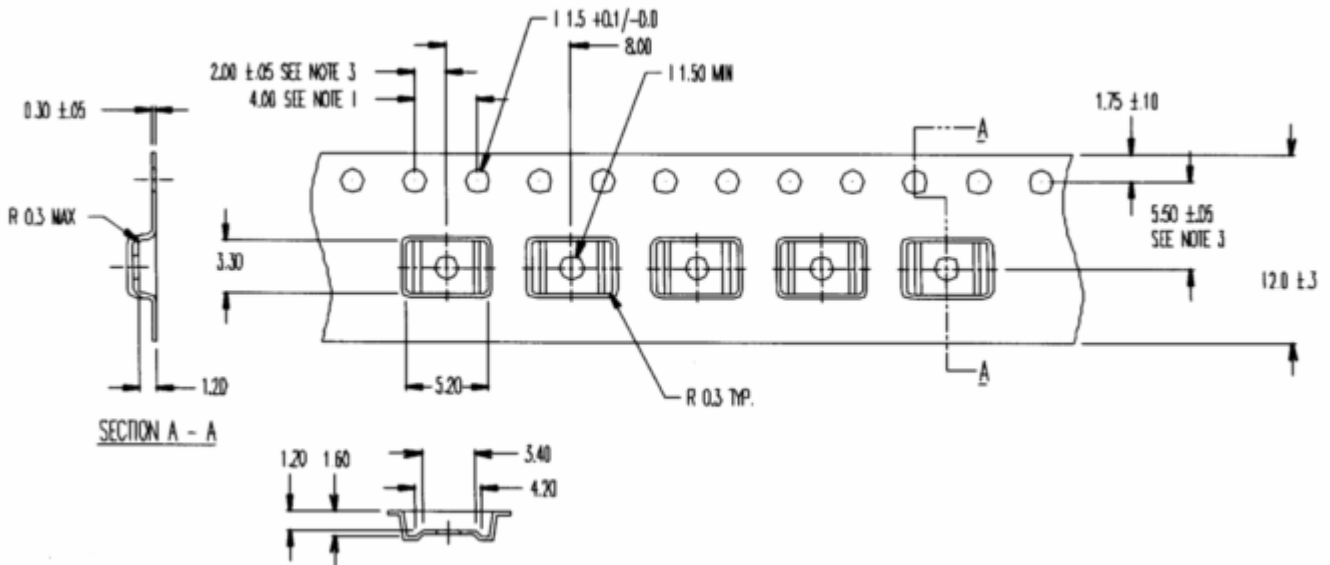
MSOP 8L

包裝方式: 2500 EA/PER REEL 1 REEL/BOX



TAPE AND REEL (CONT.)

PACKING METHOD: 2,500PCS/REEL, 1 REEL/BOX



NOTES:

1. 1D SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

X.XXX $X \pm 0.0025$
 X.XXX ± 0.005
 X.XX ± 0.025
 X.X ± 0.10
 X. ± 0.25
 尺寸單位 M.M.



PART MARKING

MSOP8 TOP MARKING

1102
MAAC

MSOP8 BACK MARKING

YYWW



ORDERING INFORMATION

AAT xxxxx-xx-x

AAT Part Number

Package Code 2
T=Taping Reel
Blank=Tube or Tray

Remark:
T=Taping Reel
PS.
MSop8→2,500pcs/reel

Package Code 1
Msop8: M