CYPRESS SEMICONDUCTOR

Multipurpose BiCMOS PLD

Features

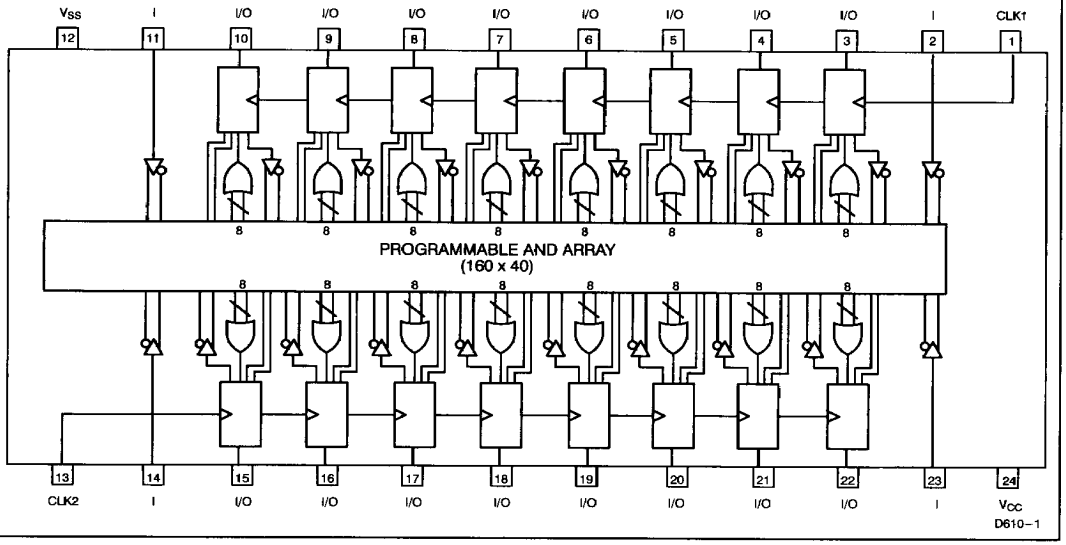
- **Function, pin, and JEDEC compatible with EP600, EP610, EP630, 85C060, and PALCE610 PLDs**
- **Very high performance**
  - **— t_{PD} = 10 ns**
- **16 I/O macrocells, each having:**
  - **— Choice of combinatorial or registered output**
  - **— Registers programmable to T-type and D-type**
  - **— Emulation of RS and JK flip-flops**
  - **— Array feedback from I/O pin or register**
  - **— Array feedback from I/O pin or register**
  - **— Product term controlled asynchronous reset**
  - **— Programmable output polarity control**
- **160 product terms**
- **Available in 24-pin, 300-mil PDIP and cerDIP, and 28-pin, J-leaded chip carriers, PLCCs, and LCCs**
- **Advanced BiCMOS technology**
- **Programmable security bit**

Functional Description

The PLD610 is a 24-pin, multipurpose, high-performance PLD with 16 I/O macrocells, 4 dedicated inputs, and 2 global clock inputs.

CLK1 provides the synchronous clock input for one bank of eight macrocells, and CLK2 provides the synchronous clock input for the other bank of eight macrocells. Output enable and selection of asynchronous or synchronous clock source are controlled with one dedicated product term per macrocell. An asynchronous reset product term is provided for each macrocell.

Logic Block Diagram



Selection Guide

		PLD610–10	PLD610–12	PLD610–15	PLD610–25
I_{CC1} (mA)	Commercial	130	130	130	130
	Military		170	170	170
t_{PD} (ns)	Commercial	10	12	15	25
	Military		12	15	25
t_S (ns)	Commercial	7	8	9	20
	Military		8	10	20
t_{CO} (ns)	Commercial	7	9	10	15
	Military		9	10	15

Functional Description (continued)

Each macrocell also has a register that can be programmed to be a D-type or T-type register. Other programmable options include output polarity, registered or combinatorial output, feedback to the array from the I/O pin or from the register output, and whether the dedicated product term controls the output enable or the register clock.

The PLD610 is available in a wide variety of packages including 24-pin, 300-mil plastic and ceramic DIPs, 28-pin, square J-leaded, ceramic chip carriers, 28-pin PLCCs, and 28-pin ceramic LCCs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC} Max.

DC Input Voltage ..... − 0.5V to (V_{CC} + 0.5V)

DC Input Current ..... − 30 mA to + 5 mA (except during programming)

DC Program Voltage 9.5V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 5%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[2]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[2]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			−250	50	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 6]			−30	−130	mA
I_{CC1}	Power Supply Current Standby[4]	V_{CC} = Max., V_{IH} = GND, Outputs Open	Com'l	−10		130	mA
				−12		150	mA
			Mil			170	
I_{CC2}	Power Supply Current at Frequency[5, 6]	V_{CC} = Max., Outputs Disabled (in High Z State), Device Operating at f_{MAX3}	Com'l	−10		130	mA
				−12		170	mA
			Mil			190	

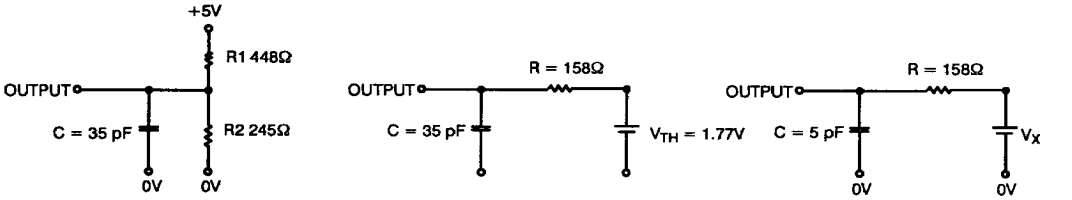
Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	10	pF

Notes:

1. T_A is the "instant on" case temperature.
2. Minimum DC input voltage is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by ground degradation.
4. Some of the devices compatible with Cypress's PLD610 have both a slow power-down mode and a faster turbo mode. Cypress's PAL610, however, only operates in a very fast turbo mode. In order to maintain full JEDEC compatibility, the Cypress PLD610 has two fuses that correspond to the turbo bits in other devices. Please note that the operation of the device is entirely independent of these "dummy" fuses. The PLD610 operates at very high speed regardless of whether the turbo bits are programmed (TURBO = ON) or unprogrammed (TURBO = OFF).
5. Tested with device programmed as a 16-bit counter.
6. Tested initially and after any design or process changes that may affect these parameters.

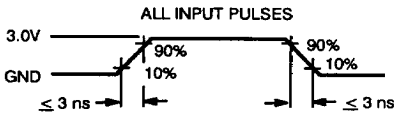
AC Test Loads and Waveforms



(a) Normal Load (Load 1) D610-7

(b) Thévenin Equivalent (Load 1) D610-8

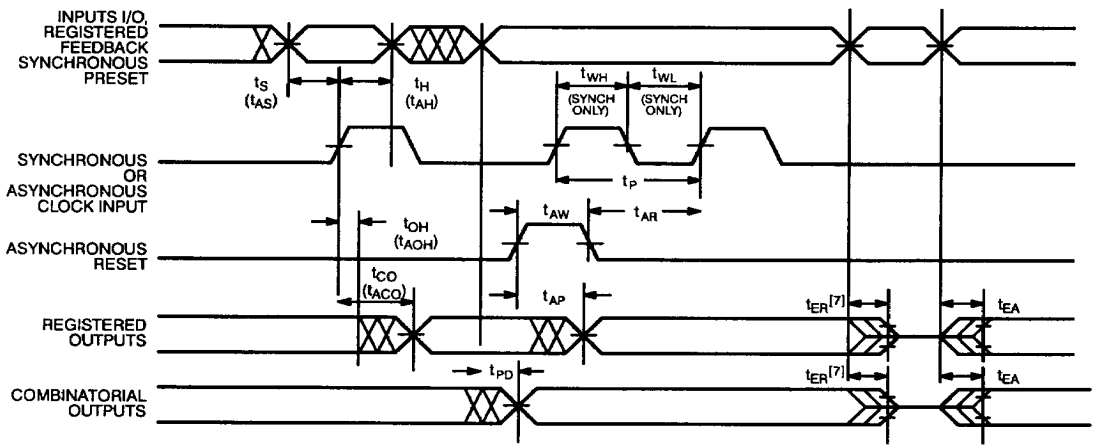
(c) Three-State Delay Load (Load 2) D610-9



(d) D610-2

Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	V_{OH}, 0.5V, V_X D610-3
$t_{ER(+)}$	2.6V	V_{OL}, 0.5V, V_X D610-4
$t_{EA(+)}$	V_{TH}	V_X, 0.5V, V_{OH} D610-5
$t_{EA(-)}$	V_{TH}	V_X, 0.5V, V_{OL} D610-6

Switching Waveform



D610-10

Note:
7. AC test load (Load 1) used for all parameters except where noted.

Switching Characteristics[7]

Parameters	Description		PLD610–10 Min.	PLD610–10 Max.	PLD610–12 Min.	PLD610–12 Max.	PLD610–15 Min.	PLD610–15 Max.	PLD610–25 Min.	PLD610–25 Max.	Units
t_{PD}	Input to Output Propagation Delay[8]	Com'l		10		12		15		25	ns
		Mil				12		15		25	
t_{EA}	Input to Output Enable Delay[8]	Com'l		12		14		15		25	ns
		Mil				14		16		25	
t_{ER}	Input to Output Disable Delay[8, 9]	Com'l		12		14		15		25	ns
		Mil				14		16		25	
t_{CO}	Clock to Output Delay[8]	Com'l		7		9		10		15	ns
		Mil				9		10		15	
t_S	Input or Feedback Set-Up Time	Com'l	7		8		9		20		ns
		Mil			8		10		20		
t_H	Input Hold Time	Com'l	0		0		0		0		ns
		Mil			0		0		0		
t_P	External Clock Period (t_{CO} + t_S)[6]	Com'l	14		17		19		35		ns
		Mil			17		20		35		
t_{WH}	Clock Width HIGH[6]	Com'l	4		5		6		10		ns
		Mil			5		6		10		
t_{WL}	Clock Width LOW[6]	Com'l	4		5		6		10		ns
		Mil			5		6		10		
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[6, 10]	Com'l	71.4		58.8		52.6		28.6		MHz
		Mil			58.8		41.7		28.6		
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[6, 11]	Com'l	125		100		83.3		50		MHz
		Mil			100		83.3		50		
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CNT})$)[6, 4, 12]	Com'l	100		83.3		83.3		40		MHz
		Mil			83.3		66.6		40		
t_{CNT}	Minimum Clock Period with Internal Feedback[6, 13]	Com'l		10		12		12		25	ns
		Mil				12		15		25	
t_{AW}	Asynchronous Reset Width[6]	Com'l	8		10		12		25		ns
		Mil			10		12		25		
t_{AR}	Asynchronous Reset Recovery Time[6]	Com'l	10		12		15		25		ns
		Mil			12		15		25		
t_{AP}	Asynchronous Reset to Registered Output Delay[8]	Com'l		12		14		16		30	ns
		Mil				14		16		30	
t_{OH}	Output Data Stable Time from Synchronous Clock Input	Com'l	1		1		1		1		ns
		Mil			1		1		1		
t_{AS}	Input Set-Up Time to Asynchronous Clock	Com'l	5		6		6		8		ns
		Mil			6		7		8		
t_{AH}	Input Hold Time from Asynchronous Clock	Com'l	5		6		6		12		ns
		Mil			6		7		12		
t_{ACO}	Asynchronous Clock to Output Delay[8]	Com'l		12		13		15		27	ns
		Mil				13		15		27	
t_{ACNT}	Minimum Asynchronous Clock Period with Internal Feedback[6]	Com'l		10		12		14		25	ns
		Mil				12		15		25	

Switching Characteristics[5] (continued)

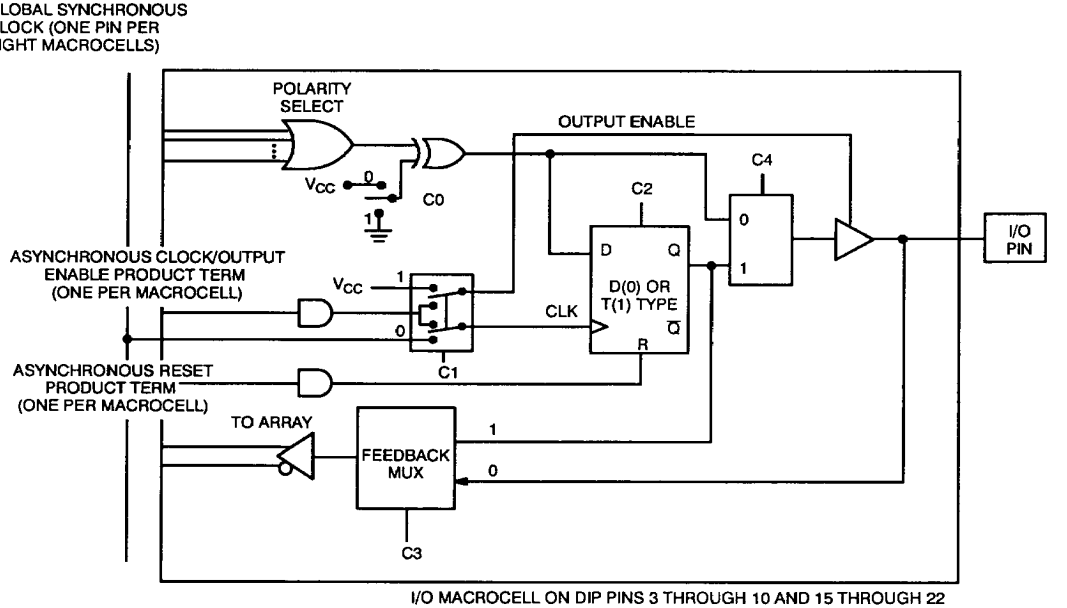
Parameters	Description		PLD610–10 Min.	PLD610–10 Max.	PLD610–12 Min.	PLD610–12 Max.	PLD610–15 Min.	PLD610–15 Max.	PLD610–15 Min.	PLD610–15 Max.	Units
f_{MAXA1}	External Maximum Frequency Asynchronous $(1/(t_{AS} + t_{ACO}))$[6]	Com'l	58.8		52.6				28.6		MHz
		Mil			52.6		45.5		28.6		
f_{MAXA2}	Internal Maximum Frequency Asynchronous $1/t_{ACNT}$[6]	Com'l	100		83.3				40		MHz
		Mil			83.3		66.6		40		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input	Com'l	1.5		1.5					1.5	ns
		Mil			1.5		1.5		1	1.5	

Notes:
8. This specification is guaranteed for eight or fewer outputs changing state in a given access cycle.
9. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max. (See Load 2.)
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
13. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 11).

Programming

The PLD610 can be programmed using the QuickPro II programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG, and other programmers. Please contact your local Cypress representative for further information.

I/O Macrocell

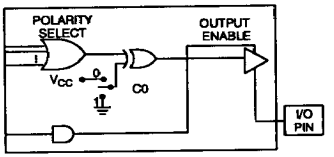


I/O MACROCELL ON DIP PINS 3 THROUGH 10 AND 15 THROUGH 22

D610–11

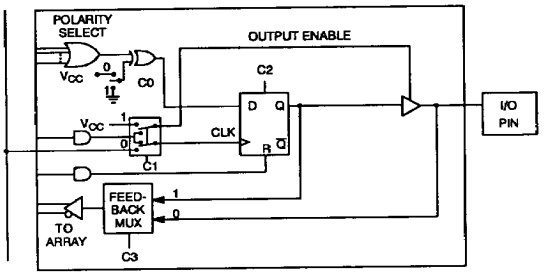
Macrocell Configurations

Combinatorial



D610–12

D-Type Flip-Flop

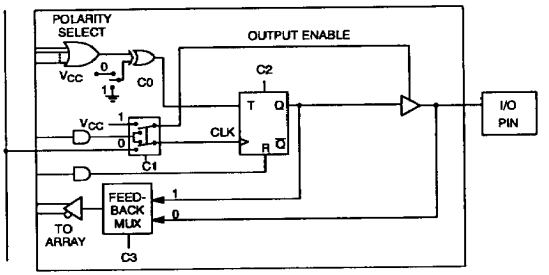


D610–13

State Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Toggle Flip-Flop

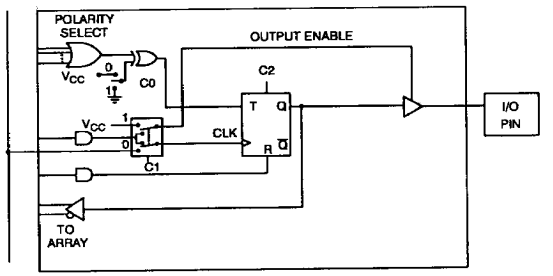


D610–14

State Table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

JK and RS Flip-Flops



D610–15

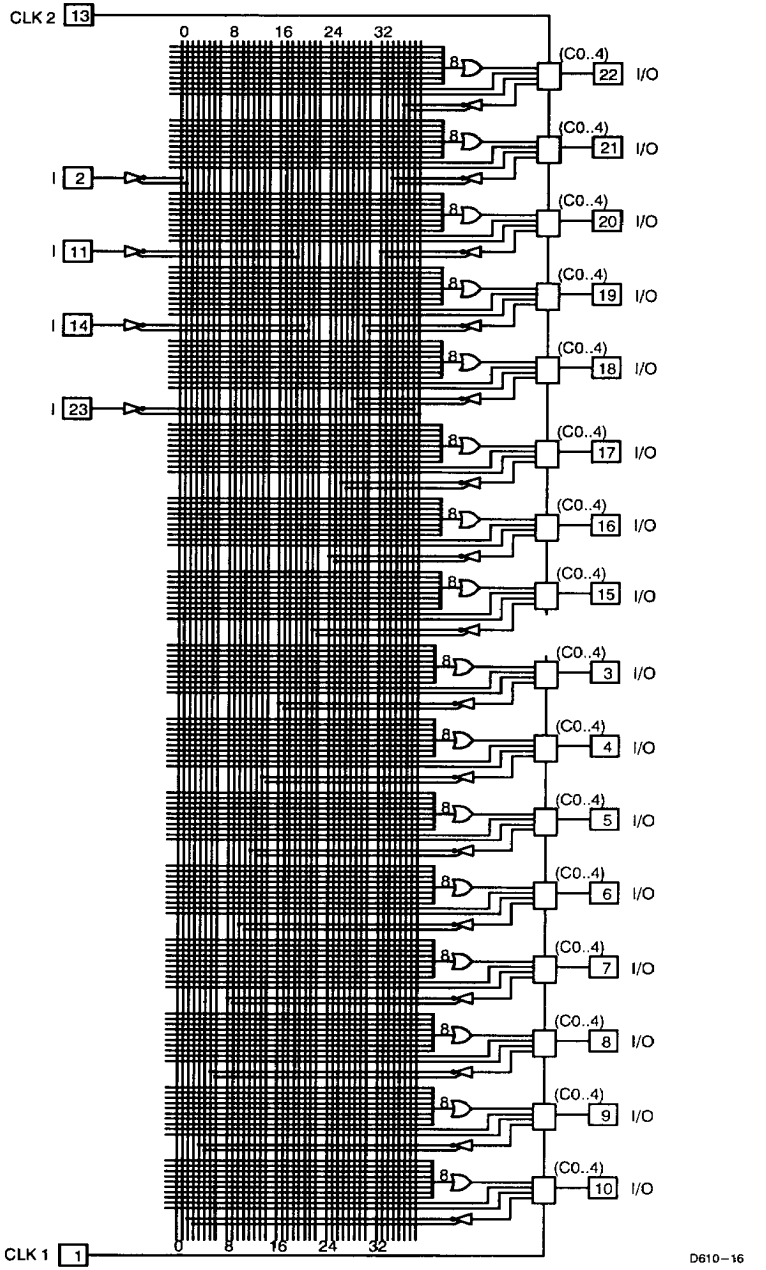
JK State Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

RS State Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

Block Diagram



Ordering Information

t_{PD} (ns)	f_{MAX3} (MHz)	Ordering Code	Package Type	Operating Range
10	100	PLD610–10DC	D14	Commercial
		PLD610–10JC	J64	
		PLD610–10PC	P13	
12	83.3	PLD610–12DC	D14	Commercial
		PLD610–12JC	J64	
		PLD610–12PC	P13	
		PLD610–12DMB	D14	Military
		PLD610–12LMB	L64	
15	83.3	PLD610–15DC	D14	Commercial
		PLD610–15JC	J64	
		PLD610–15PC	P13	
	66.6	PLD610–15DMB	D14	Military
		PLD610–15LMB	L64	
25	40	PLD610–25DC	D14	Commercial
		PLD610–25JC	J64	
		PLD610–25PC	P13	
		PLD610–25DMB	D14	Military
		PLD610–25LMB	L64	

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