National Semiconductor

GAL20RA10-15, -20, -25 Generic Array Logic

General Description

The NSC E²CMOS™ GAL® device combines a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The GAL20RA10 is made up of ten Output Logic Macro Cells (OLMC). Four programmable AND array outputs feed into the fixed OR-gate for each OLMC to generate the device's output functions. Four other AND array outputs are used for control functions in the OLMC. With a robust mixture of logic derived controlled functions and selectable output data paths, the GAL20RA10 provides an ideal solution for registered random logic applications.

This device is housed in a 24-pin 300 mil DIP. A 28-pin PCC package is also available. It can be programmed by most PAL programmers.

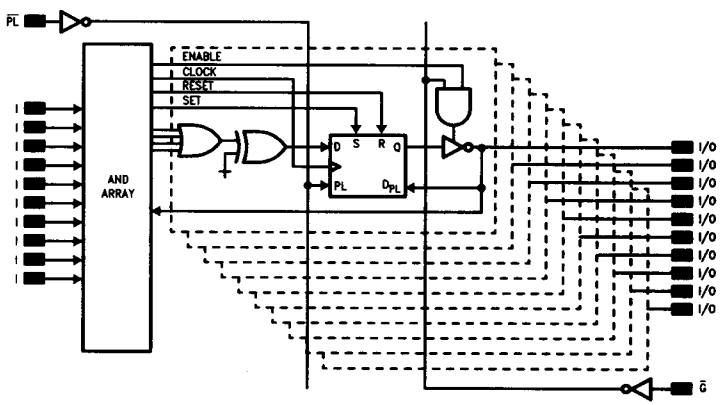
Programming is accomplished using industry standard available hardware and software tools. NSC guarantees a minimum 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability of the GAL devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

Features

- High performance E²CMOS technology
  - 15 ns maximum propagation delay
  - f_{CLK} = 45 MHz
  - 15 ns maximum from clock input to data output
  - TTL compatible 16 mA outputs
  - UltraMOS® III advanced CMOS technology
- Electrically erasable cell technology
  - Reconfigurable logic
  - Reprogrammable cells
  - 100% tested/guaranteed 100% yields
  - High speed electrical erasure (<50 ms)
  - 20 year data retention
- 10 output logic macrocells
  - Maximum flexibility for complex logic designs
  - Programmable output polarity
  - Programmable asynchronous set and reset
  - Individually programmable clocks
  - Programmable and dedicated pin control of output TRI-STATE®
  - Programmable Register bypass
  - TTL level Register preload
- Power-up reset for registered outputs
- JEDEC-compatible programming equipment and development software available
- Preload and power-up reset of all registers
  - 100% functional testability
- Full supported development software
- Electronic signature for identification
- Security fuse prevents direct copying of logic patterns
- JEDEC map identicle to Bipolar PAL versions
- Fully supported by National OPAL™ and OPALjr development software

Block Diagram—GAL20R10



*Output macrocell shown is configured as an active high register output.

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
Input Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Off-State Output Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Output Current	±100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	65°C to +125°C
Junction Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance	550V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

SUPPLY VOLTAGE AND TEMPERATURE

Symbol	Parameter	Commercial			Industrial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	4.5	5	5.5	V
T_A	Operating Free-Air Temperature	0	25	75	−40	25	85	°C

AC TIMING REQUIREMENTS

Symbol	Parameter		GAL20RA10-15 COM		GAL20RA10-20 IND		GAL20RA10-25 COM		Units
			Min	Max	Min	Max	Min	Max	
t_{SU}	Set-Up Time (Input or Feedback before Clock		7		10		15		ns
t_H	Hold Time (Input after Clock)		0		0		0		ns
t_W	Clock Pulse Width (High/Low)		10		12		15		ns
t_{CYCLE}	Clock Cycle Period (with Feedback) (Note 3)		22		30		40		ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback	45		33		25.0		MHz
		Without Feedback	50.0		41.7		33.3		MHz
f_I	Input Frequency (Note 5)		66.7		50.0		40.0		MHz
t_{PR}	Clock Valid after Power-Up		100		100		100		ns
t_{RESET}	Power-Up to Register Output			45		45		45	µs
t_{ARW}	Asynchronous Reset Pulse Width		15		20		25		ns
t_{APW}	Asynchronous Preset Pulse Width		10		12		15		ns
t_{REC}	Asynchronous Reset/Preset Recovery Time		10		12		15		ns
t_{WP}	Preload Pulse Width		15		20		25		ns
t_{SUP}	Preload Setup Time		10		15		20		ns
t_{HP}	Preload Hold Time		10		15		20		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: $t_{CYCLE} = t_{SU} + t_{CLK}$

Note 4: t_{CLK} (with feedback) = (t_{CYCLE}) 1
t_{CLK} (without feedback) = $(2\ t_W)$ 1

Note 5: $t_I = (t_{PD})$ 1

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Temperature Range	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0		V_{CC} + 1	V
V_{IL}	Low Level Input Voltage			−1.0		0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = **Min** I_{OH} = −3.2 mA	COM/IND	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = **Min** I_{OL} = 8 mA	COM/IND			0.5	V
I_{OZH}	High Level Off State Output Current	V_{CC} = **Max**, V_O = V_{CC} **Max**				10	μA
I_{OZL}	Low Level Off State Output Current	V_{CC} = **Max**, V_O = **GND**				−10	μA
I_I	Maximum Input Current	V_{CC} = **Max**, V_I = V_{CC} **Max**				10	μA
I_{IH}	High Level Input Current	V_{CC} = **Max**, V_I = V_{CC} **Max**				10	μA
I_{IL}	Low Level Input Current	V_{CC} = **Max**, V_I = **GND**				−10	μA
I_{OS}*	Output Short Circuit Current	V_{CC} = 5.0V, V_O = **GND**		−30		−150	mA
I_{CC}	Supply Current	f = 15 **MHz**, V_{CC} = **Max**	COM			100	mA
			IND			120	mA
C_I	Input Capacitance	V_{CC} = 5.0V, V_I = 2.0V				8	pF
$C_{I/O}$	I/O Capacitance	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V				10	pF

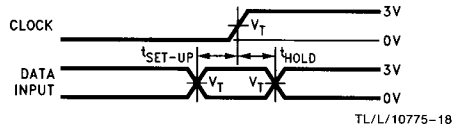
*One output at a time for a maximum duration of one second

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	GAL20RA10-15 COM		GAL20RA10-20 IND		GAL20RA10-25 COM		Units
			Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output	C_L = 50 pF, S1 Closed		15		20		25	ns
t_{CLK}	Clock Input to Registered Output or Feedback	C_L = 50 pF, S1 Closed		15		20		25	ns
t_S	Asynchronous Set Input to Registered Output Low			15		20		25	ns
t_R	Asynchronous Reset Input to Registered Output High			15		20		25	ns
t_{PZXG}	$\overline{G}$ Pin Output Enabled	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		12		15		20	ns
t_{PXZG}	$\overline{G}$ Pin Output Disabled	C_L = 5 pF, From V_{OH}: S1 Open, From V_{OL}: S1 Closed		12		15		20	ns
t_{PZXI}	Input to Output Enabled via Product Term	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		15		20		25	ns
t_{PXZI}	Input to Output Disabled via Product Term	C_L = 5 pF, From V_{OH}: S1 Open, From V_{OL}: S1 Closed		15		20		25	ns

Test Waveforms

Set-Up and Hold



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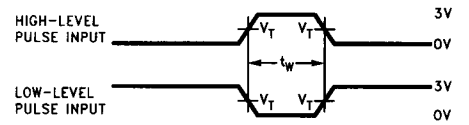
Pulse Width



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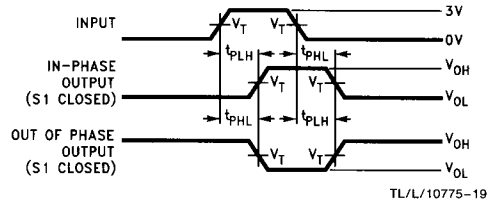
Propagation Delay



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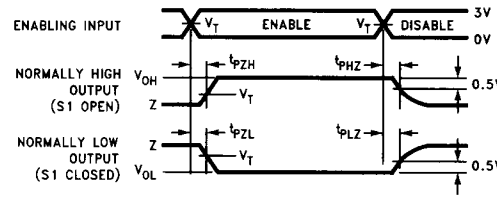
Enable and Disable



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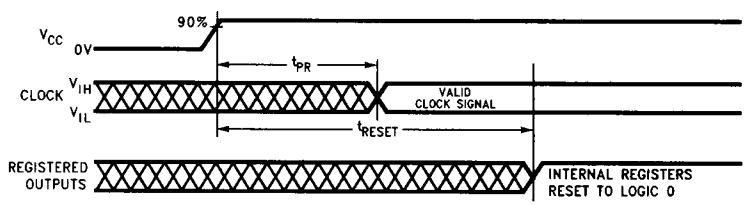
Notes:

V_T = 1.5V

C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Power-Up Reset Waveforms



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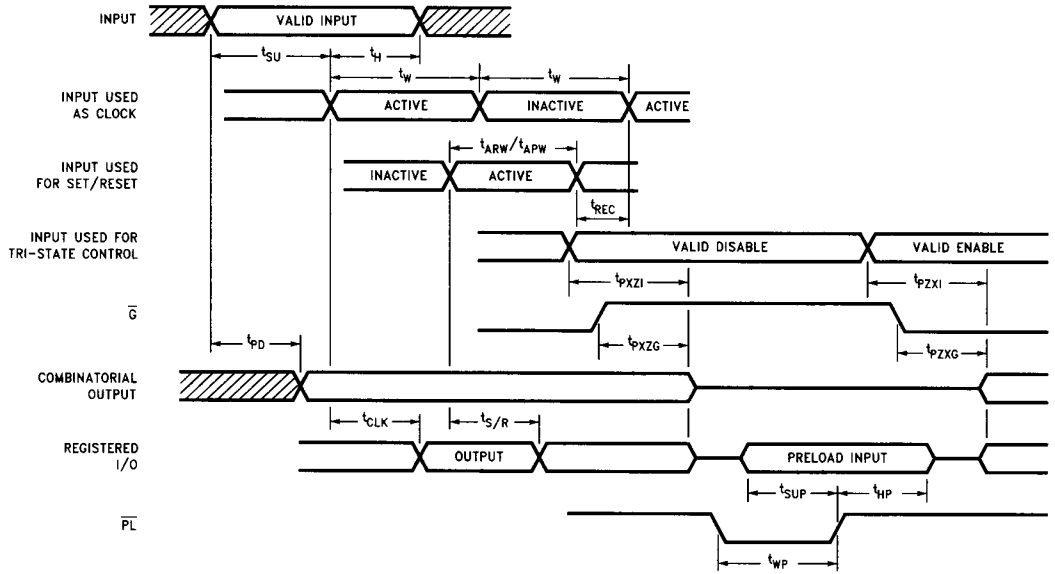
Switching Waveforms



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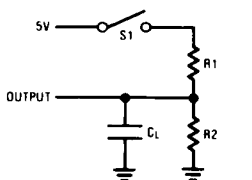
AC Test Load



COM/IND
R1 = 300Ω
R2 = 390Ω

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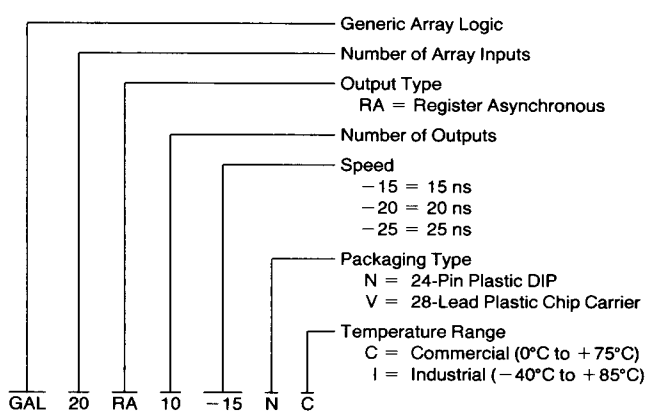
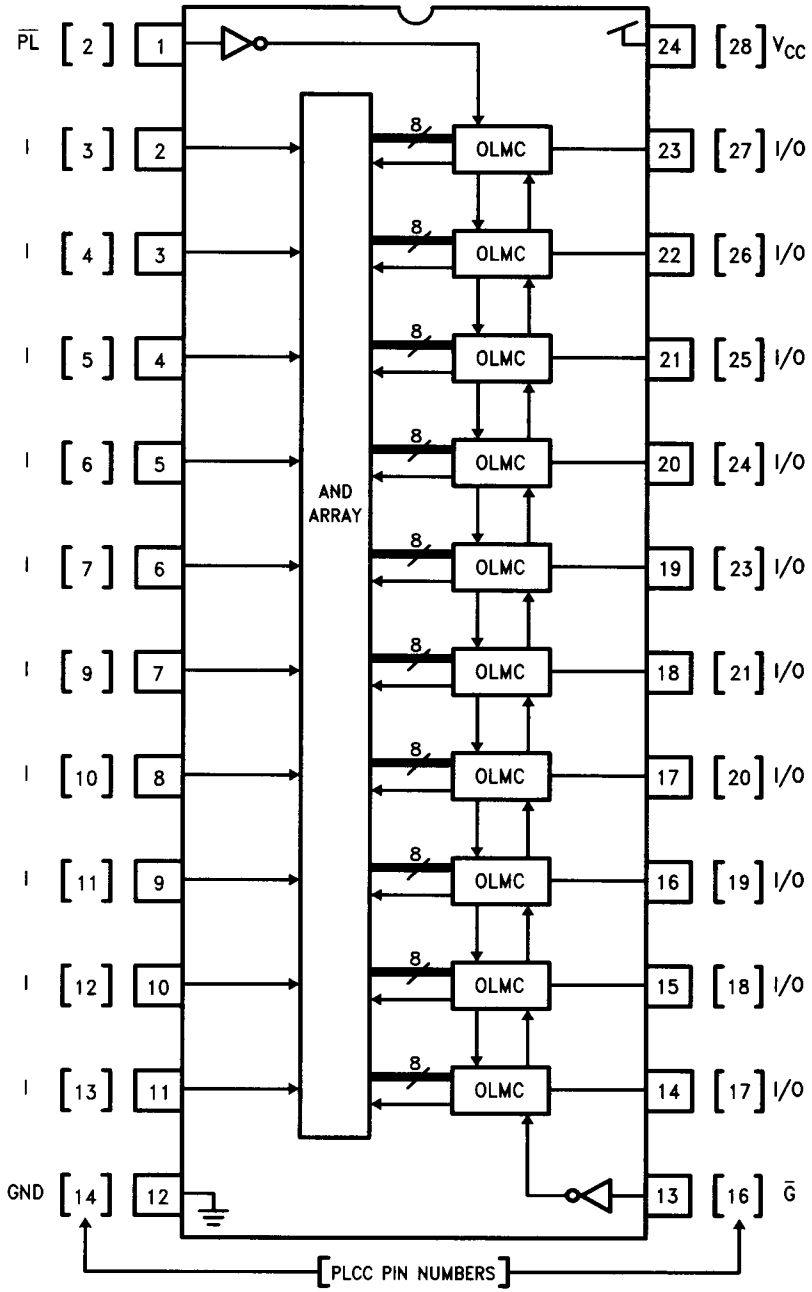
Ordering Information



GAL20RA10 Block Diagram—DIP Connections



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Functional Description

The GAL20RA10 logic array consists of 20 complementary input lines and 80 product-term lines with an EE programmable cell at each intersection (3200 cell). The product terms are organized into ten groups of eight each. Four of the eight product terms in each group connect into an OR-gate to produce the sum-of-products logic function. The remaining four product terms in each group are used for control functions in the "Output Logic Macro Cell" (OLMC).

As shown in the GAL20RA10 Block Diagram a total of ten output logic functions are available. Under control of an OLMC each output may be designated either as a registered output configuration or combinatorial.

The logic function output passes through a D-type Flip-Flop triggered by the rising edge of the clock which is defined by one product-term line.

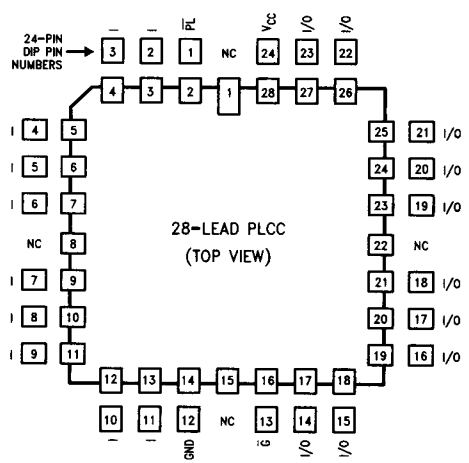
Two product-terms are designated to set or reset the output register and to define the output configuration (register or combinatorial).

Set	Reset	Output Mode
0	0	Register Mode
0	1	Reset
1	0	Set
1	1	Combinatorial Mode

All architecture cells are normally configured automatically by the development software.

Connection Diagram

28-Lead PLCC



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PROGRAMMABLE SET AND RESET

In each OLMC cell, two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic "1", the output pin becomes a "0". If the reset product line is high, the register output becomes a logic "0", the output pin becomes a "1". The operation of the programmable set and reset overrides the clock.

INDIVIDUALLY PROGRAMMABLE REGISTER BYPASS

If both the set and reset product lines are high, the sum-of-products bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

PROGRAMMABLE CLOCK

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.

PROGRAMMABLE AND HARD-WIRED TRI-STATE OUTPUTS

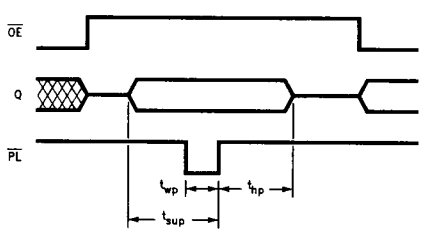
The GAL20RA10 provides a product term dedicated to output control. There is also an output control pin (Pin 13). The output is enabled if both the output control pin is low and the output control product term is HIGH. If the output control pin is high all outputs will be disabled or if an output control product term is low, then that output will be disabled.

PROGRAMMABLE OUTPUT POLARITY

The outputs can be programmed either active-low or active-high. This is represented by the exclusive-OR gates shown in the GAL20RA10 Logic Diagram. When the output polarity is unprogrammed the lower input to the exclusive-OR gate is high, so the output is active-high. Similarly, when the output polarity cell is 0, or a low impedance connection to GND, the output is active-low. The programmable output polarity features allows the user a high degree of flexibility when writing equations.

Output Register Preload

Register preload allows any arbitrary state to be loaded into the PAL output registers. This allows complete logic verification, including states that are impossible or impractical to reach. To use the preload feature, first disable the outputs by bringing $\overline{OE}$ high, and present the data at the output pins. A low-level on the preload pin ($\overline{PL}$) will then load the data into the registers.



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POWER-UP RESET

The GAL20RA10 device resets all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going transition.

Clock/Input Frequency Specifications

The clock frequency (f_{CLK}) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions feed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum "data window" period (t_W high + t_W low) and the minimum "data window" period (t_{SU} + t_H). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period ($t_{CYCLE} = f_{CLK}^{-1}$ with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle.

The input frequency (f_I) parameter specifies the maximum rate at which each GAL input can be toggled and still produce valid logic transitions on each combinatorial output. The f_I specification is derived as the inverse of the combinatorial propagation delay (t_{PD}).

Design Development Support

A variety of software tools and programming equipment is available to support the development of designs using GAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible "cell-map" (analogous to a PAL "fuse-map"). The industry-standard JEDEC format ensures that the resulting cell-map file can be down-loaded into a variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The OPAL™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. OPAL software also provides automatic device selection based on the designer's Boolean logic equations.

National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells. To ensure data retention and reliability, the programming algorithm also tracks the number of programming cycles to which each GAL device has been subjected since shipment, and stores this information automatically in the device.

The special GAL programming algorithm can also program a GAL device using a standard fuse-map developed for any of the emulated PAL products. PAL fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL device into the programming unit (provided the PAL device has not been secured). However, to utilize the full flexibility of the GAL architecture, true GAL development software (such as OPAL software) is recommended.

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL logic array and OLMC are provided for direct map editing and diagnostic purposes (see "Programming Details"). For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.

Security Cell

A security cell is provided on all GAL20RA10 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature

Each GAL device contains an electronic signature word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information is read out of the device using the normal program verification procedure provided by the programming equipment. The information may be accessed at anytime independent of the state of the security cell. National's OPAL development software allows electronic signature data to be entered by the user and downloaded to the programming equipment.

Bulk Erase

The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Latch-Up Protection

GAL devices are designed with an on-chip charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

To insure that no undesired bias conditions occur with P+ diffusions, a Latch-Lock™ power-up circuitry has been developed. The drain of all P channel devices normally connected to the device supply are now connected to an alternate supply that powers up after the device N-wells have been biased and the substrate has reached its negative clamp value. This prevents any hazardous bias conditions from developing in the power-up sequence. After power-up is complete, the Latch-Lock circuitry becomes dormant until a full power-down has occurred; this eliminates the chance of an unwanted P channel power-down during device operation.

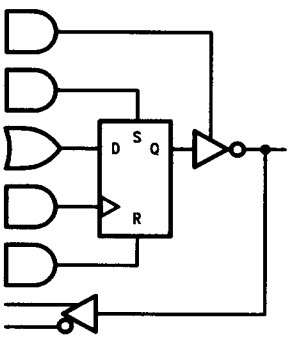
Manufacturer Testing

Because of E²CMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to data sheet specifications.

The testing procedure performed on all GAL devices by the manufacturer tests all aspects of device operation. Extensive testing of all programmable cells in the device include margin testing, internal verify, and program retention during high-temperature bake. All DC and AC parameters are tested at hot and cold temperatures using a variety of worst-case logic and signal patterns. Functional test include reprogramming each OLMC to all valid architectural configurations.

OLMC Configurations

Registered/Active Low



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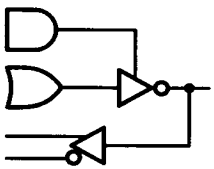
Combinatorial/Active Low



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Output Always Enabled

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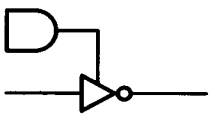
Programmable



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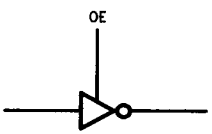
Hard-Wired



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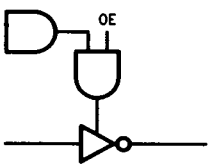
Combination of Programmable and Hard-Wired



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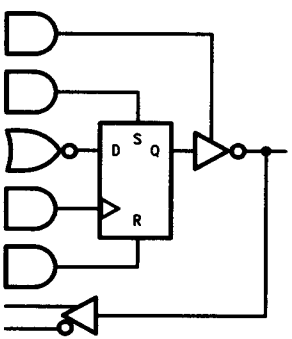
Registered/Active High



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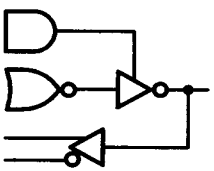
Combinatorial/Active High



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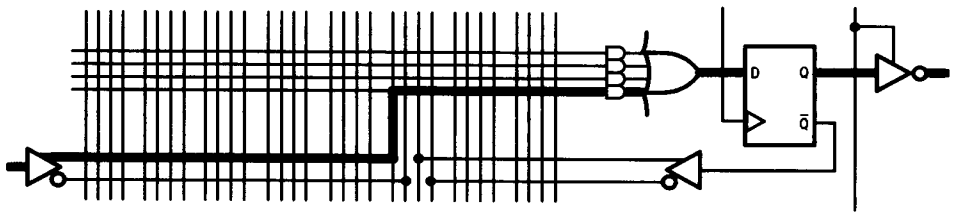
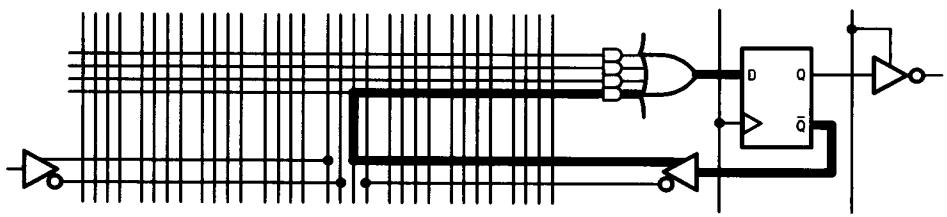
Functional Description

Typical Registered Logic Function Without Feedback

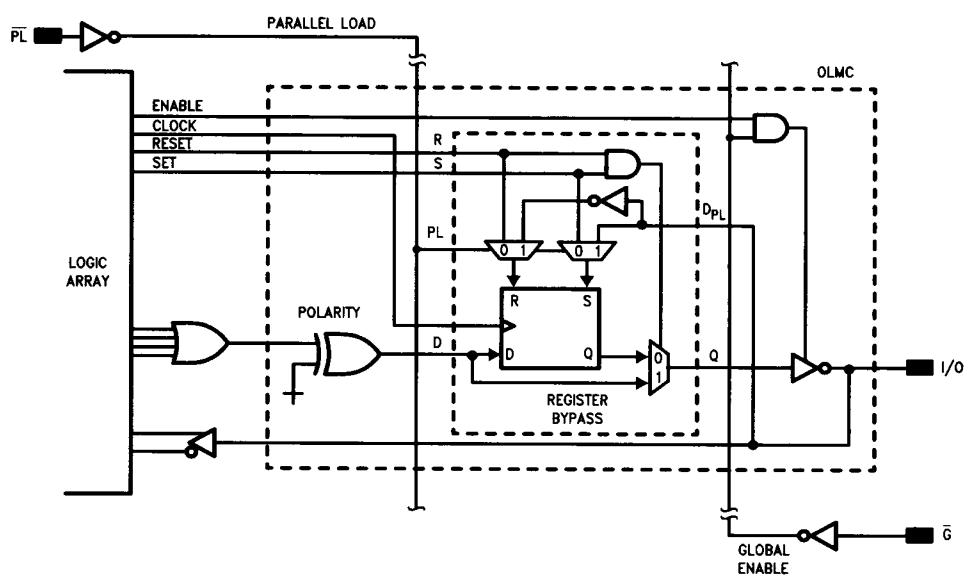


TL/L/10775–15

Typical Registered Logic Function With Feedback



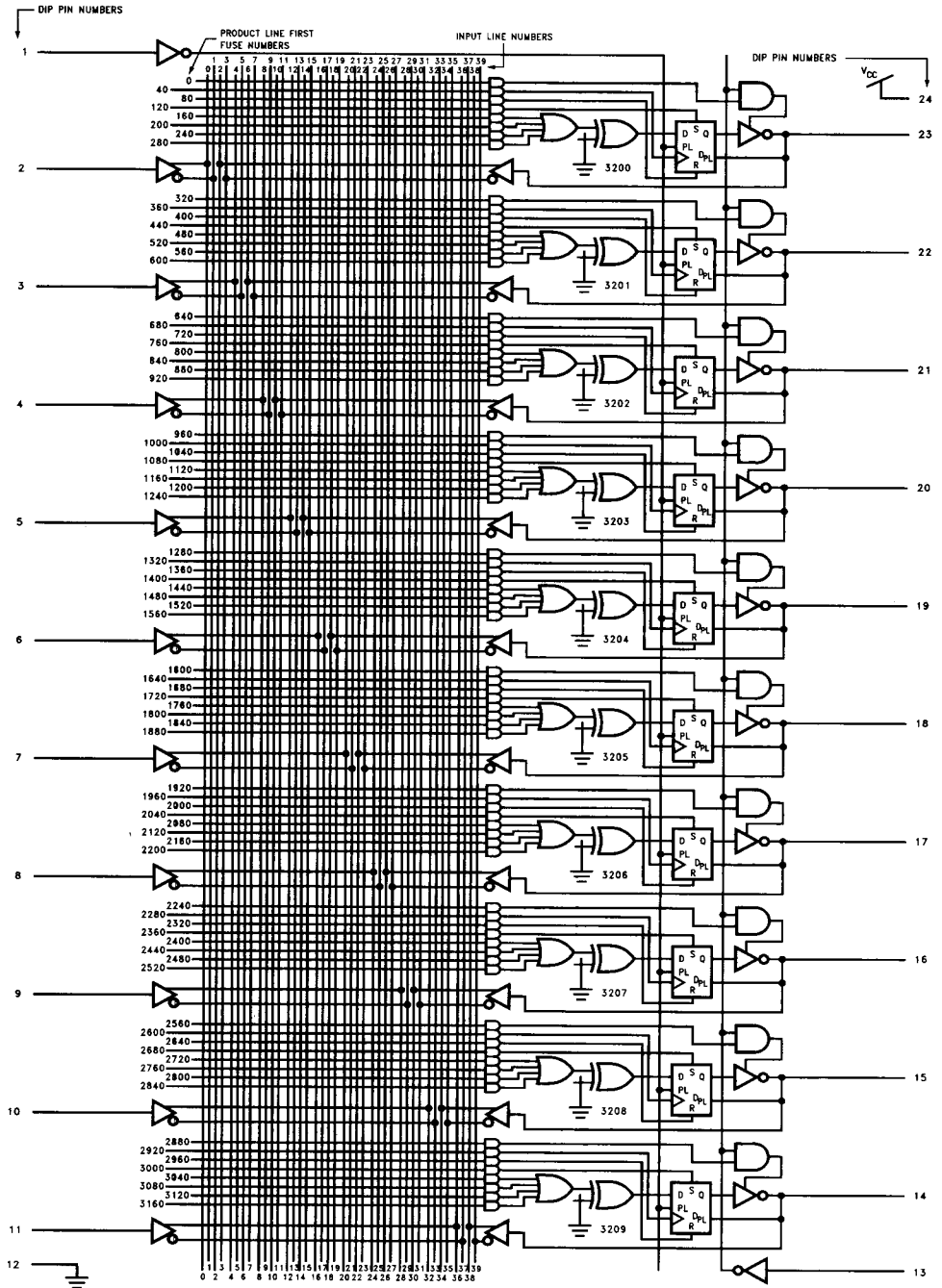
TL/L/10775–16



TL/L/10775–17

FIGURE 1. "RA" Output Logic Macrocell Logic Diagram

Logic Diagram—GAL20RA10



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JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number.