# Am79R100

Ringing Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Ideal for short-loop applications
  - ISDN terminal adaptor and NT1+, fixed radio access, PBX and cable telephony
- Through trapezoidal ringing
- On-chip ring-trip detector
- Low standby state power
- Battery operation:
  - V_{BAT1}: −15 V to −99 V
  - V_{BAT2}: −15 V to V_{BAT1}
- On-chip battery switching and feed selection
- On-hook transmission
- Two-wire impedance set by single external impedance

- Programmable constant-current feed
- Programmable Open Circuit voltage
- Programmable loop-detect threshold
- Current gain = 1000
- Ground-key detector
- Tip Open state for ground-start lines
- Polarity reversal option available
- Internal V_{EE} regulator (no external −5 V power supply required)
- Two on-chip relay drivers and snubber circuits
- Meets UL1950 safety requirements

BLOCK DIAGRAM

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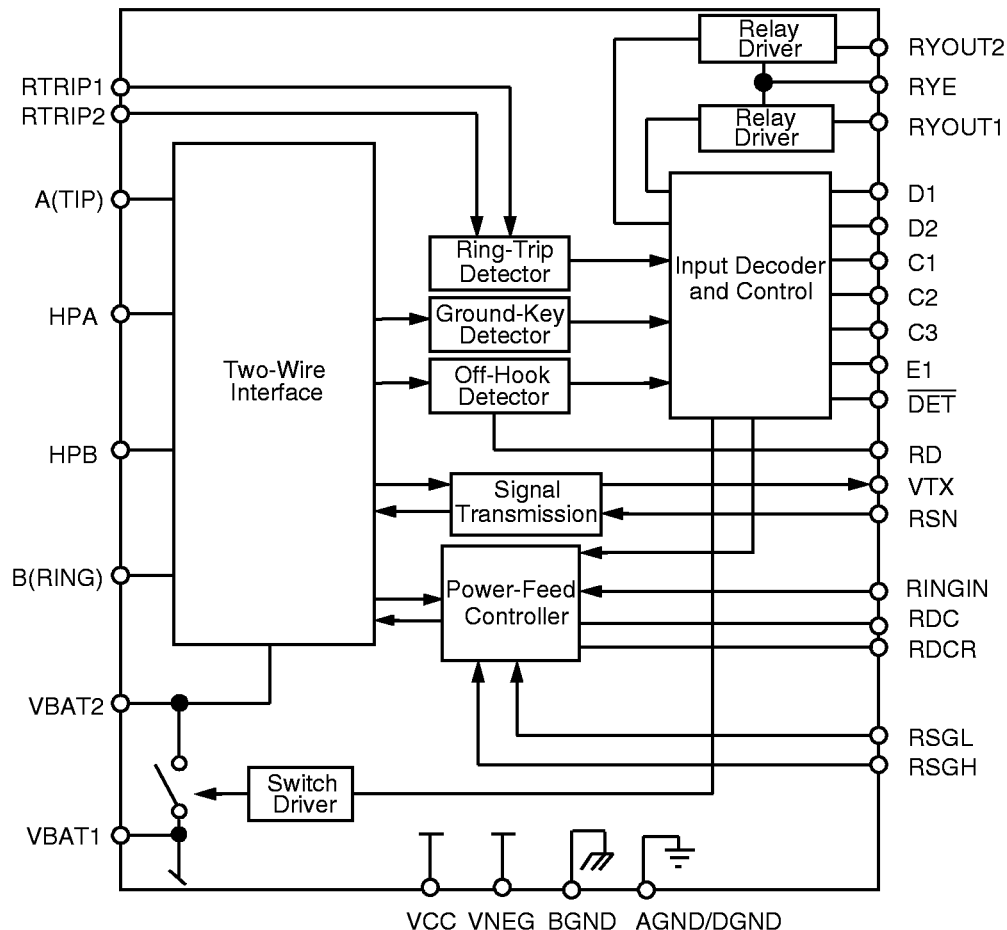
GENERAL DESCRIPTION

The AMD family of subscriber line interface circuit (SLIC) products provide the telephone interface functions required throughout the worldwide market. AMD SLIC devices address all major telephony markets including central office (CO), private branch exchange (PBX), digital loop carrier (DLC), fiber-in-the-loop (FITL), radio-in-the-loop (RITL), hybrid fiber coax (HFC), and cable telephony applications.

The AMD SLIC devices offer support of BORSHT (battery feed, overvoltage protection, ringing, supervision, hybrid, and test) functions with features including current limiting, on-hook transmission, polarity reversal, Tip Open, and loop-current detection. These features allow reduction of linecard cost by minimizing component count, conserving board space, and supporting automated manufacturing.

The AMD SLIC devices provide the two- to four-wire hybrid function, DC-loop feed, and two-wire supervision. Two-wire termination is programmed by a scaled impedance network. Transhybrid balance can be achieved with an external balance circuit or simply programmed using a companion AMD codec device, the Am79C02/03/031 DSLAC™ device, the Am79Q02/021/03 Programmable Quad SLAC (QSLAC™) device, or the Am79Q5457/4457 Nonprogrammable QSLAC device.

The Am79R100 Ringing SLIC device is a bipolar monolithic SLIC that offers on-chip ringing. Now designers can achieve significant cost reductions at the system level for reduced-loop applications by integrating the ringing function on chip. Examples of such applications

would be ISDN terminal adaptors, PBX, fiber-in-the-loop, radio-in-the-loop, hybrid fiber/coax and telephony (home-side) boxes. The Am79R100 Ringing SLIC can provide sufficient voltage to meet the stringent LSSGR five-ringer equivalent specification. Using a CMOS-compatible input waveform and wave shaping R-C network, the Am79R100 Ringing SLIC can provide trapezoidal wave ringing to meet various design requirements.
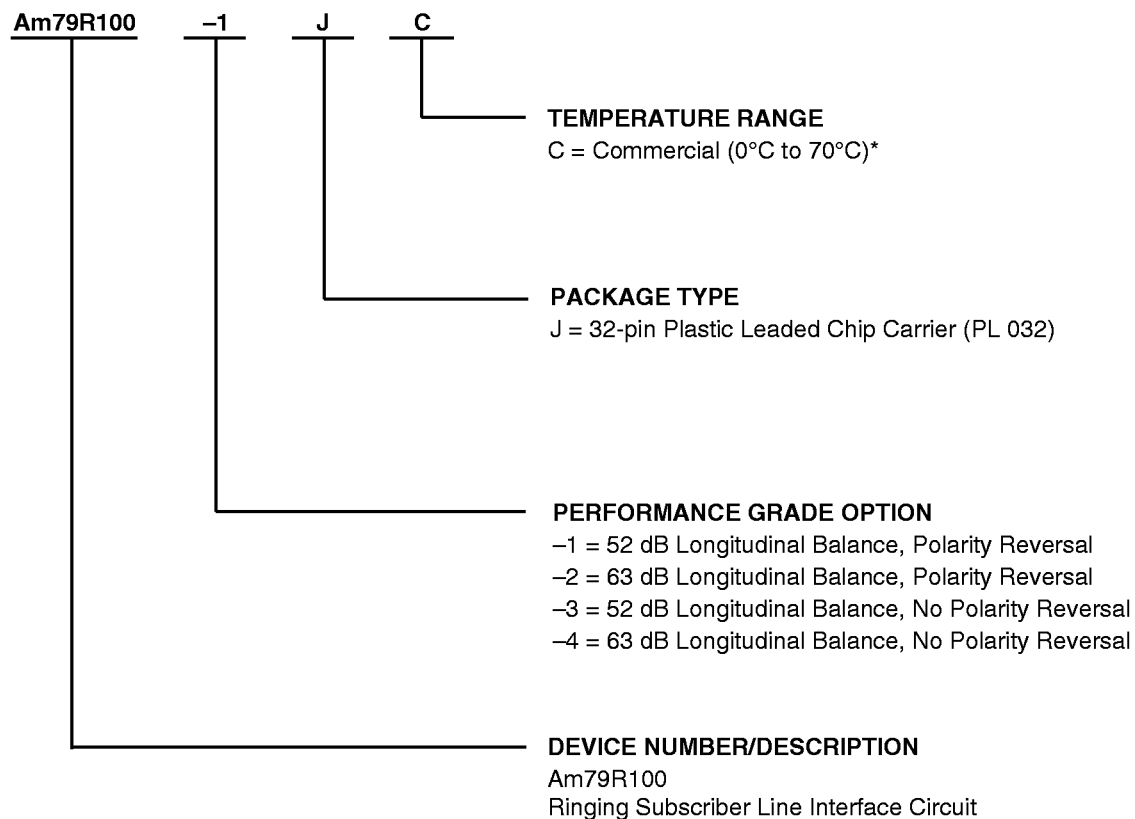
In order to further enhance the suitability of this device in short-loop, distributed switching applications, AMD has maximized power savings by incorporating battery switching on chip. The Am79R100 Ringing SLIC device switches between two battery supplies such that in the off-hook (active) state, a low battery is used to save power. In order to meet the Open Circuit voltage requirements of fax machines and maintenance termination units (MTU), the SLIC automatically switches to a higher voltage in the on-hook (standby) state.

Like all of the AMD SLIC devices, the Am79R100 Ringing SLIC device supports on-hook transmission, ring-trip detection, programmable loop-detect threshold, and is available with on-chip polarity reversal. The Am79R100 Ringing SLIC device is a programmable constant-current feed device with two on-chip relay drivers to operate external relays. Several performance grades are available to meet both ITU and LSSGR requirements, including various longitudinal balance options. This unique device is available in the 100 V bipolar process in a 32-pin PLCC package.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am79R100   –1   J   C

TEMPERATURE RANGE
C = Commercial (0°C to 70°C)*

PACKAGE TYPE
J = 32-pin Plastic Leaded Chip Carrier (PL 032)

PERFORMANCE GRADE OPTION
–1 = 52 dB Longitudinal Balance, Polarity Reversal
–2 = 63 dB Longitudinal Balance, Polarity Reversal
–3 = 52 dB Longitudinal Balance, No Polarity Reversal
–4 = 63 dB Longitudinal Balance, No Polarity Reversal

DEVICE NUMBER/DESCRIPTION
Am79R100
Ringing Subscriber Line Interface Circuit

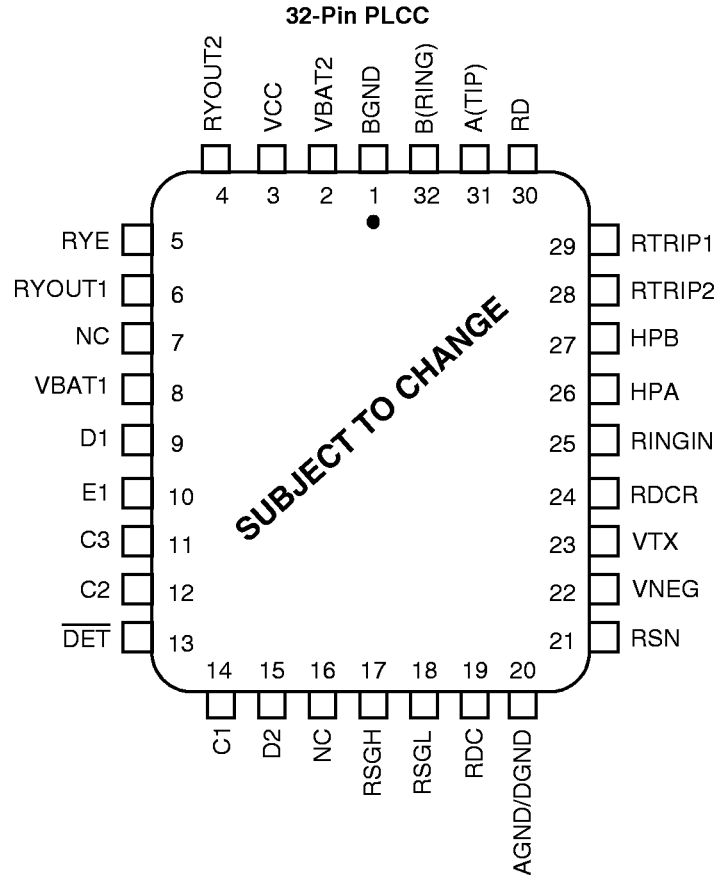| Valid Combinations		
Am79R100	–1	JC
	–2	
	–3	
	–4	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note:

* *Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

AMD

CONNECTION DIAGRAM

Top View

32-Pin PLCC

Pin	Signal
4	RYOUT2
3	VCC
2	VBAT2
1	BGND
32	B(RING)
31	A(TIP)
30	RD
5	RYE
6	RYOUT1
7	NC
8	VBAT1
9	D1
10	E1
11	C3
12	C2
13	DET
14	C1
15	D2
16	NC
17	RSGH
18	RSGL
19	RDC
20	AGND/DGND
21	RSN
22	VNEG
23	VTX
24	RDCR
25	RINGIN
26	HPA
27	HPB
28	RTRIP2
29	RTRIP1

SUBJECT TO CHANGE

Notes:

1. Pin 1 is marked for orientation.

2. NC = No connect

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and digital ground
A(TIP)	Output	Output of A(TIP) power amplifier
BGND	Gnd	Battery (power) ground
B(RING)	Output	Output of B(RING) power amplifier
C3–C1	Input	Decoder. SLIC control pins. C3 is MSB and C1 is LSB. TTL compatible.
D1	Input	Relay1 Control. TTL compatible. Logic Low activates the Relay1 relay driver.
D2	Input	Relay2 Control. (Option) TTL compatible. Logic Low activates the Relay2 relay driver.
$\overline{\text{DET}}$	Output	Switchhook Detector. When enabled, a logic Low indicates that a selected condition is detected. The detect condition is selected by the logic inputs (C3–C1 and E1). The output is open collector with a built-in 15 kΩ pull-up resistor.
E1	Input	Ground-Key Enable. (Option) A logic High selects the off-hook detector. A logic Low selects the ground-key detector. TTL compatible.
HPA	Capacitor	High-Pass Filter. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter. B(RING) side of high-pass filter capacitor.
NC	—	Not internally connected.
RD	Resistor	Detect Resistor. Detector threshold set and filter pin.
RDC	Output	DC Feed Resistor. Connection point for the DC-feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of VRDC is negative for normal polarity and positive for reverse polarity.
RDCR	—	Connection point for feedback during ringing.
RINGIN	Input	Ring Signal. Pin for ring signal input. Square-wave shaped by external RC filter. Requires 50% duty cycle. CMOS-compatible input.
RSGH	Input	Saturation Guard High. Pin for resistor to adjust Open Circuit voltage when operating from V_{BAT1}.
RSGL	Input	Saturation Guard Low. Pin for resistor to adjust the anti-saturation cut-in voltage when operating from both $V_{BAT1 \text{ and }} V_{BAT2}$.
RSN	Input	Receive Summing Node. The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.
RTRIP1	Input	Ring-Trip Detector. Ring-trip detector threshold set and filter pin.
RTRIP2	Input	Ring-Trip Detector. Ring-trip detector threshold offset (switch to V_{BAT1}). For power conservation in any nonringing state, this switch is open.
RYE	Output	Common Emitter of RYOUT1/RYOUT2. Emitter output of RYOUT1 and RYOUT2. Normally connected to relay ground.
RYOUT1	Output	Relay/Switch Driver. Open collector driver with emitter internally connected to RYE.
RYOUT2	Output	Relay/Switch Driver. (Option) Open collector driver with emitter internally connected to RYE.
VBAT1	Battery	Battery supply and connection to substrate.
VBAT2	Battery	Power supply to output amplifiers. Connect to off-hook battery through a diode.
VCC	Power	Positive analog power supply
VNEG	Power	Negative analog power supply. This pin is the return for the internal V_{EE} regulator.
VTX	Output	Transmit Audio. This output is a 0.5066 gain version of the A(TIP) and B(RING) metallic AC voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature .... –55°C to +150°C

V_{CC} with respect to AGND/DGND .... 0.4 V to +7 V

V_{NEG} with respect to AGND/DGND ...... 0.4 V to V_{BAT2}

V_{BAT2} .... V_{BAT1} to GND

V_{BAT1} with respect to AGND/DGND:

    Continuous .... +0.4 V to –104 V
    10 ms .... +0.4 V to –109 V

BGND with respect to AGND/DGND .... +3 V to –3 V

A(TIP) or B(RING) to BGND:

    Continuous .... V_{BAT1} –5 V to +1 V
    10 ms (f = 0.1 Hz) .... V_{BAT1} –10 V to +5 V
    1 µs (f = 0.1 Hz) .... V_{BAT1} –15 V to +8 V
    250 ns (f = 0.1 Hz) .... V_{BAT1} –20 V to +12 V

Current from A(TIP) or B(RING) .... ±150 mA

RYOUT1, RYOUT2 current .... 75 mA

RYOUT1, RYOUT2 voltage .... RYE to +7 V

RYOUT1, RYOUT2 transient .... RYE to +10 V

RYE voltage .... BGND to V_{BAT1}

C3–C1, D2–D1, E1

    Input voltage .... –0.4 V to V_{CC} + 0.4 V

ESD Immunity (Human Body Model) .... 1500 V min

Maximum power dissipation, continuous,

T_A = 85°C, No heat sink (See note):

    In 32-pin PLCC package .... 1.33 W

Thermal data: .... θ_{JA}

    In 32-pin PLCC package .... 45°C/W typ

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature .... 0°C to +70°C*

V_{CC} .... 4.75 V to 5.25 V

V_{NEG} .... –4.75 V to V_{BAT2}

V_{BAT1} .... –15 V to –99 V

V_{BAT2} .... –15 V to V_{BAT1}

AGND/DGND .... 0 V

BGND with respect to
    AGND/DGND .... –100 mV to +100 mV

Load resistance on VTX to ground .... 20 kΩ min

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)		Min	Typ	Max	Unit	Note
Transmission Performance							
2-wire return loss	200 Hz to 3.4 kHz (Test Circuit D)		26			dB	1, 4, 6
Z_{VTX}, analog output impedance				3	20	Ω	4
V_{VTX}, analog output offset voltage	0°C to +70°C		−35		+35	mV	
	−40°C to +85°C		−40		+40		4
Z_{RSN}, analog input impedance				1	20	Ω	
Overload level, 2-wire and 4-wire, off hook	Active state		2.5			Vpk	2a
Overload level, 2-wire	On hook, R_{LAC} = 600 Ω, OHT state		0.88			Vrms	2b
THD (Total Harmonic Distortion)	+3 dBm			−64	−50	dB	5
THD, on hook, OHT state	0 dBm, R_{LAC} = 600 Ω				−40		
Longitudinal Performance (See Test Circuit C)							
Longitudinal to metallic L-T, L-4 balance	200 Hz to 1 kHz	−1, −3*	52			dB	
	normal polarity	−2, −4	63				
	reverse polarity	−2	54				
	normal polarity, −40°C to +85°C	−2, −4	58				4
	1 kHz to 3.4 kHz	−1, −3*	52				
	normal polarity	−2, −4	58				
	reverse polarity	−2	54				
	normal polarity, −40°C to +85°C	−2, −4	54				4
Longitudinal signal generation 4-L	200 Hz to 800 Hz normal polarity		42				
Longitudinal current per pin (A or B)	Active or OHT state		8.5	17		mArms	4
Longitudinal impedance at A or B	0 to 100 Hz, T_A = +25°C			25		Ω/pin	
Idle Channel Noise							
C-message weighted noise	0°C to +70°C			+7	+11	dBrnC	
	−40°C to +85°C				+12		4
Psophometric weighted noise	0°C to +70°C			−83	−79	dBmp	
	−40°C to +85°C				−78		
Insertion Loss and Four- to Four-Wire Balance Return Signal (See Test Circuits A and B)							
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz		−0.20	0	+0.20		
Gain accuracy 2- to 4-wire and 4- to 4-wire	0 dBm, 1 kHz		−6.22	−6.02	−5.82		
Gain accuracy 4- to 2-wire	OHT state, on hook		−0.35	0	+0.35		3
Gain accuracy 2- to 4-wire and 4- to 4-wire	OHT state, on hook		−6.37	−6.02	−5.77		
Gain accuracy over frequency	300 to 3400 Hz 0°C to +70°C		−0.10		+0.10	dB	
	relative to 1 kHz −40°C to +85°C		−0.15		+0.15		
Gain tracking	+3 dBm to −55 dBm 0°C to +70°C		−0.10		+0.10		
	relative to 0 dBm −40°C to +85°C		−0.15		+0.15		3, 4
Gain tracking OHT state, on hook	0 dBm to −37 dBm 0°C to +70°C		−0.10		+0.10		
	−40°C to +85°C		−0.15		+0.15		
	+3 dBm to 0 dBm		−0.35		+0.35		3
Group delay	0 dBm, 1 kHz			3		µs	1, 4, 6

Note:
Performance Grade

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I_L, Loop-current accuracy, Active state	I_L in constant-current region	$0.915I_L$	I_L	$1.085I_L$		
I_L, Long loops, Active state	R_{LDC} = 600 Ω, RSGL = open	20	21.7		mA	
	R_{LDC} = 1250 Ω, RSGL = short Bat2 = −35 V	20				
I_LLIM	Active, A and B to ground		35	70	mA	
	OHT, A and B to ground		35			4
I_L, Loop current, Open Circuit state	R_L = 0			100	µA	
I_A, Pin A leakage, Tip Open state	R_L = 0			100		
I_B, Pin B current, Tip Open state	B to ground		34		mA	
VA, Standby, ground-start signaling	A to −48 V = 7 kΩ, B to ground = 100 Ω	−7.5	−5		V	4
V_{AB}, Open Circuit voltage	OHT state, RSGH = short	42.8		60		8
V_A, V_B, Open Circuit, Standby state				−60		10
I_L, Accuracy, Standby state	I_L = Resistive feed region $$I_L = \frac{54}{R_L + 400}, \text{Vbat} < -62$$	$0.8I_L$	I_L	$1.2I_L$	mA	
	I_L = constant-current region T_A = 25°C	18	27	39		
	T_A = −40°C to +85°C	18	27			4
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC}	50 Hz to 3400 Hz	33	50		dB	5
V_{NEG}	50 Hz to 3400 Hz	30	40			
V_{BAT1}	50 Hz to 3400 Hz	30	50			
V_{BAT2}	50 Hz to 3400 Hz	30	50			
Power Dissipation						
On hook, Open Circuit state			53		mW	
On hook, Standby state			61			10
On hook, OHT state			220			
On hook, Active state			240			
Off hook, Standby state, Instantaneous	R_L = 300 Ω		TBD	TBD		10
Off hook, OHT state	R_L = 300 Ω		TBD	TBD		
Off hook, Active state	R_L = 300 Ω		TBD	TBD		
Supply Currents						
I_{CC}, On-hook V_{CC} supply current	Open Circuit state		3.0	4.5	mA	
	Standby state		3.2	5.5		
	OHT state		6.2	8.0		
	Active state–normal		6.5	9.0		
I_{NEG}, On-hook V_{NEG} supply current	Open Circuit state		0.1	0.2	mA	
	Standby state		0.1	0.2		
	OHT state		0.7	1.1		
	Active state–normal		0.7	1.1		
I_{BAT1}, On-hook V_{BAT1} supply current	Open Circuit state		0.45	1.0		
	Standby state		0.6	1.5		
	OHT state		2.0	4.0		
	Active state–normal		2.7	5.0		
I_{BAT2} On-hook V_{BAT2} supply current	Active state–normal					

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Logic Inputs (C3–C1, D2–D1, and E1)						
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				
Logic Output $\overline{DET}$						
V_{OL}, Output Low voltage	I_{OUT} = 0.8 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				
Ring-Trip Detector Input						
Ring detect accuracy	See ring-trip detection equation.	–10		+10	%	
Ring Signal						
V_{AB}, Ringing	Ringload = 1570 Ω	90	93		Vpk	7
V_{AB} Ringing offset	V_{RINGIN} = 2.5 V	–10	0	10	V	
$\Delta V_{AB}/\Delta V_{RINGIN}$ (RINGIN gain)		150	180	210		
Off-hook current limit	R_L = 300 Ω	73	83	93	mA	
Ground-Key Detector Thresholds						
Ground-key current threshold	B to ground		11		mA	
Loop Detector						
R_{LTH}, Loop-resistance detect threshold	Active	–20		20		
	OHT	–20		20	%	9
I_{LTH}, Loop-current detect threshold	Standby	–12		12		
Relay Driver Output (RELAY1 and 2)						
V_{OL}, On voltage (each output)	I_{OL} = 30 mA		+0.25	+0.4	V	
V_{OL}, On voltage (each output)	I_{OL} = 40 mA		+0.30	+0.8		4
I_{OH}, Off leakage (each output)	V_{OH} = +5 V			100	µA	
Zener breakover (each output)	I_Z = 100 µA	6.6	7.9		V	
Zener on voltage (each output)	I_Z = 30 mA		11			

RELAY DRIVER SCHEMATIC
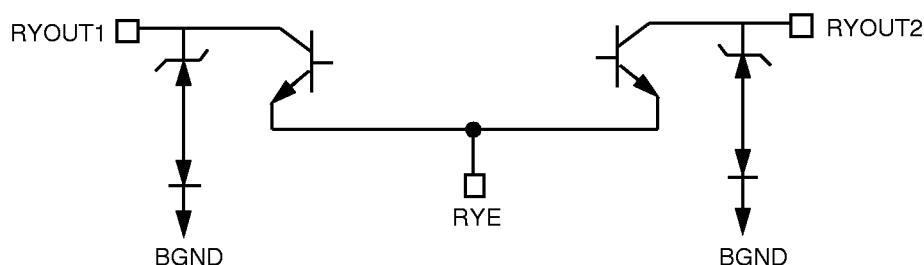
Notes:

1. Unless otherwise noted, test conditions are BAT1 = –99 V, BAT2 = –21 V, V_{CC} = +5 V, V_{NEG} = –5 V, R_L = 600 Ω, R_{DC1} = 50 kΩ, R_{DC2} = 50 kΩ, R_D = 75 kΩ, no fuse resistors, C_{HP} = 0.018 μF, C_{DC} = 1.2 μF, D_1 = D_2 = 1N400x, two-wire AC input impedance (ZSL) is a 600 Ω resistance synthesized by the programming network shown below. R_{SGL} = open, R_{SGH} = open, R_{DCR1} = 15 kΩ, R_{DCR2} = 15 kΩ, C_{DCR} = 10 nF, R_{RT1} = 600 kΩ, R_{RT2} = 12 kΩ, C_{RT} = 1.5 μF, R_{SLEW} = 100 kΩ, C_{SLEW} = 0.33 μF.
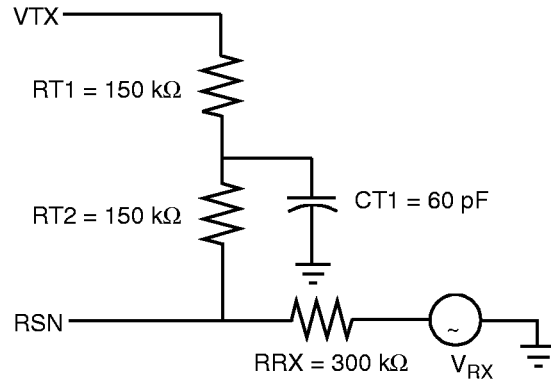
2. a. Overload level is defined when THD = 1%.
   b. Overload level is defined when THD = 1.5%.

3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the programmed impedance.

4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.

5. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.

6. Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than 2 μs and increases 2WRL. The effect of group delay on linecard performance may also be compensated for by synthesizing complex impedance with the QSLAC or DSLAC device.

7. 90 Vpk provides 64 Vrms with a crest factor of 1.25 to a load of 1400 Ω with 2 • Rf = 100, and Rline = 70 Ω (1570 Ω).

8. Open Circuit V_{AB} can be modified using RSGH. Longitudinal voltage in OHT state is 30 V limiting V_{AB} to 60 V.

9. R_D must be greater than 52 kΩ. Refer to Table 2 for typical value of R_{LTH}.

10. Conforms to UL1950.

Table 1. SLIC Decoding

State	C3 C2 C1	2-Wire Status	(DET) Output		Battery
			E1 = 1	E1 = 0	
0	0 0 0	Open Circuit	Ring trip	Ring trip	VBAT2
1	0 0 1	Ringing	Ring trip	Ring trip	VBAT1
2	0 1 0	Active	Loop detector	Ground key	VBAT2
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key	VBAT1
4	1 0 0	Tip Open	Loop detector	Ground key	VBAT1
5	1 0 1	Standby	Loop detector	Ground key	VBAT1
6*	1 1 0	Active Polarity Reversal	Loop detector	Ground key	VBAT2
7*	1 1 1	OHT Polarity Reversal	Loop detector	Ground key	VBAT1

Note:
* Only –1 and –2 performance grade devices support polarity reversal.

Table 2. User-Programmable Components

$Z_T = 500(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \dfrac{Z_L}{G_{42L}} \bullet \dfrac{1000 \bullet Z_T}{Z_T + 500(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \dfrac{2500}{I_{LOOP}}$ $R_{DCR1} + R_{DCR2} = \dfrac{2500}{Iringlim}$ $C_{DC} = 19 \text{ ms} \bullet \dfrac{R_{DC1} + R_{DC2}}{R_{DC1} R_{DC2}}$ $C_{DCR} = \dfrac{R_{DCR1} + R_{DCR2}}{R_{DCR1} R_{DCR2}} \bullet 150 \text{ μs}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. I_{LOOP} is the desired loop current in the constant-current region. R_{DCR1}, R_{DCR2}, and C_{DCR} form the network connected to the RDCR pin. See Applications Circuit for these components. C_{DCR} sets the ringing time constant, which can be between 15 μs and 150 μs.
$R_D = R_{LTH} \bullet 18$ for OHT state	R_D is the resistor connected from the RD pin to GND and R_{LTH} is the loop-resistance threshold between on-hook and off-hook detection. R_D should be greater than 52 kΩ to guarantee detection occurs in the Standby state. Choose the value of R_D for high battery state; then use the equation for R_{LTH} to find where the threshold is for low battery.
Loop-Threshold Detect Equations	
$R_{LTH} = \dfrac{R_D}{18}$ for OHT state	This is the same equation as for R_D above, except solved for R_{LTH}.
$R_{LTH} = \dfrac{R_D}{14.8}$ for Active state	For low battery, the detect threshold is slightly higher, which avoids oscillating between states.
$R_{LTH} = \dfrac{|V_{BAT1}| - 8}{825} \bullet R_D - 400 - 2R_F \qquad V_{BAT1} > -62 \text{ V}$ $R_{LTH} = \dfrac{54}{825} - R_D - 400 - 2R_F \qquad V_{BAT1} < -62 \text{ V}$	R_{LTH} standby < R_{LTH} OHT < R_{LTH} Active, which guarantees no unstable states under all operating conditions. This equation shows at what resistance the standby threshold is; it is actually a current threshold rather than a resistance threshold, which is shown by the Vbat dependency.
Ring-Trip Detection Equation	
$I_{RTD} = \left(\dfrac{|V_{BAT1}| - 1}{R_{RT1}} + I_{OFFSET} \right) \bullet 325$	$I_{OFFSET} = 8$ μA for ON transition $I_{OFFSET} = -20$ μA for OFF transition

AMD

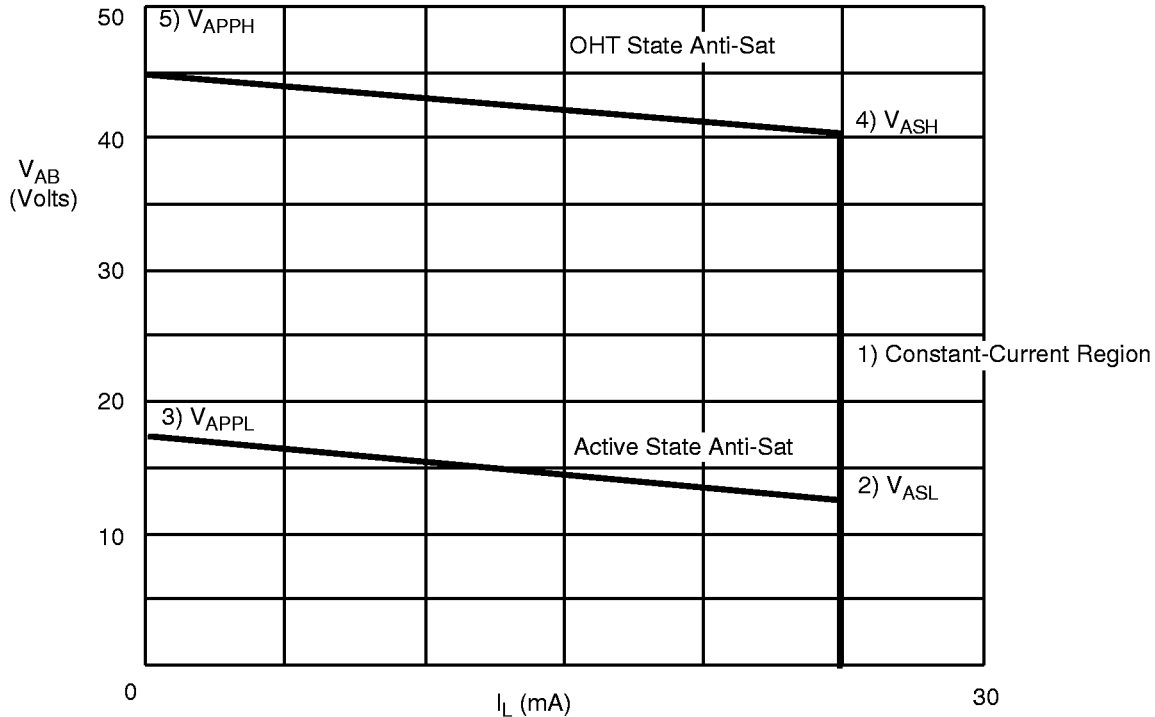## DC FEED CHARACTERISTICS (SEE NOTE 1)

Figure 1. Typical V_{AB} vs. I_L DC Feed Characteristics

Notes:

1. *Constant-current region:* $V_{AB} = I_L R_L = \dfrac{2500}{RDC} R_L$; *where* $R_L = R_L + 2R_F$,

2. *Active state Anti-sat region:*

$$V_{ASL} = \frac{61.44(125 \bullet 10^3 + R_{SGL})}{308 \bullet 10^3 + 4.92\ R_{SGL}}\ ;\quad \text{where } R_{SGL} = \text{open is default setting}$$

where R_{SGL} = resistor to GND. VASL increase.

$$V_{APPL} = 4.17 + V_{ASL}$$

$$I_{LOOPL} = \frac{V_{APPL}}{\dfrac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$$

3. *OHT state Anti-sat region:*

$$V_{ASH} = V_{ASHH} + V_{ASL}$$

$$V_{ASH} = \frac{61.44 \bullet (101 \bullet 10^3 + R_{SGH})}{223 \bullet 10^3 + 4\ R_{SGH}}\ ;\quad \text{where } R_{SGH} = \text{resistor to GND,}$$

R_{SGH} = 0 is default setting.

where R_{SGH} = open, V_{ASH} decrease.

$$V_{APPH} = 4.17 + V_{ASH}$$

$$I_{LOOPH} = \frac{V_{APPH}}{\dfrac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$$

RING-TRIP COMPONENTS

$R_{RT2} = 12 \text{ k}\Omega$

$C_{RT} = 1.5 \text{ }\mu\text{F}$

$$R_{RT1} = 300 \bullet CF \bullet \frac{V_{BAT1}}{Vbat - 3.5 - (15 \text{ }\mu A \bullet 300 \bullet CF \bullet (R_{LRT} + 150 + 2R_F))} \bullet (R_{LRT} + 150 + 2R_F)$$

where R_{LRT} = Loop-detection threshold resistance for ring trip and CF = Crest factor of ringing signal ($\approx$ 1.25)

R_{SLEW}, C_{SLEW}

Ring waveform rise time $\approx$ 0.214 $\bullet$ ($R_{SLEW} \bullet C_{SLEW}$) $\approx$ tr.

For a 1.25 crest factor @ 20 Hz, tr $\approx$ 10 mS.

$\therefore$ (R_{SLEW} = 150 kΩ, C_{SLEW} = 0.33 μF.)

C_{SLEW} should be changed if a different crest factor is desired.

0

Ringing Reference
(Input to R_{SLEW})

B(RING)

A(TIP)

Battery

This is the best time for
switching between Ringing
and other states for minimizing
detect switching transients.
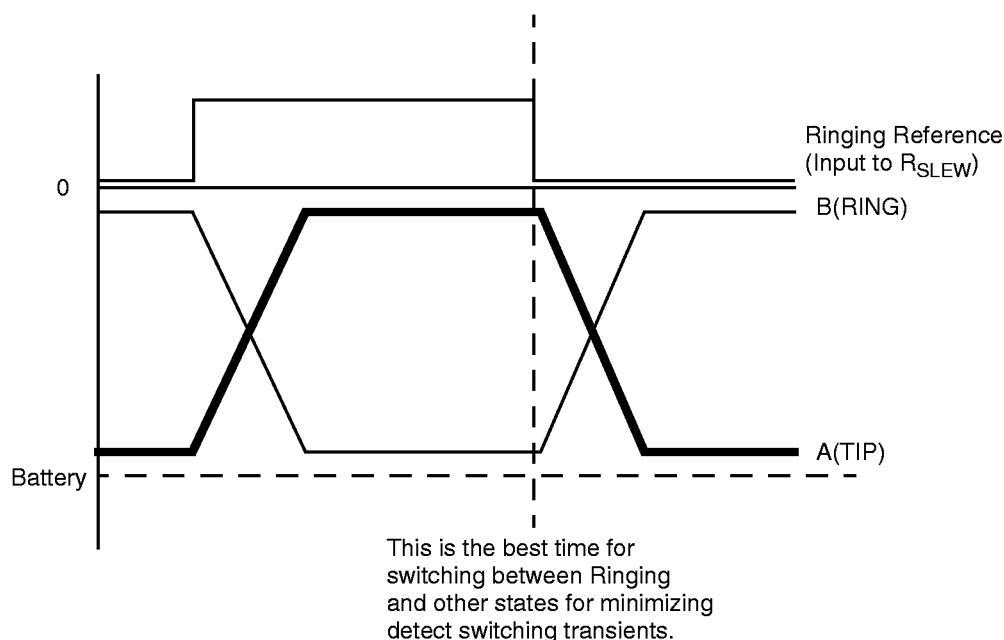
Figure 2. Ringing Waveforms
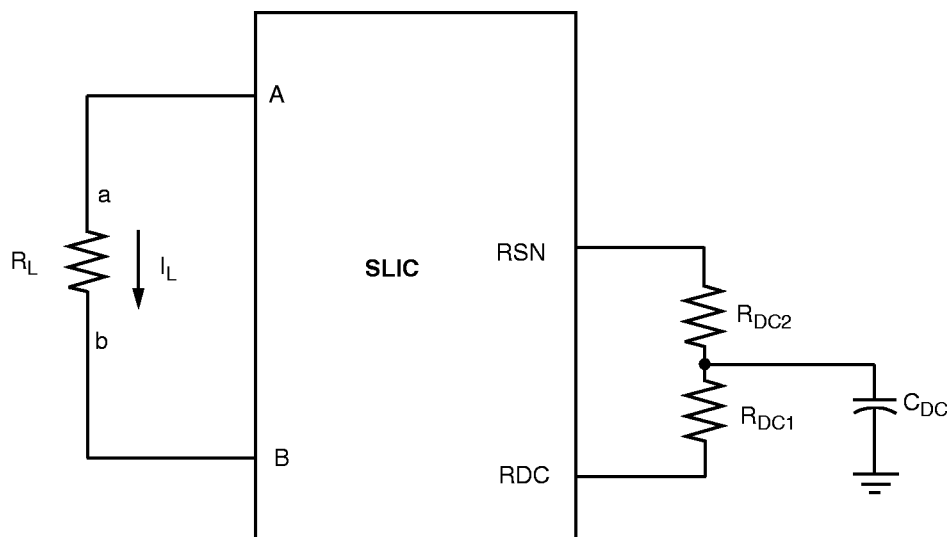
Feed current programmed by R_{DC1} and R_{DC2}

Figure 3. Feed Programming

TEST CIRCUITS

$$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$$
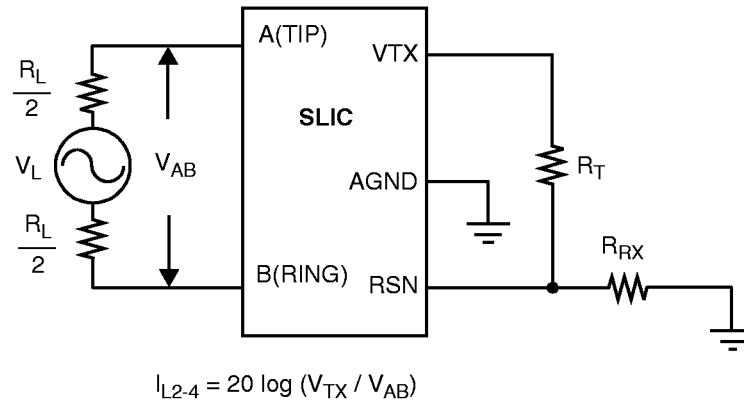
A. Two- to Four-Wire Insertion Loss

$$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$$ $$BRS = 20 \log (V_{TX} / V_{RX})$$
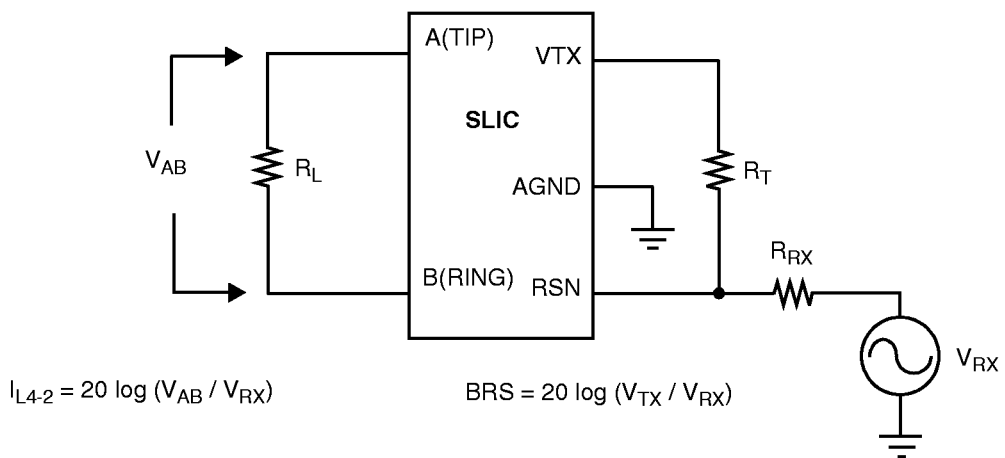
B. Four- to Two-Wire Insertion Loss and Four- to Four-Wire Balance Return Signal

S2 Open, S1 Closed

L-T Long. Bal. $= -20 \log (V_{AB} / V_{L})$

L-4 Long. Bal. $= -20 \log (V_{TX} / V_{L})$

S2 Closed, S1 Open

4-L Long. Sig. Gen. $= 20 \log (V_{L} / V_{RX})$
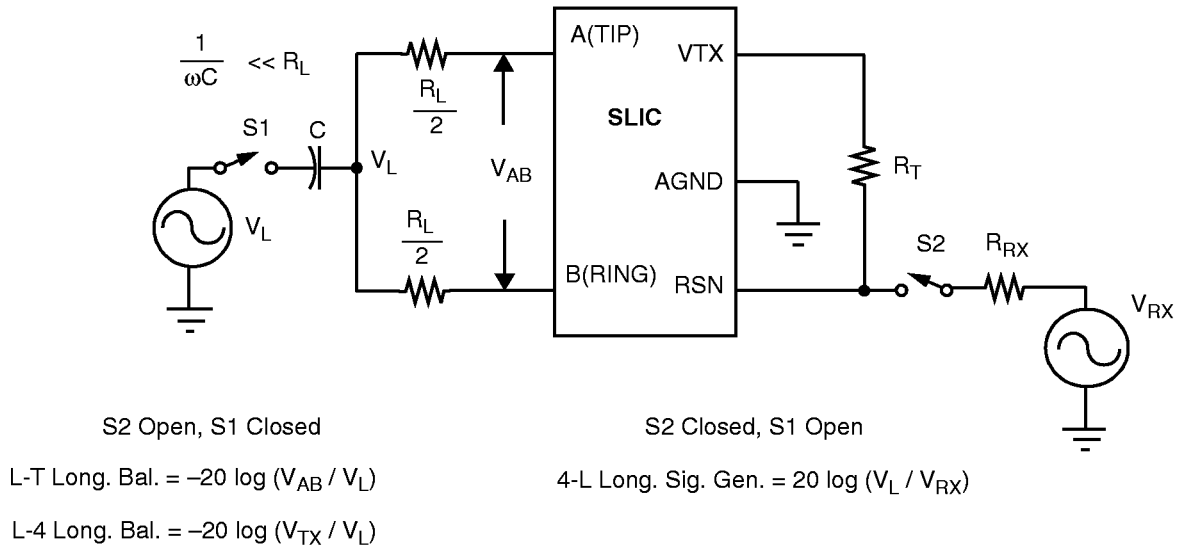
C. Longitudinal Balance

TEST CIRCUITS (continued)
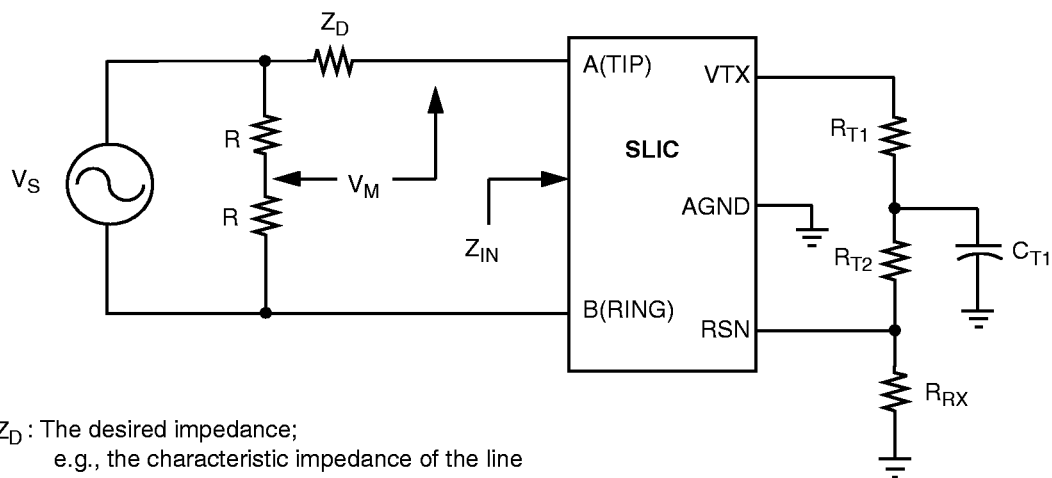
Z_D : The desired impedance;
e.g., the characteristic impedance of the line

$$\text{Return loss} = -20 \log (2\, V_M / V_S)$$

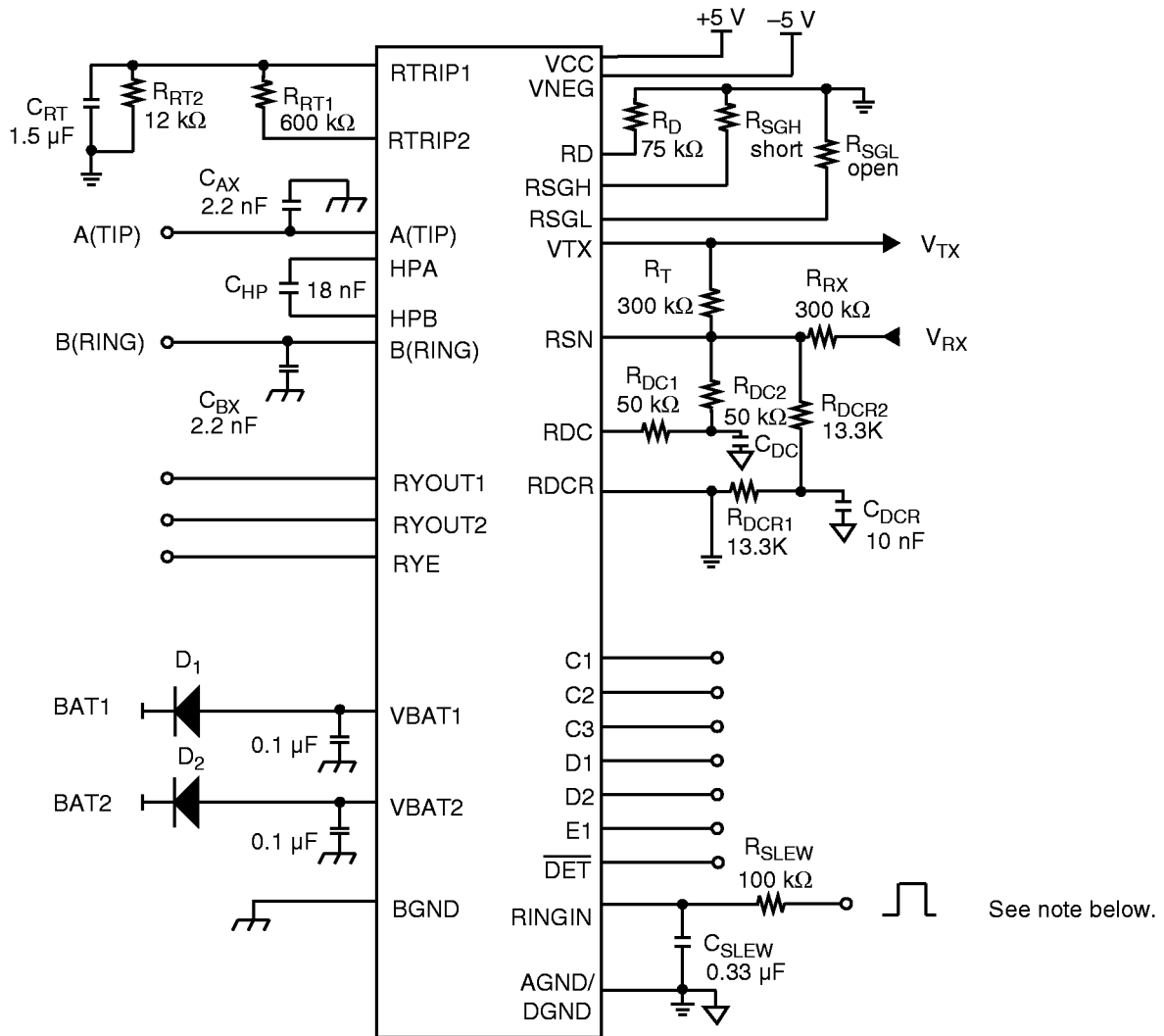**D. Two-Wire Return Loss Test Circuit**
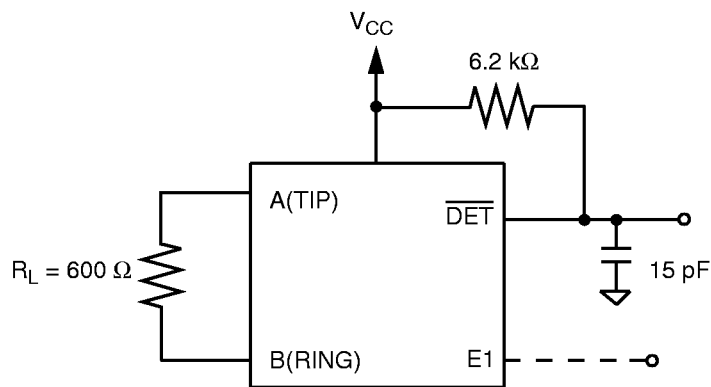
E. Loop-Detector Switching
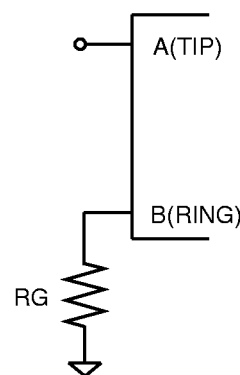
F. Ground-Key Switching
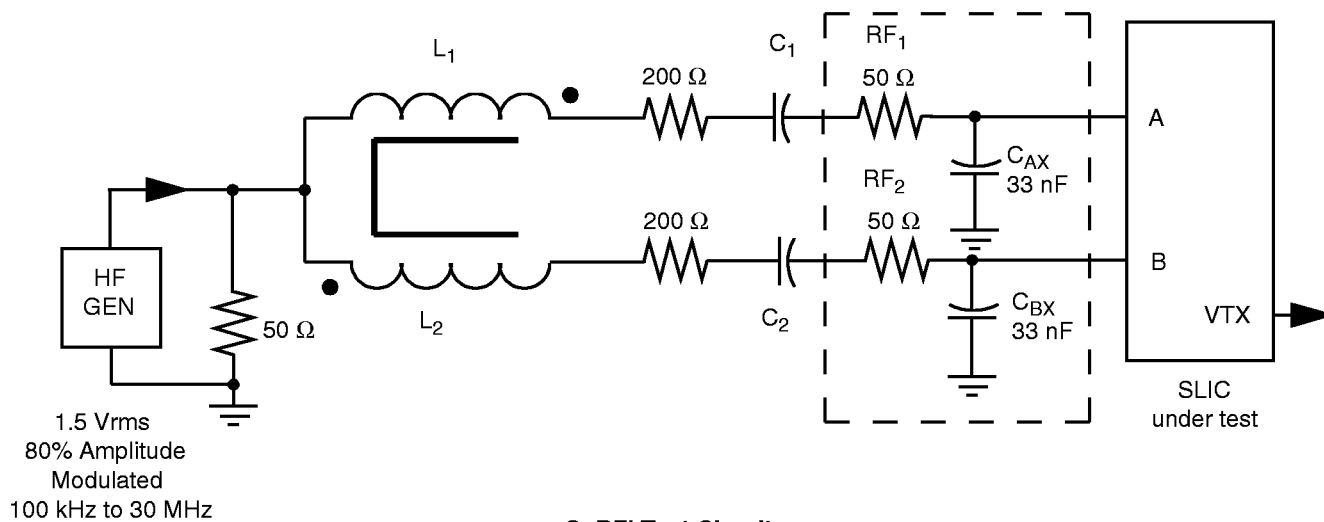
G. RFI Test Circuit

TEST CIRCUITS (continued)

Note:

The input should be 50% duty cycle CMOS-compatible input.
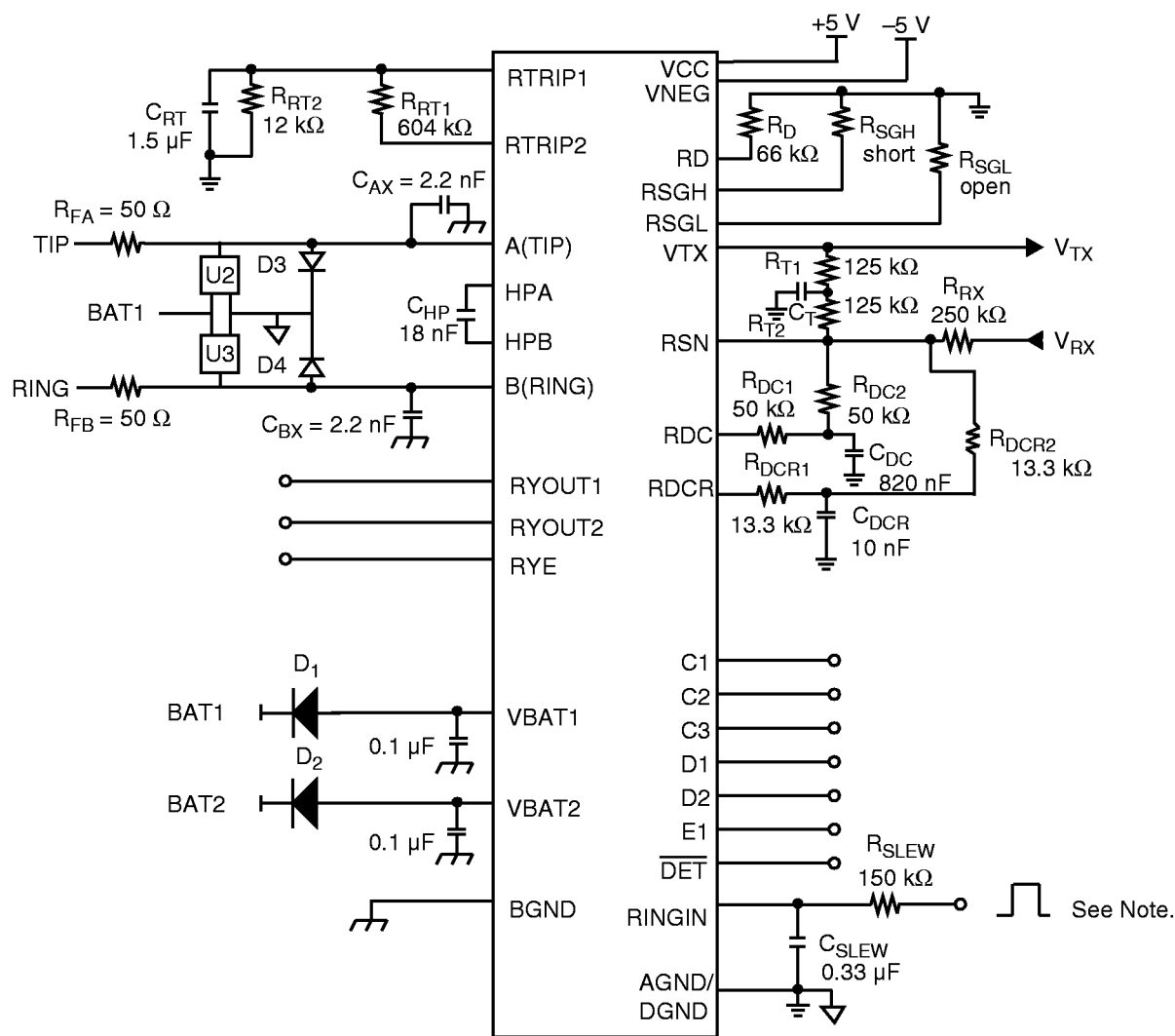
BATTERY
GROUND

ANALOG
GROUND

DIGITAL
GROUND

H. Am79R100 Test Circuit

APPLICATION CIRCUIT

Assumptions:
1. 1.25 CF
2. 25 mA I_{LOOP}
3. 94 mA Ringing Current Limit

4. 5.2 kΩ High Battery Loop Threshold
5. 1100 Ω Ringing Loop Threshold
6. 600 Ω Two-wire Impedance, 600 Ω Z_L

7. $G_{42L} = 1$
8. –95 V BAT1, –24 V BAT2

Note:

The input should be 50% duty cycle CMOS-compatible input.

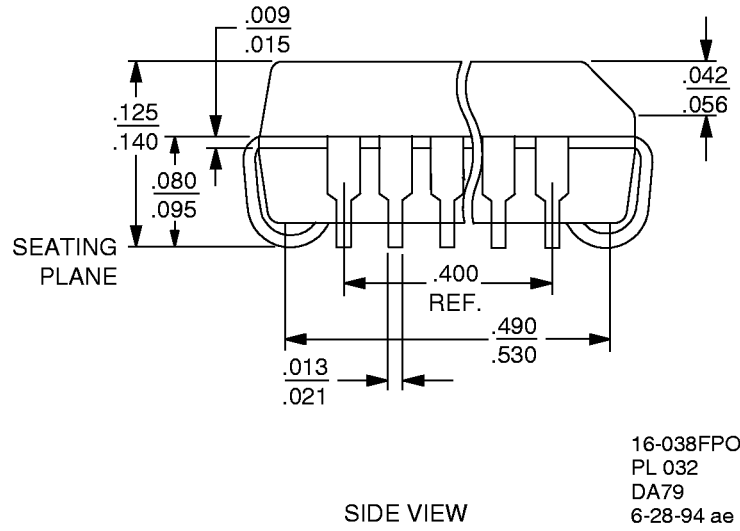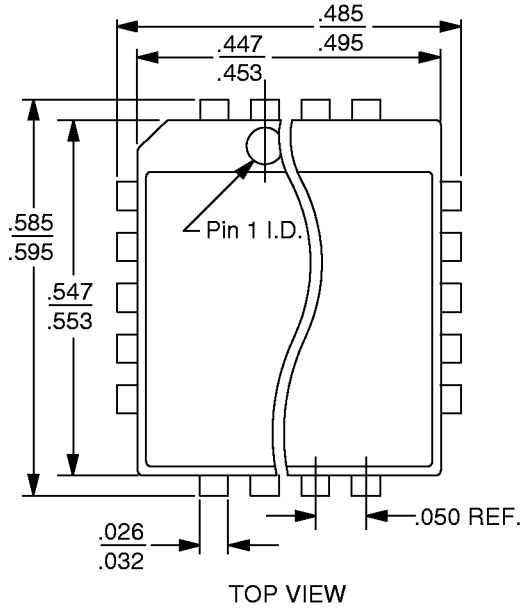*U2, U3 - TECCOR BATTRAX P1001SC protector or TISP61089AD from Power Innovation.*
For battery voltages below 80 V, see Am79R79 for alternate protection.

D3, D4: 1A, 100 V

I. Application Circuit

AMD

PHYSICAL DIMENSION

PL032

.485
.495

.447
.453

Pin 1 I.D.

.585
.595

.547
.553

.026
.032

.050 REF.

TOP VIEW

.009
.015

.125
.140

.080
.095

.042
.056

SEATING
PLANE

.400
REF.

.490
.530

.013
.021

SIDE VIEW

16-038FPO-5
PL 032
DA79
6-28-94 ae