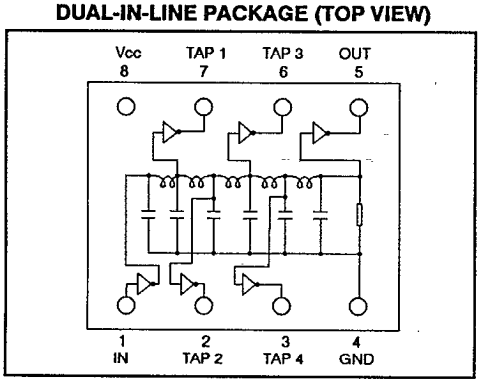
- ❒ **Schottky TTL buffered**
- ❒ **8 pin package**
- ❒ **5 equally spaced taps**
- ❒ **Low profile**
- ❒ **TTL compatible**

DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The 80A series of Digital Delay Modules are Schottky buffered delay lines providing precise delay times and direct compatibility with TTL. Five equally spaced fixed delay taps are packaged in a low profile 8 pin dual-in-line configuration having an industry standard pin-out. Internal termination of the delay line and compensation for propagation delays are incorporated in the design so that no additional external components are required. These modules are very compact and are particularly suitable for high density board designs.
The 80Sseries is the surface mount version which may be vapour phased at temperatures below 218C for durations of up to 2 minutes.

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{cc} 7V
Input voltage 5.5V
Min. pulse width as % of total delay 80%
Input pulse repetition rate PRR . . . . . 3 x pulse width min.
Operating free-air temperature range . . . . . 0C to 70C
Storage temperature range . . . . . -55C to 125C
Temperature coefficient of delay . . . . . ±300ppm/C
Lead temperature 1.5mm from case for 10 seconds 300C

drive capabilities

Logic 0 output . . . . . 10 TTL loads per tap max.
20 TTL loads per unit max.
Logic 1 output . . . . . 20 TTL loads per unit max.

electrical specifications over operating free-air temperature range, Vcc = 5±0.25V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} High-level output voltage	V_{IH} =2V, I_{OH}=–1mA Vcc =4.75V	2.7	3.4		V
V_{OL} Low-level output voltage	Vcc =4.75V I_{OL}=20mA,V_{IL} =0.8V			0.5	V
I_{IH} High-level input current	Vcc=5.25V,V_{IH}=2.7V			50	μA
I_{IL} Low-level input current	Vcc=5.25V, V_{IL}=0.5V			–2	mA
Icc Supply current outputs high	Vcc=5.25V			24	mA
Icc Supply current outputs low	Vcc=5.25V			54	mA

delay characteristics Vcc = 5V, Ta = 25C, no load at taps; input test pulse width 100% of total delay, rise time 3.0ns.

delay tolerance from input to tap ±2ns or ±5% whichever is greater

80A SERIES 5 Tap 8 Pin DIP
Package style A

PART No (1)	TOTAL DELAY (ns) ±5% (2)	TAP TO TAP DELAY (ns)	RISE TIME MAX. (ns)
80A - 5250	25	5 ± 2	4
80A - 5400	40	8 ± 2	4
80A - 5500	50	10 ± 2	4
80A - 5600	60	12 ± 2	4
80A - 5750	75	15 ± 2	4
80A - 5101	100	20 ± 2	4
80A - 5125	125	25 ± 3	4
80A - 5151	150	30 ± 3	4
80A - 5201	200	40 ± 4	4
80A - 5251	250	50 ± 5	4

Note: Delays measured at 1.5V on leading edge, Rise Time measured from 0.75V to 2.4V
(1) Surface mount part No. starts with 80S Package style B
(2) or ±2ns whichever is greater