



Microchip

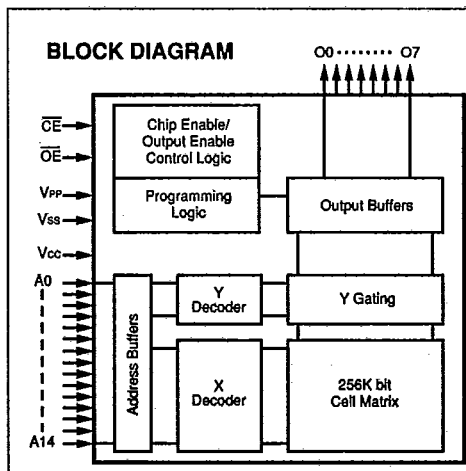
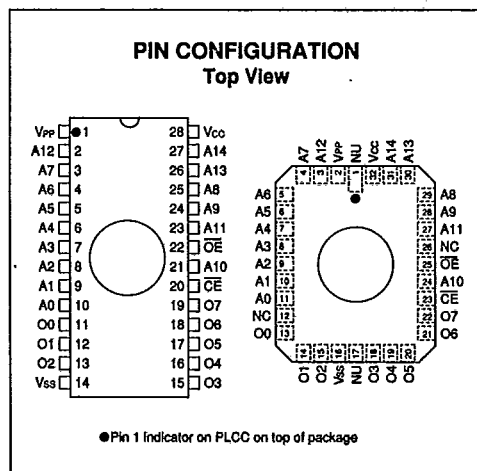
T-46-13-29
27C256**256K (32K x 8) CMOS UV Erasable PROM****FEATURES**

- High speed performance
 - 150ns maximum access time
- CMOS Technology for low power consumption
 - 20mA Active current
 - 100µA Standby current
- OTP (one-time-programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- Two programming algorithms allow improved programming times
 - Fast programming
 - Rapid-pulse programming
- Organized 32K x 8: JEDEC standard pinouts
 - 28-pin Dual-in-line package
 - 32-pin Chip carrier (leadless or plastic)
- Available for extended temperature ranges:
 - Commercial: 0° C to 70° C
 - Industrial: -40° C to 85° C
 - Military (B): -55° C to 125° C

DESCRIPTION

The Microchip Technology Inc 27C256 is a CMOS 256K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 150ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. One Time Programming (OTP) is available for low cost (plastic) applications.



** See 27C256 Military Data sheet DS60013

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PIN FUNCTION TABLE	
Name	Function
A0 - A14	Address Inputs
CE	Chip Enable
OE	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
Vcc	+5V Power Supply
Vss	Ground
NC	No Connection;
	No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS**Maximum Ratings***

Vcc and input voltages w.r.t. Vss -0.6V to +7.25V
 VPP voltage w.r.t. Vss during programming -0.6V to +14.0V
 Voltage on A9 w.r.t. Vss -0.6V to +13.5V
 Output voltage w.r.t. Vss -0.6V to Vcc + 1.0V
 Storage temperature -65° C to 150° C
 Ambient temp. with power applied -65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION DC Characteristics				Vcc = +5V ±10% Commercial: Tamb= 0° C to 70° C Industrial: Tamb= -40° C to 85° C			
Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V _{IH} V _{IL}	2.0 -0.5	Vcc+1 0.8	V V	
Input Leakage	all		I _{LI}	-10	10	μA	V _{IN} = 0 to Vcc
Output Voltages	all	Logic "1" Logic "0"	V _{OH} V _{OL}	2.4	0.45	V V	I _{OH} = -400μA I _{OL} = 2.1mA
Output Leakage	all		I _{LO}	-10	10	μA	V _{OUT} = 0V to Vcc
Input Capacitance	all		C _{IN}		6	pF	V _{IN} = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		C _{OUT}		12	pF	V _{OUT} = 0V; Tamb = 25° C; f = 1MHz
Power Supply Current, Active	S X	TTL input TTL input	I _{CC1} I _{CC2}		20 25	mA mA	Vcc = 5.5V; VPP = Vcc; f = 1MHz; OE = CE = V _{IL} ; I _{OUT} = 0mA; V _{IL} = -0.1 to 0.8 V; V _{IH} = 2.0 to Vcc; Note 1
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	I _{CC(S)}		2 3 100	mA mA μA	CE = Vcc ±0.2V
I _{PP} Read Current VPP Read Voltage	all all	Read Mode Read Mode	I _{PP} VPP	Vcc-0.7	100 Vcc	μA V	VPP = 5.5V Note 2

* Parts: S = Standard Power; X = Industrial Temp Range;

Notes: (1) AC Power component above 1MHz: 5mA up to maximum frequency.

(2) Vcc must be applied before VPP, and be removed simultaneously or after VPP.

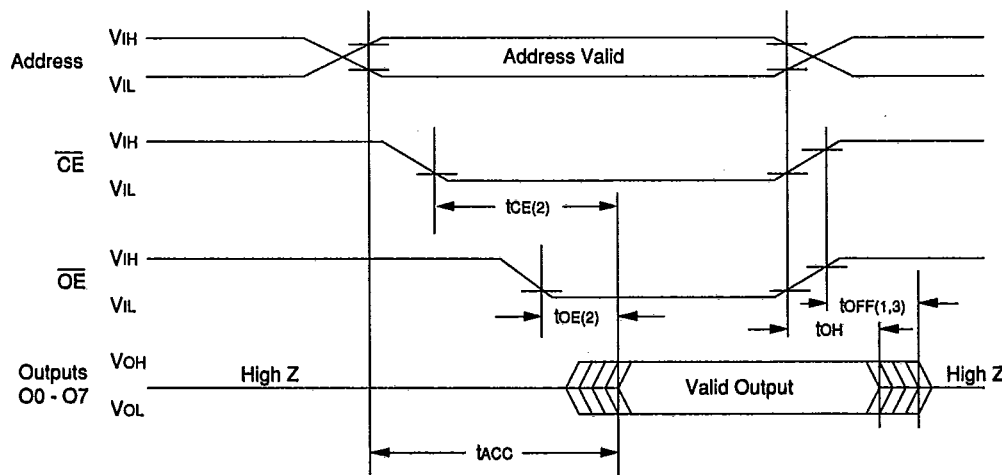
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**READ OPERATION
AC Characteristics**

AC Testing Waveform: $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$; $V_{OH} = 2.0V$ $V_{OL} = 0.8V$
 Output Load: 1 TTL Load + 100pF
 Input Rise and Fall Times: 10nsec
 Ambient Temperature: Commercial: $T_{amb} = 0^{\circ}C$ to $70^{\circ}C$
 Industrial: $T_{amb} = -40^{\circ}C$ to $85^{\circ}C$

Parameter	Sym	27C256-15		27C256-17		27C256-20		27C256-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		170		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		150		170		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}		60		70		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0		0		0		0		ns	

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READ WAVEFORMS

- Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
 (2) $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{OE}
 (3) This parameter is sampled and is not 100% tested.

PROGRAMMING DC Characteristics		Ambient Temperature: Tamb = 25° C ±5° C For VPP and VCC Voltages refer to Programming Algorithms				
Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V _{IH} V _{IL}	2.0 -0.1	V _{CC} +1 0.8	V V	
Input Leakage		I _{LI}	-10	10	μA	V _{IN} = 0V to V _{CC}
Output Voltages	Logic "1" Logic "0"	V _{OH} V _{OL}	2.4	0.45	V V	I _{OH} = -400μA I _{OL} = 2.1mA
VCC Current, program & verify		I _{CC2}		20	mA	Note 1
VPP Current, program		I _{PP2}		25	mA	Note 1
A9 Product Identification		V _H	11.5	12.5	V	

Note: (1) VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

PROGRAMMING

AC Characteristics

for Program, Program Verify
and Program Inhibit Modes

AC Testing Waveform: $V_{IH} = 2.4\text{ V}$ and $V_{IL} = 0.45\text{ V}$; $V_{OH} = 2.0\text{ V}$; $V_{OL} = 0.8\text{ V}$

Output Load: 1 TTL Load + 100 pF

Ambient Temperature: $T_{amb} = 25^{\circ}\text{ C} \pm 5^{\circ}\text{ C}$

For VPP and Vcc Voltages, refer to Programming Algorithms

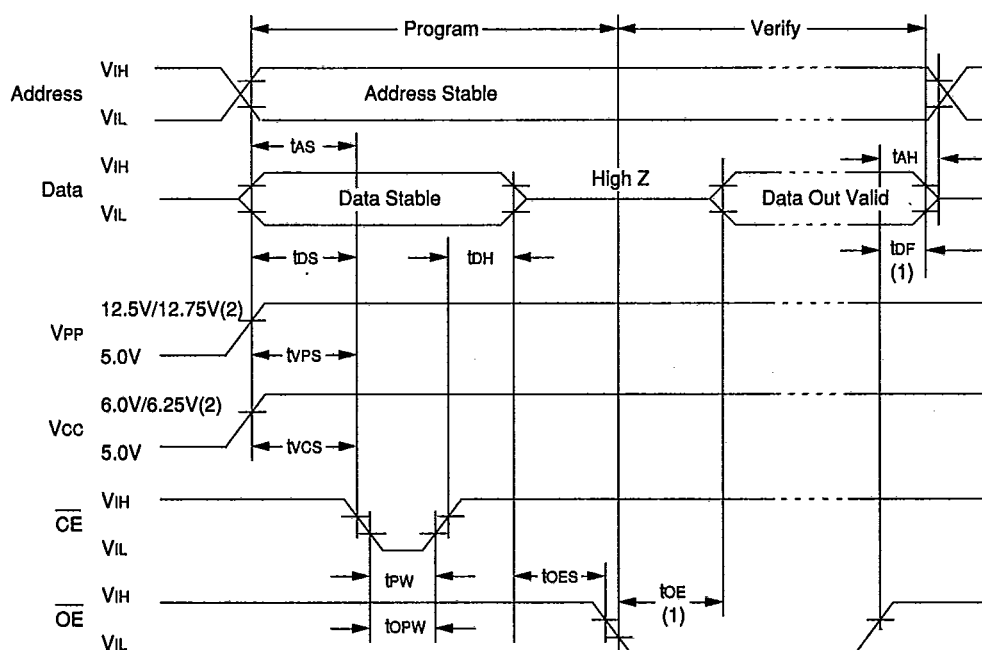
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	tAS	2		μs	
Data Set-Up Time	tDS	2		μs	
Data Hold Time	tDH	2		μs	
Address Hold Time	tAH	0		μs	
Float Delay (3)	tDF	0	130	ns	
Vcc Set-Up Time	tVCS	2		μs	
Program Pulse Width (1)	tPW	0.95	1.05	ms	1ms typical
Program Pulse Width (1)	tPW	95	105	μs	100μs typical
$\overline{\text{OE}}$ Set-Up Time	tCES	2		μs	
$\overline{\text{OE}}$ Set-Up Time	tOES	2		μs	
VPP Set-Up Time	tVPS	2		μs	
Overprogram Pulse Width (2)	tOPW	2.85	78.75	ms	
Data Valid from $\overline{\text{OE}}$	tOE		100	ns	

Notes: (1) For rapid-pulse programming algorithm, initial programming width tolerance is 100μsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1msec ± 5%.

(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75msec as a function of the iteration counter value.

(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

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PROGRAMMING
Waveforms

- Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer
 (2) VCC = 6.0 V $\pm$ 0.25 V, VPP = V_H = 12.5 V $\pm$ 0.50 V for fast programming algorithm
 VCC = 6.25 V $\pm$ 0.25 V, VPP = V_H = 12.75 V $\pm$ 0.25 V for rapid pulse programming algorithm

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	V _{IL}	V _{IL}	VCC	X	DOUT
Program	V _{IL}	V _{IH}	V _H	X	DIN
Program Verify	V _{IH}	V _{IL}	V _H	X	DOUT
Program Inhibit	V _{IH}	V _{IH}	V _H	X	High Z
Standby	V _{IH}	X	VCC	X	High Z
Output Disable	V _{IL}	V _{IH}	VCC	X	High Z
Identity	V _{IL}	V _{IL}	VCC	V _H	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

- the $\overline{CE}$ pin is low to power up (enable) the chip
- the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

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Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these condition are met, the supply current will drop from 20mA to 100 μ A.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and a program is not defined.

Erase Mode

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 μ W/cm² for 20 minutes.

Programming Mode

Two programming algorithms are available. The fast programming algorithm is the industry-standard programming mode that requires both initial programming pulses and overprogramming pulses. A flowchart of the fast programming algorithm is shown in Figure 1.

The rapid-pulse programming algorithm has been developed to improve on the programming throughput times in a production environment. Up to 25 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the rapid-pulse programming algorithm is shown in Figure 2.

Programming takes place when:

- VPP is brought to proper V_H level,
- VCC is brought to proper voltage and
- the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

- VPP is at the proper V_H level,
- VCC is at the proper level,
- the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

Identity Mode

In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL} . A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer Device Type*	V_{IL}	0	0	1	0	1	0	0	1	29
	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

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FIGURE 1 - PROGRAMMING - FAST ALGORITHM

Conditions:

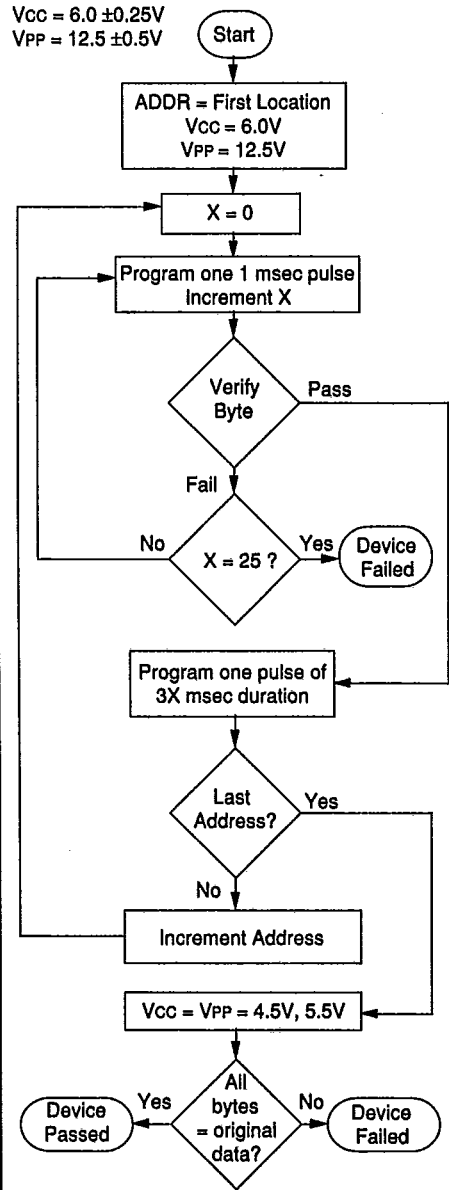
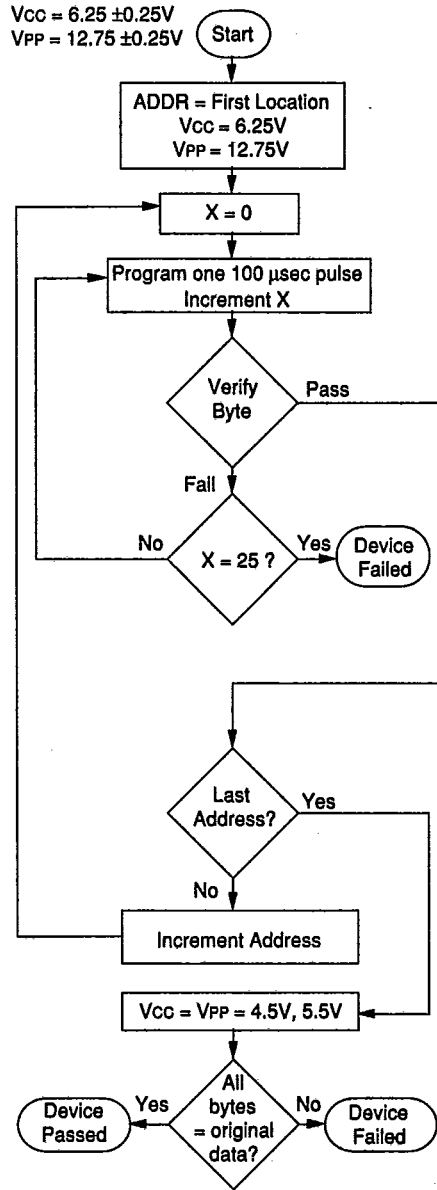
 $T_{amb} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC} = 6.0 \pm 0.25\text{V}$ $V_{PP} = 12.5 \pm 0.5\text{V}$ 

FIGURE 2 - PROGRAMMING - RAPID PULSE ALGORITHM

Conditions:

 $T_{amb} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC} = 6.25 \pm 0.25\text{V}$ $V_{PP} = 12.75 \pm 0.25\text{V}$ 

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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C256 - 25 I/P

Package:

J	CERDIP
K	Ceramic Leadless Chip Carrier
L	Plastic Leaded Chip Carrier (OTP Available)
P	Plastic DIP (OTP Available)
SO	SOIC 28 Pin

Temperature Range:

Blank	0° C to 70° C
I	-40° C to 85° C

Access Time:

15	150 nsec
17	170 nsec
20	200 nsec
25	250 nsec

Device: 27C256 256K (32K x 8) CMOS EPROM