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GigaBit Logic

10G001

Quad 2 Input NOR Gate
320 ps Gate Delay
10G PicoLogic™ Family

2

FEATURES

- 320 ps max propagation delay
- Output rise and fall times of 150 ps
- 0°C to +85°C operating temperature range
- 10G PicoLogic compatible inputs and outputs
- VBB reference voltage for improved threshold tracking over temperature and power supply variation
- On-chip VBBS (-1.3V) threshold reference voltage
- Supports a wide range of load resistor and termination voltage combinations
- Wire-OR output capability
- Available in 40 pin C-leaded or leadless chip carrier, or die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- Logic functions
- Precision gating/strobing
- Data distribution
- Digital multiplexing
- High speed TTL/CMOS to10G/ECL and 10G to TTL/CMOS translation ability

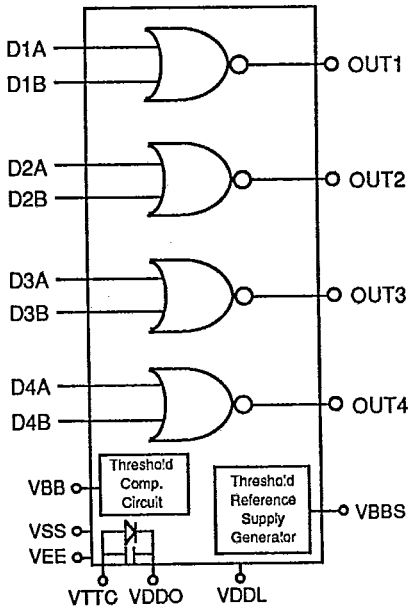
FUNCTIONAL DESCRIPTION

The10G001 is an ultra fast quad 2 input NOR gate featuring a maximum propagation delay of 320 ps for packaged parts. It offers a typical speed four times faster than equivalent ECL NOR gates.

The10G001 is ideally suited for use in high performance systems requiring improved throughput, reduced signal skew and increased timing margin. It can also drive and be driven from CMOS and TTL gates, providing the user a high speed TTL/CMOS to10G/ECL translation capability.

For compatibility with other high speed logic families, the 10G001 features the PicoLogic™ family standard VBB input. This input allows the 10G001's threshold voltage to be controlled by thedriving logic family. Therefore, mismatches in threshold level due to temperature and power supply variations can be compensated, providing high system noise inmunity. An on-chip threshold
voltage ouput (pin VBBS) is also provided. VBBS must be strapped to the VBB input when PicoLogic™ is used to drive the 10G001. The 10G001 has input clamps VICH and VICL. When connected to -1.3V, these internally truncate an overdriven sine wave input signal to a square wave, thus allowing inputs to be driven with faster rise and fall times. When not used, the input clamps should be connected to VICL = VSS and VICH = VDDO for transient protection.

BLOCK DIAGRAM



10G001 ORDERING INFORMATION

PACKAGE TYPE	DELAY (Max @ 25°C)	
	320 ps	390 ps
40 Pin C-Leaded CC	10G001-C	10G001-4C
40 Pin Leadless CC	10G001-L	10G001-4L
Die		10G001-4X

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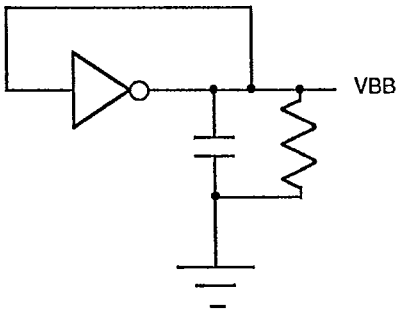
FUNCTIONAL DESCRIPTION (Continued)

A major design goal of the PicoLogic family is to provide full interface capability to other logic families without sacrificing noise immunity. Since each family exhibits differing input threshold sensitivity to temperature and power supply variations, it is necessary to "tell" the PicoLogic device which family it is interfacing to.This can easily be accomplished via the VBB input pin. A nominal -1.3V reference voltage is applied to the VBB pin to cause the PicoLogic threshold to equal and track the threshold of the interfacing logic family.

When the 10G001 is interfaced with other PicoLogic parts, VBB may be strapped to the VBBS output pin. The internal VBBS circuit generates a nominal -1.3V reference output with only a 17% VSS sensitivity. It thus provides a convenient reference supply which can be used over the commercial temperature range of 0°C to + 85°C for a GaAs to GaAs interface.

If VBBS is not supplied by the other logic family, it may be generated by connecting an inverting device output to its input as illustrated below.

Generating the Switching Threshold (VBB) Reference Level from Interfacing Logic.



PIN DESCRIPTIONS

D1-4	Data inputs
OUT1-4	Outputs
VDDO	Output driver ground (0V)
VDDL	Internal logic ground (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 10G001 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the 10G001 die.VTTC is typically equal to VTT (nominally -2.0V).
VDCH	Output driver clamp supply.When VDCH is connected to VTT = -2.0V the output driver high level is limited to approximately -0.6V, thus providing ECL output compatibility. When not used, VDCH should be connected to VDDO.
VICH,VICL	Input protection clamp supply. When connected to -1.3V, these allow an over-driven sine wave input signal to be truncated to a square wave, thus allowing inputs to be driven with faster rise and fall times. When not used, the input clamps should be connected to VICL =VSS and VICH =VDDO for transient protection.
VBB	GaAs threshold reference input voltage. Allows direct tracking of another family's reference voltage. Connect to the VBBS pin for PicoLogic interface. When interfacing to ECL, connect to the reference voltage supply (VBB). This pin may not be left unconnected.
VBBS	GaAs threshold reference voltage. Connect to VBB when interfacing with PicoLogic.

TRUTH TABLE

A	B	OUTPUT
H	X	L
X	H	L
L	L	H

X = Don't care input

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DC CHARACTERISTICS

TC = 0 °C to + 85 °C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input Voltage High	- 0.7		VDDL	V	
VOH	Output Voltage High	-0.7			V	
VIL	Input Voltage Low	VSS		- 1.8	V	
IIN	Input Current	-100	120	400	µA	VIN =-0.7V to -1.8V
ISS	Power Supply Current		110	180	mA	
IEE	Power Supply Current		25	45	mA	
PD	Power Dissipation		500	875	mW	

NOTE: The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides device specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1,3)

10G001

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	235	330	230	300	320	245	350	ps	
T2	Prop. Delay, High to Low	235	330	230	300	320	245	350	ps	
T3	Output Rise Time		175		150	175		190	ps	2
T4	Output Fall Time		175		150	175		190	ps	2

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SYMBOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	265	390	265	360	390	275	410	ps	
T2	Prop. Delay, High to Low	265	390	265	360	390	275	410	ps	
T3	Output Rise Time		215		190	215		230	ps	2
T4	Output Fall Time		215		190	215		230	ps	2

Note 1. Test conditions (unless otherwise indicated) :

VBB = -1.3V VICH = 0V VIH = -0.7V
VTT = -2.0V VICL = VSS VIL = -1.8V
VTTC = VTT VDCH = -2.0V VOH = -0.7V
RLOAD = 50Ω to -2.0V VOL = -1.8V
Input signal rise and fall time ≤ 150 ps

2. Rise and fall times are measured between 20% and 80% points.
3. All values of parameters T1 and T2 are 30 ps less for the "L36" and "F" packages.

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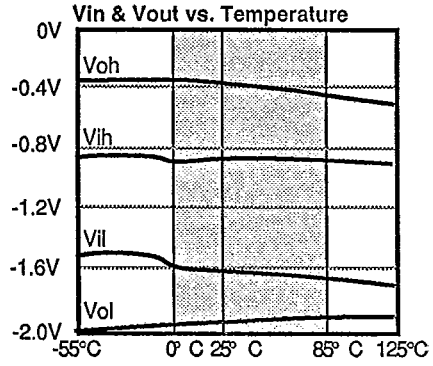
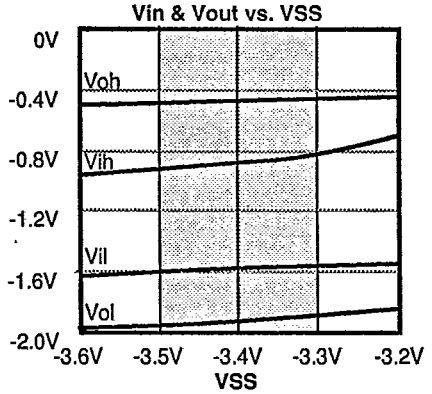
TYPICAL PERFORMANCE CHARACTERISTICS

Vin & Vout vs. Temperature

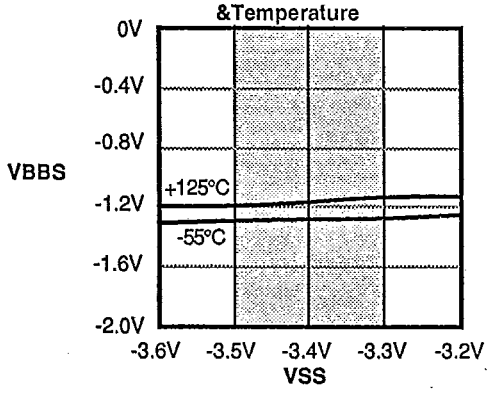


Vin & Vout vs. VSS

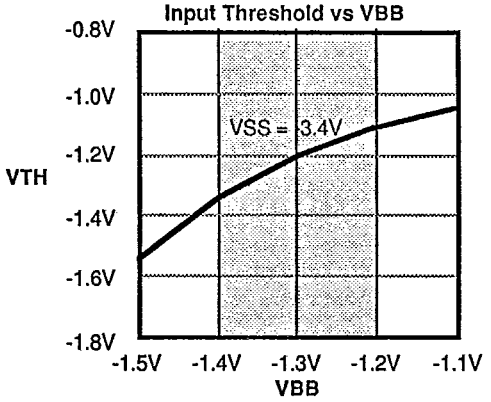


VBB = -1.3V. The VOH and VOL curves result when the inputs are driven from -0.7V to -1.8V. The VIH and VIL curves shown result in output levels from -0.7V to -1.8V.

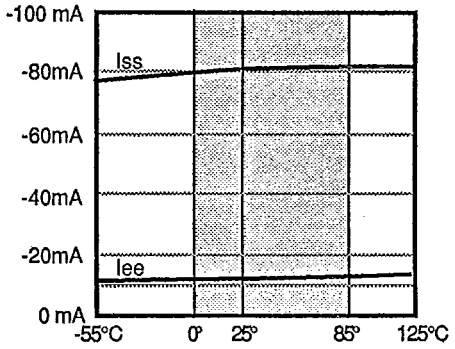
VBBS vs VSS &Temperature



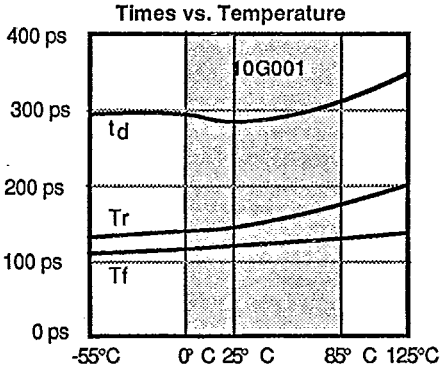
Input Threshold vs VBB



ISS & IEE vs. Temperature



Prop. Delay and Rise and Fall Times vs. Temperature



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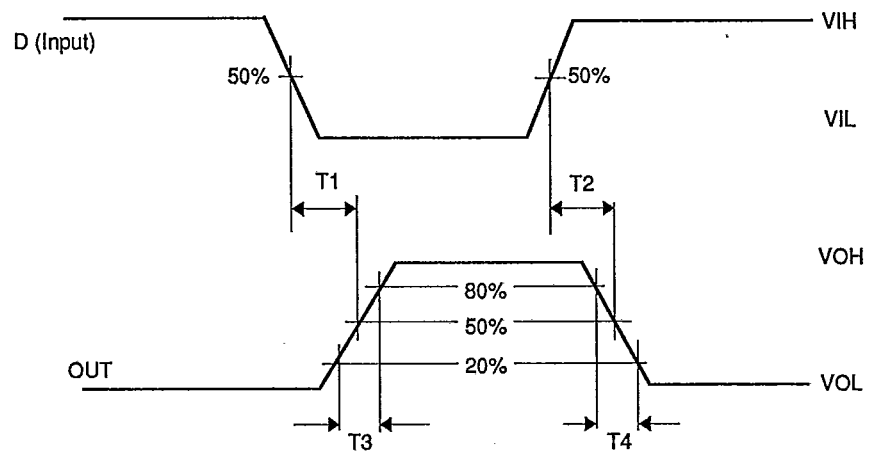
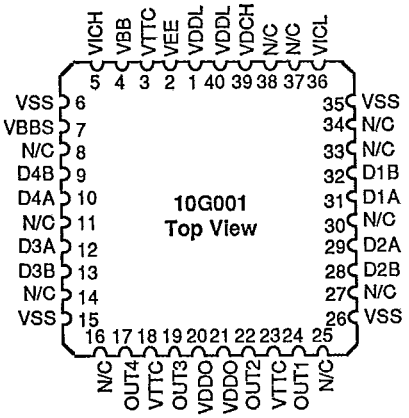
SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



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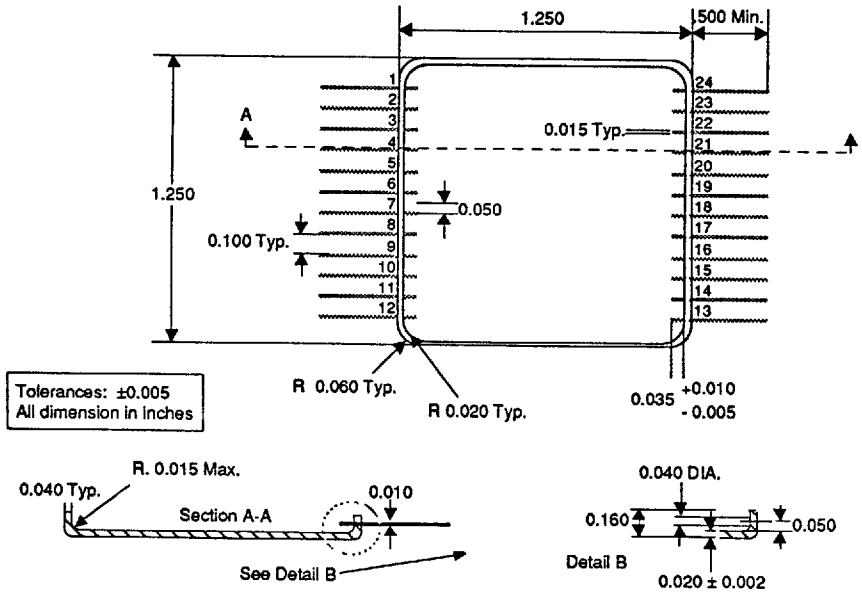
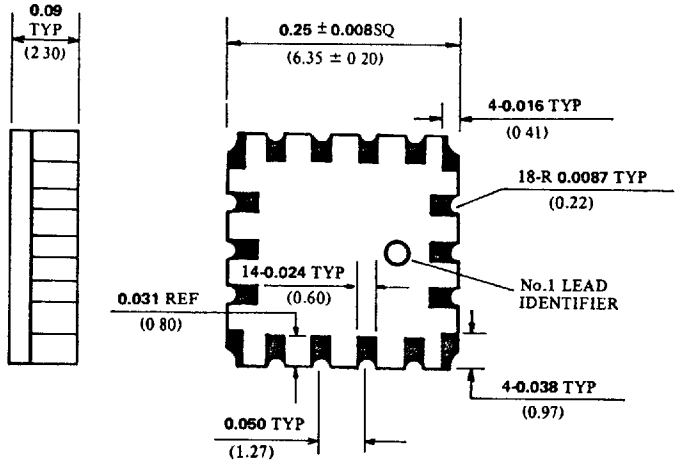
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

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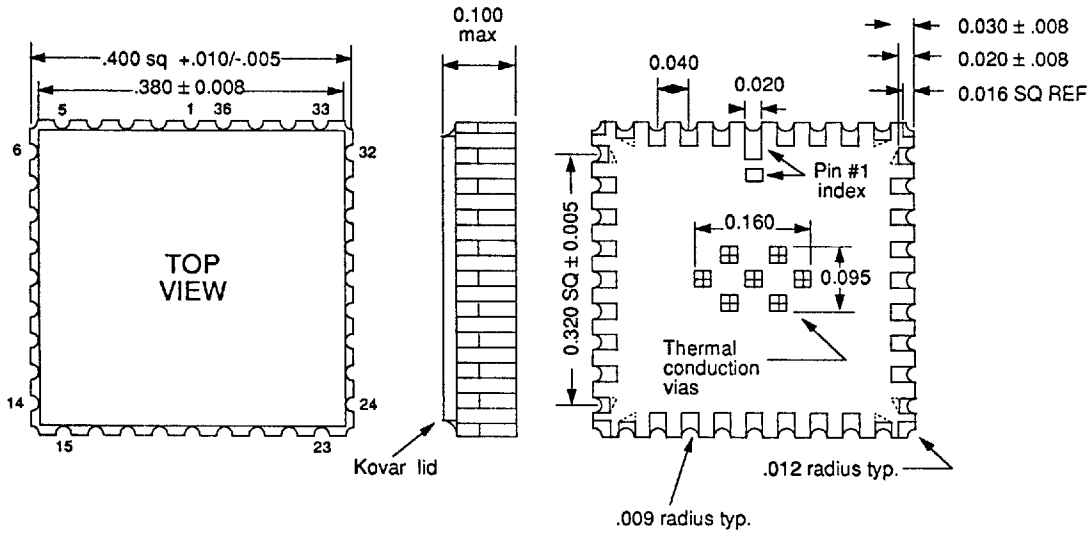
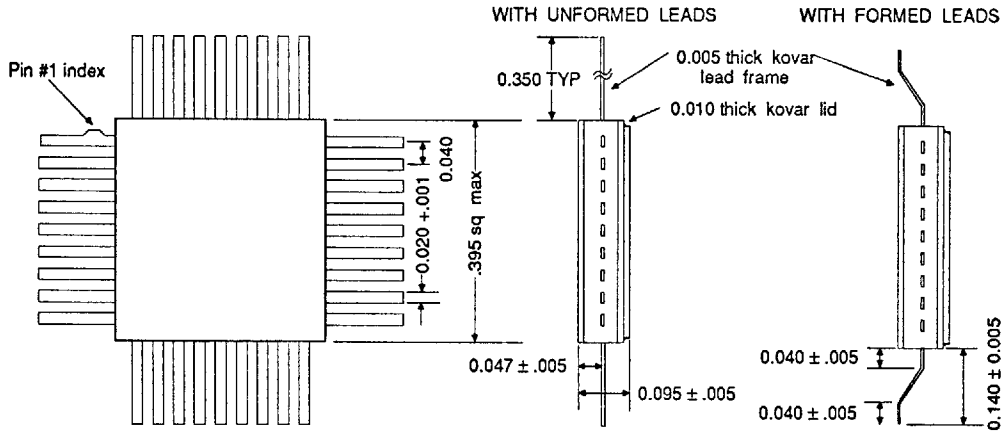
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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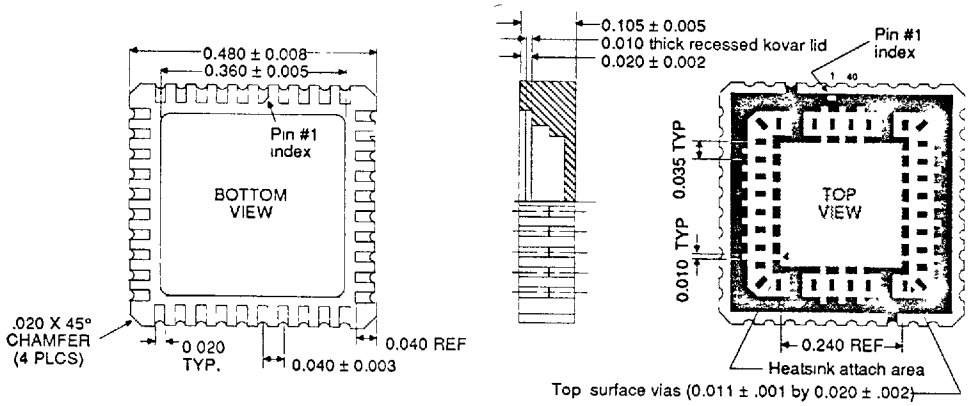
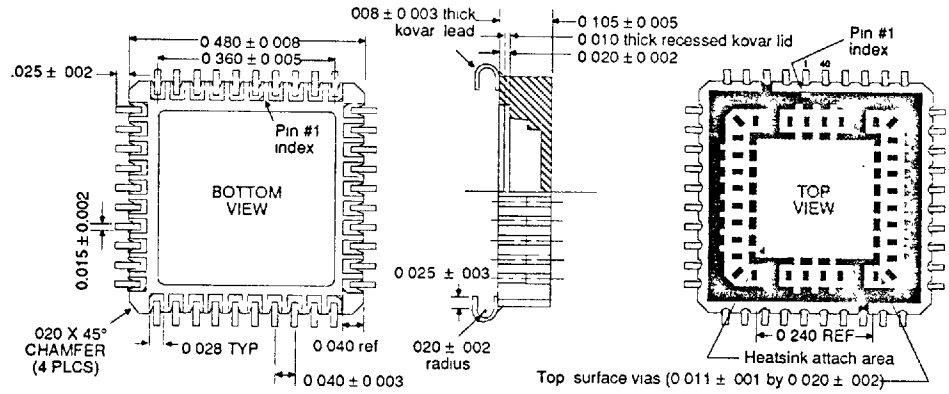
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

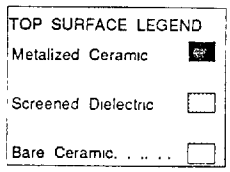


40 PIN LEADED CHIP CARRIER
TYPE C

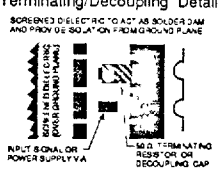


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



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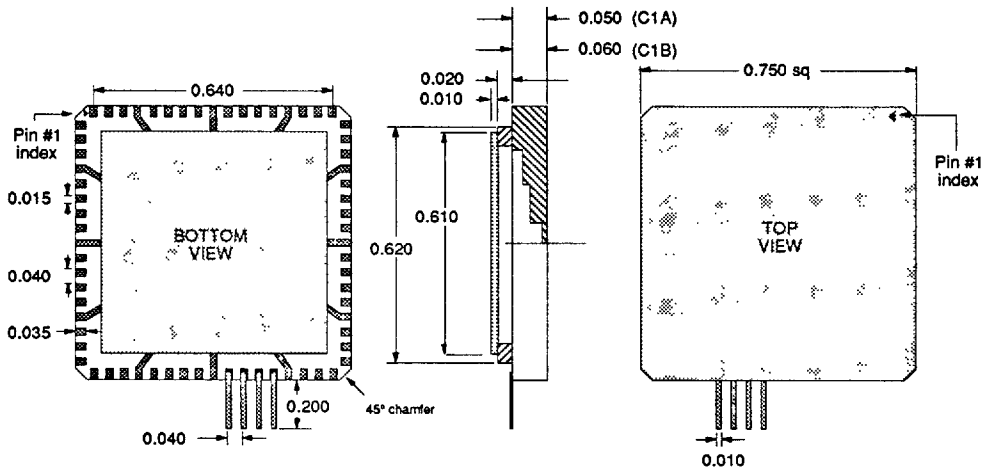
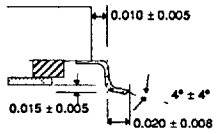
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3