Programmable Peripheral
ZPSD3XX Family
Field-Programmable Microcontroller Peripheral

Key Features

- ❑ Single Chip Zero Power Programmable Peripheral for Microcontroller-based Applications

- ❑ Integrated Power Management
  - — Standby typically 10µA (ZPSD3XX) or 1 µA (ZPSD3XXV)
  - — Extremely low AC power

- ❑ Wide Operating Voltage Range
  - — V-Versions = 2.7 to 5.5 volts
  - — Others = 4.5 to 5.5 volts

- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Zero Power Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS

- ❑ Two Zero Power Programmable Arrays (PAD A and PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Address Decoding up to 1 MB
  - — Logic replacement
  - — Turbo Bit to control speed/power

- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control input

- ❑ 256 Kb, 512 Kb, 1 Mbits, or 2 Mbits of Zero Power UV EPROM (2 Mbit version is SRAMless)
  - — Configurable x8 or x16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — 70 ns EPROM access time, including input latches and PAD address decoding.
  - — Block resolution is from 4K x 8 or 2K x 16 (ZPSD3X1) to 32K x 8 or 16K x 16 (ZPSD3X4R)

- ❑ 16 Kbit Zero Power Static RAM (SRAM)
  - — Configurable as 2K x 8 or as 1K x 16
  - — 70 ns SRAM access time, including input latches and PAD address decoding

- ❑ Power Management
  - — CMiser Bit: Programmable option to reduce AC power consumption
  - — Turbo Bit: Volatile bit set to achieve zero DC power

Key Features (Cont.)

- ❑ Built-in Page Logic (except ZPSD3X1)
  - — Expands the MCU address space up to sixteen 1 Mb pages
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the ZPSD3XX Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC, CLDCC and TQFP
- ❑ Simple Development Software:
  Configure the ZPSD3XX on an IBM PC
- ❑ ZPSD3XX standard versions are ideal for general purpose applications
- ❑ ZPSD3XXR RAMless versions result in lower cost
- ❑ ZPSD3XXV versions (2.7 to 5.5 volt operation) are excellent for very low power applications, they eliminate mixing and matching discrete low-voltage parts
- ❑ ZPSD3XXM mask-programmable versions are ideal for code-stable, high-volume low cost applications

ZPSD3XX Family Feature Summary

Part	Zero Power PLD Inputs/ Product Terms	Ports	Zero Power EPROM Size	Zero Power SRAM Size	Configuration	Memory Paging	C-Miser and ZPLD Turbo Bit	Security Bit
ZPSD301	14/40	19	256 Kb	16 Kb	x8 or x16		X	X
ZPSD311	14/40	19	256 Kb	16 Kb	x8		X	X
ZPSD302	18/40	19	512 Kb	16 Kb	x8 or x16	X	X	X
ZPSD312	18/40	19	512 Kb	16 Kb	x8	X	X	X
ZPSD303	18/40	19	1 Mb	16 Kb	x8 or x16	X	X	X
ZPSD313	18/40	19	1 Mb	16 Kb	x8	X	X	X
ZPSD304R	18/40	19	2 Mb	–	x8 or x16	X	X	X
ZPSD314R	18/40	19	2 Mb	–	x8	X	X	X

Partial Listing of Microcontrollers Supported

- **Motorola family:**
  M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- **Intel family:**
  8031/8051, 8096/8098, 80186/88, 80196/98, 386EX
- **Philips Semiconductors:**
  SC80C451, SC80552
- **TI:**
  SC80C451, TMS320C14
- **Zilog:**
  Z8, Z80, Z180
- **National:**
  HPC16000, HPC46400
- **Echelon:**
  NEURON® 3150™ Chip

Applications

- Computers (Notebook and Portable PCs)
  — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- Telecommunications
  — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- Portable Industrial Equipment
  — Measurement Meters, Data Recorders
- Medical Instrumentation
  — Hearing Aids, Monitoring Equipment, Diagnostic Tools

Introduction

The ZPSD3XX family is the market's first very low power single chip solution for microcontroller-based applications where fast time-to-market, small form factor, and low power consumption are essential criteria. When combined in an 8- or 16-bit system, virtually any microcontroller (68HC11, 8051, 80186, etc.) and the ZPSD3XX device work together to create a very powerful chip-set solution. The low voltage ZPSD3XXV versions eliminate mixing and matching various discrete component low voltage specifications. They also provide all the required control and peripheral elements needed in a microcontroller-based system with no external discrete "glue" logic required.

The ZPSD3XX family comes complete with simple software development tools for interfacing the ZPSD3XX to a microcontroller. Hosted on IBM PC platforms or compatibles, the easy-to-use PSDsoft software enables the designer to quickly configure the device and use it immediately.

The ZPSD3XX standard versions include EPROM, SRAM and features described in this data sheet. They are ideal for general purpose embedded systems applications.

The ZPSD3XXR RAM-less versions are excellent for designs that require no on-chip SRAM or require large off-chip SRAMs for data storage.

The ZPSD3XXV low voltage, low-power versions operate down to 2.7 volts and feature standby current of only 1 µA typical (at 3.0 volts).

The ZPSD3XXM mask-programmable versions deliver the lowest cost ZPSD3XX solution. See the Masked-PSD Ordering Information chapter in this databook for the mask-programmable ZPSD3XXM ordering procedure.

References in this document to ZPSD3XX versions include any "Non-V" products (ZPSD3XX, ZPSD3XXR, ZPSD3XXM, and ZPSD3XXRM). References to ZPSD3XXR include any RAM-less product (ZPSD3XXR, ZPSD3XXRM, ZPSD3XXRV, ZPSD3XXRVM). References to ZPSD3XXV include ZPSD3XXV, ZPSD3XXVM, ZPSD3XXRV and ZPSD3XXRVM. References to ZPSD3XXM includes ZPSD3XXM, ZPSD3XXRM, ZPSD3XXVM and ZPSD3XXRVM.

ZPSD Background

Portable and battery powered systems have recently become major embedded control application segments. As a result, the demand for electronic components having extremely low power consumption has increased dramatically. Recognizing this need, WSI, Inc. has developed a new ZPSD (Zero Power PSD) technology. ZPSD products virtually eliminate the DC component of power consumption reducing it to standby levels. Eliminating the DC component is the basis for the words "Zero Power" in the ZPSD name. ZPSD products also minimize the AC power component when the chip is changing states. The result is a programmable microcontroller peripheral family that replaces at least six discrete circuit functions while drawing much less power than a single EPROM.

Integrated Power Management™ Operation

Upon each address or logic input change to the ZPSD, the device powers up from low power standby for a short time. Then the ZPSD consumes only the necessary power to deliver new logic or memory data to its outputs as a response to the input change. After the new outputs are stable, the ZPSD latches them and automatically reverts back to standby mode. The I_{CC} current flowing during standby mode and during DC operation is identical and is only a few microamperes.

The ZPSD automatically reduces its DC current drain to these low levels and does not require controlling by the CSI (Chip Select) input. Disabling the CSI pin unconditionally forces the ZPSD to standby mode independent of other input transitions.

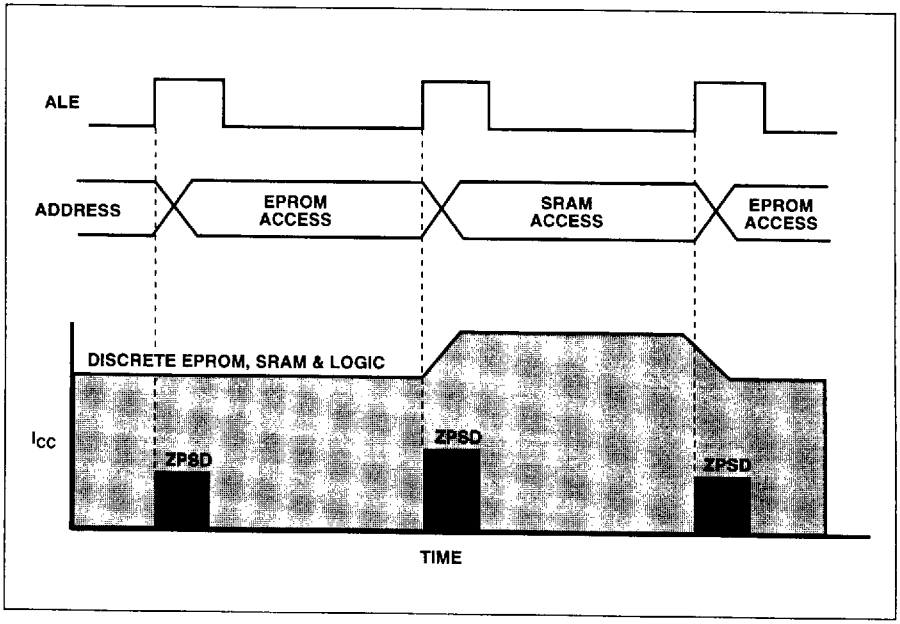
The only significant power consumption in the ZPSD occurs during AC operation.

The ZPSD contains the first architecture to apply zero power techniques to memory circuit blocks as well as logic.

Figure 1 compares ZPSD zero power operation to the operation of a discrete solution. A standard microcontroller (MCU) bus cycle usually starts with an ALE (or AS) pulse and the generation of an address. The ZPSD detects the address transition and powers up for a short time. The ZPSD then latches the outputs of the PAD, EPROM and SRAM to the new values. After finishing these operations, the ZPSD shuts off its internal power, entering standby mode. The time taken for the entire cycle is less than the ZPSD's "access time."

The ZPSD will stay in standby mode if the address does not change between bus cycles (for example, looping on a single address or a Halt operation). In an alternate system implementation using discrete EPROM, SRAM and other discrete components, the system will consume operating power during the entire bus cycle. This is because the chip select inputs on the memory devices are usually active throughout the entire cycle. The AC power consumption of the ZPSD may be calculated using the ALE frequency.

Figure 1. ZPSD Power Operation vs. Discrete Implementation



Product Description

The ZPSD3XX family integrates high performance user-configurable zero-power blocks of EPROM, SRAM, and zero-power programmable logic. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 256K to 2Mbit of EPROM, 16K bits of SRAM, input latches, and output ports. The ZPSD3XX family is ideal for applications requiring very low power and very small form factors. These include hard disk control, wireless or mobile products, modems, cellular telephones, instrumentation, computer peripherals, military and similar applications.

The ZPSD3XX family offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.
- ❑ Expanded microcontroller address space.

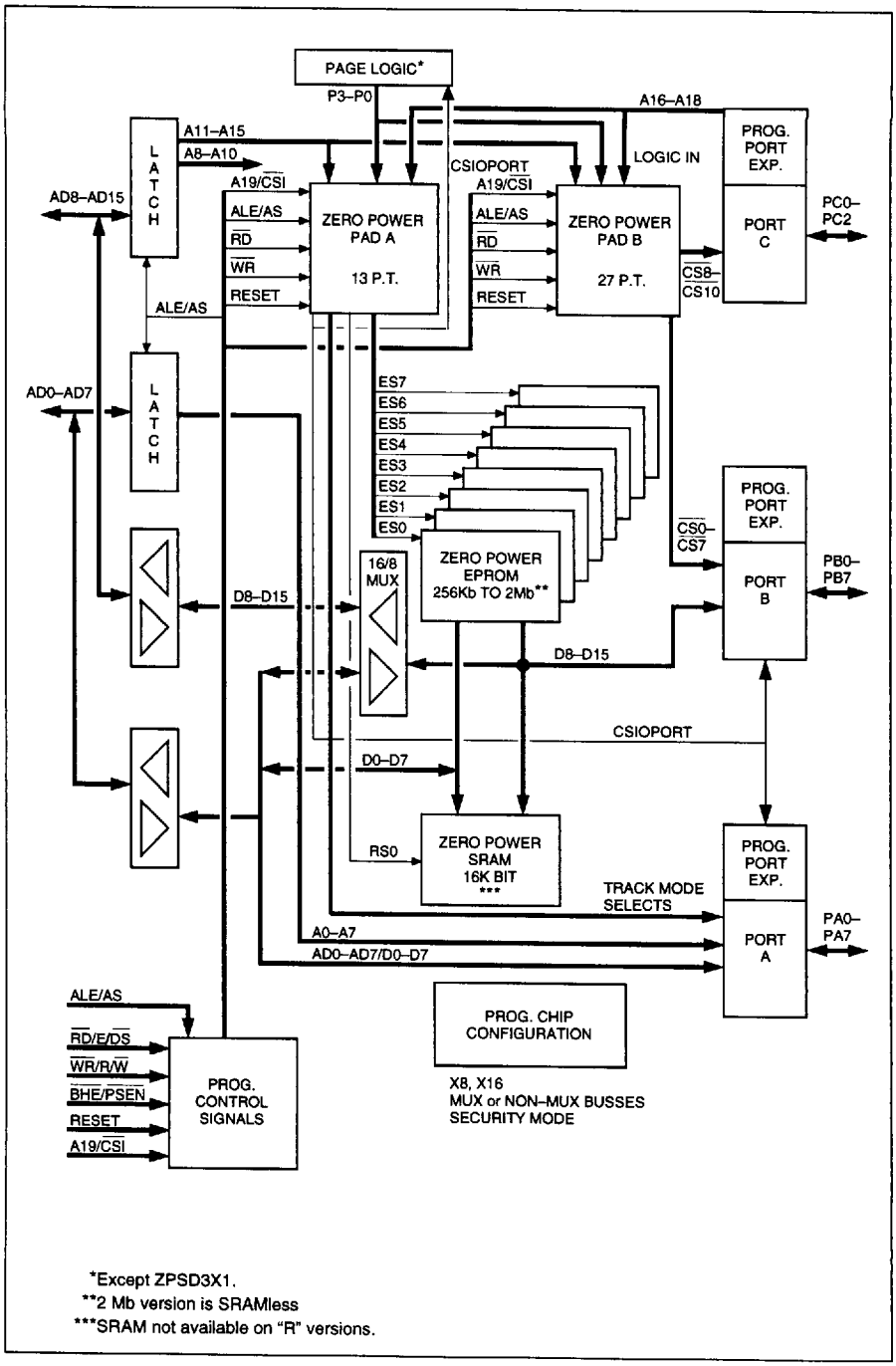
WSI's ZPSD3XX Family Architecture (Figure 2) can efficiently interface with, and enhance, any low-voltage 8- or 16-bit microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays (PAD A and PAD B), an interface to shared resources, 256K, 512K, 1M or 2M bit EPROM, and 16K bit SRAM on a single chip. The ZPSD3XX family does not require any glue logic for interfacing to any 8- or 16-bit microcontroller.

The 8051 microcontroller family can take full advantage of the ZPSD3XX's separate program and data address spaces. Users of the 68HCXX microcontroller family can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and DS signals. (Users of 16-bit microcontrollers, including the 80186, 8096, 80196 and 16XXX, can use the ZPSD301/302/303/304R in a 16-bit configuration). Address and data buses can be configured as separate or multiplexed, whichever is required by the host processor.

The flexibility of the ZPSD3XX I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The page register extends the accessible address space of certain microcontrollers from 64 K to 1 M. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of 16 address line microcontrollers by a factor of 16.

Figure 2. ZPSD3XX Family Architecture



*Except ZPSD3X1.
**2 Mb version is SRAMless
***SRAM not available on "R" versions.

Table 1. ZPSD3XX Pin Descriptions

Name	Type	Description
$\overline{BHE}/\overline{PSEN}$ (ZPSD30X Devices)	I	When the data bus width is 8 bits (CDATA = 0), this pin is $\overline{PSEN}$. In this mode, $\overline{PSEN}$ is the active low EPROM read pulse. The ZSRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ and $\overline{RD}/E/\overline{DS}$ pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, PSEN should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the ZSRAM, I/O ports, and EPROM. When the data bus width is configured as 16 (CDATA = 1), this pin is $\overline{BHE}$. When $\overline{BHE}$ is low, data bus bits D8–D15 are read from or written into the ZPSD3XX depending on the operation being read or write, respectively. In programming mode, this pin is pulsed between V_{PP} and 0.
or $\overline{PSEN}$ (ZPSD31X Devices Only)	I	The $\overline{PSEN}$ is the active low EPROM read pulse. The ZSRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{RD}$/E pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the correspondinbg host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, $\overline{PSEN}$ should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the ZSRAM, I/O ports, and EPROM.
$\overline{WR}/V_{PP}$ or R/$\overline{W}$/V_{PP}	I	In the operating mode this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1). When configured as R/$\overline{W}$, the following tables summarize the read and write operations (CRRWR = 1): CEDS = 0: R/$\overline{W}$ = X, E = 0, NOP; R/$\overline{W}$ = 0, E = 1, write; R/$\overline{W}$ = 1, E = 1, read CEDS = 1 (Note 2): R/$\overline{W}$ = X, $\overline{DS}$ = 1, NOP; R/$\overline{W}$ = 0, $\overline{DS}$ = 0, write; R/$\overline{W}$ = 1, $\overline{DS}$ = 0, read When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}/E/\overline{DS}$ (Note 2)	I	The pin function depends on the CRRWR and CEDS configuration bits. If CRRWR = 0, $\overline{RD}$ is an active low read pulse. When CRRWR = 1, this pin and the R/$\overline{W}$ pin define the following cycle type: If CEDS = 0, E is an active high strobe. If CEDS = 1, $\overline{DS}$ is an active low strobe.
or $\overline{RD}$/E (Note 3)	I	When configured as $\overline{RD}$ (CRRWR = 0), this pin provides an active low $\overline{RD}$ strobe. When configured as E (CRRWR = 1), this pin becomes an active high pulse, which, together with R/$\overline{W}$ defines the cycle type. Then, if R/$\overline{W}$ = 1 and E = 1, a read operation is executed. If R/$\overline{W}$ = 0 and E = 1, a write operation is executed.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.
2. ZPSD3X2/3X3/3X4R only.
3. ZPSD3X1 only.

Table 1. ZPSD3XX Pin Descriptions (Cont.)

Name	Type	Description
A19/$\overline{CSI}$	I	This pin has two configurations. When it is $\overline{CSI}$ (A19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 12 and 13 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (A19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 (CATD = 1 for ZPSD3X1) defines the pin as an address; CADLOG3 = 0 (CATD = 0 for ZPSD3X1) defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET*	I	The user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 10a, 10b and 11 for the chip state after reset.
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0 and A16–A19 in 16-bit mode (AD7/A7–AD0/A0 and A16–A19 in 8-bit mode) and $\overline{BHE}$, depending on the ZPSD3XX configuration. See Table 8. In the non-multiplexed modes (ZPSD3X2/3X3/3X4R), it can be used as a general-purpose logic input to the PAD.
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRAT = 0), the port becomes the data bus lines (D0–D7). See Figure 5.
PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$–$\overline{CS7}$ then are each a function of up to two product terms. On the ZPSD301/302/303/3X4R, when the chip is in non-multiplexed mode (CADDRAT = 0) and the data bus width is 16 (CDATA = 1), the port becomes the data bus (D8–D15). See Figure 7.

*Reset is active low (only) on ZPSD3XXV versions.

Table 1. ZPSD3XX Pin Descriptions (Cont.)

Name	Type	Description
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD A and B input or output. When configured as an input (CPCF = 0), a bit individually becomes an address (CADLOG = 1 for ZPSD3X2/3X3/3X4R, CATD = 1 for ZPSD3X1) or a logic input (CADLOG = 0 for ZPSD3X2/3X3/3X4R, CATD = 0 for ZPSD3X1). The addresses can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PADs (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 8.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E ($\overline{RD}$/E/$\overline{DS}$ on the ZPSD302/312/303/313/304R/314R), $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{BHE}/\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.
AD8/A8 AD9/A9 AD10/A10 AD11/A11 AD12/A12 AD13/A13 AD14/A14 AD15/A15	I/O	In 16-bit multiplexed mode, these pins are the multiplexed high-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{BHE}/\overline{PSEN}$ pins. In all other modes, these pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The ZPSD3XX's four operating modes enable it to interface directly to 8- and 16-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are:

- ❑ Multiplexed 8-bit address/data bus
- ❑ Multiplexed 16-bit address/data bus (ZPSD30X)
- ❑ Non-multiplexed address/data, 8-bit data bus
- ❑ Non-multiplexed 16-bit address/data bus (ZPSD30X)

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$ pin, $\overline{BHE}$/$\overline{PSEN}$ or $\overline{PSEN}$ pin and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Multiplexed 16-bit Address/Data Bus

This mode is used to interface to microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) is bi-directional and permits latching of the high-order address when the ALE signal is active on the same pins. The high-order data bus is read from or written to the device, depending on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

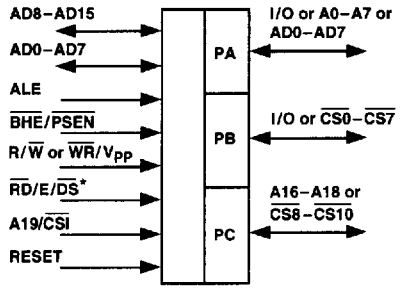
This mode is used to interface to non-multiplexed 8-bit microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) (A8–A15 on the ZPSD31X) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Non-Multiplexed Address/Data, 16-bit Data Bus

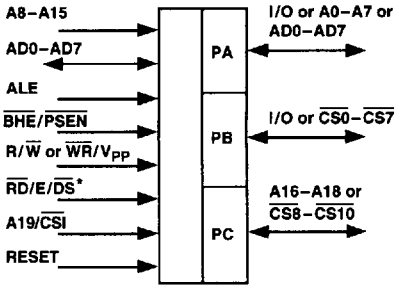
This mode is used to interface to non-multiplexed 16-bit microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B is the high-order data bus.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

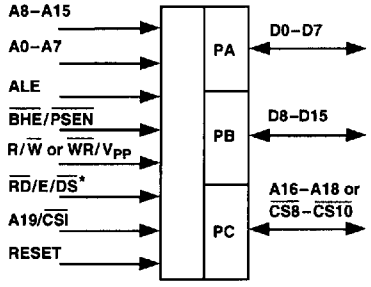
Figure 3a. ZPSD30X Port Configurations (x8/x16)



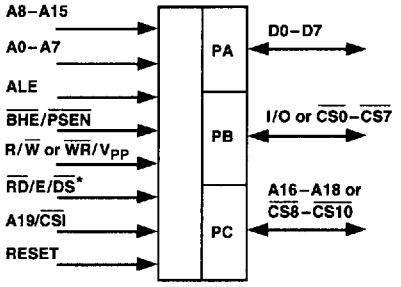
1. Configured for multiplexed 16-bit address/data bus.



2. Configured for multiplexed 8-bit address/data bus.

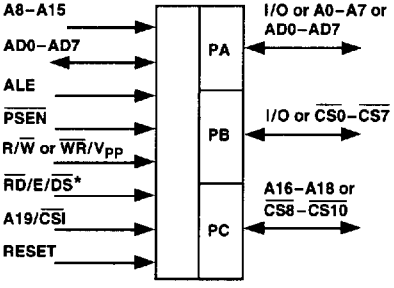


3. Configured for non-multiplexed 16-bit address/data bus.

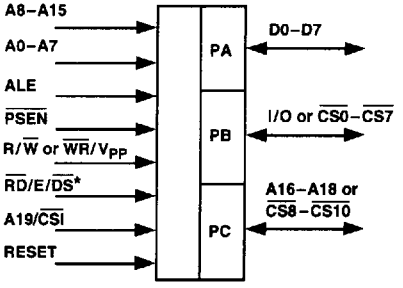


4. Configured for non-multiplexed 8-bit address/data bus.

Figure 3b. ZPSD31X Port Configurations (x8 Only)



1. Configured for multiplexed 8-bit address/data bus.



2. Configured for non-multiplexed 8-bit address/data bus.

Legend: AD8–AD15 = Addresses A8–A15 multiplexed with data lines D8–D15.
AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.
* = $\overline{DS}$ is available on ZPSD3X2/3X3/3X4R only.

Table 2. ZPSD30X Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O and/or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order address bus byte	High-order address bus byte
16-bit Data Bus		
Port A	I/O or low-order address lines or low-order multiplexed address/data byte	Low-order data bus byte
Port B	I/O and/or $\overline{CS0}$–$\overline{CS7}$	High-order data bus byte
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address/data byte	High-order address bus byte

Table 2a. ZPSD31X Bus and Port Configuration Options

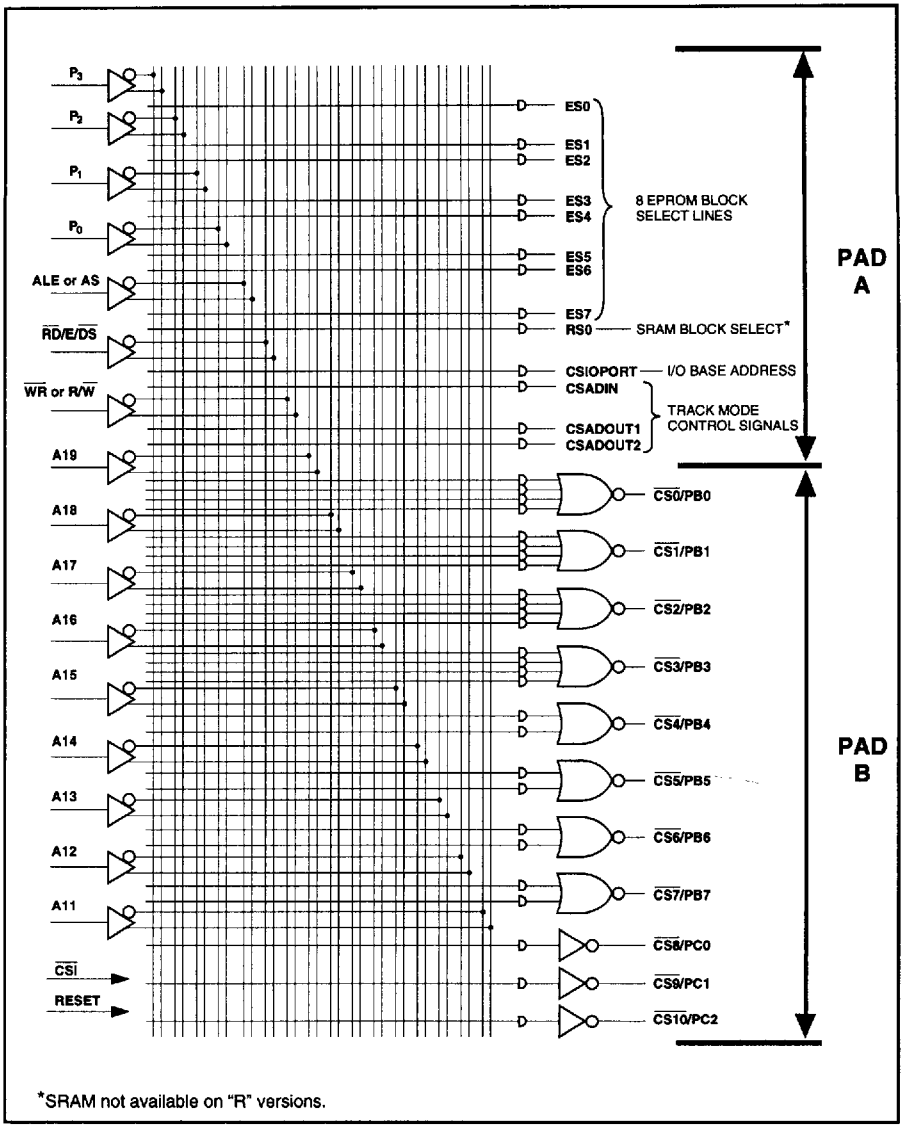
	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O and/or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
A8–A15	High-order address bus byte	High-order address bus byte

Zero Power Programmable Address Decoder (PAD)

The ZPSD3XX consists of two zero power programmable arrays referred to as PAD A and PAD B (Figure 4). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 4. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's development software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 4. PAD Description



*SRAM not available on "R" versions.

NOTES: 4. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 12 and 13.

5. RESET deselects all PAD output signals. See Tables 10 and 11.
6. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.
7. P_0–P_3 are not included on ZPSD3X1 devices.
8. $\overline{DS}$ is not available on ZPSD3X1 devices.

Table 3. ZPSD3XX PAD A and PAD B Functions

	Function
PAD A and PAD B Inputs	
A19/$\overline{CSI}$	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 12 and 13). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 4, Note 6.
A11–A15	These are address inputs.
P0–P3	These are page number inputs (not available on ZPSD3X1 versions).
$\overline{RD}$/E/$\overline{DS}$	This is the read pulse or enable strobe input. (Note 9)
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/W select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 10 and 11.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Tables 6 and 7.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 6.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 6.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 6.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 4, Note 6. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. These tables are for information only since to implement to a specific mode, the PSD Development software will automatically set the configuration bits by using simple interactive menus.

Table 4. ZPSD3XX Non-Volatile Configuration Bits

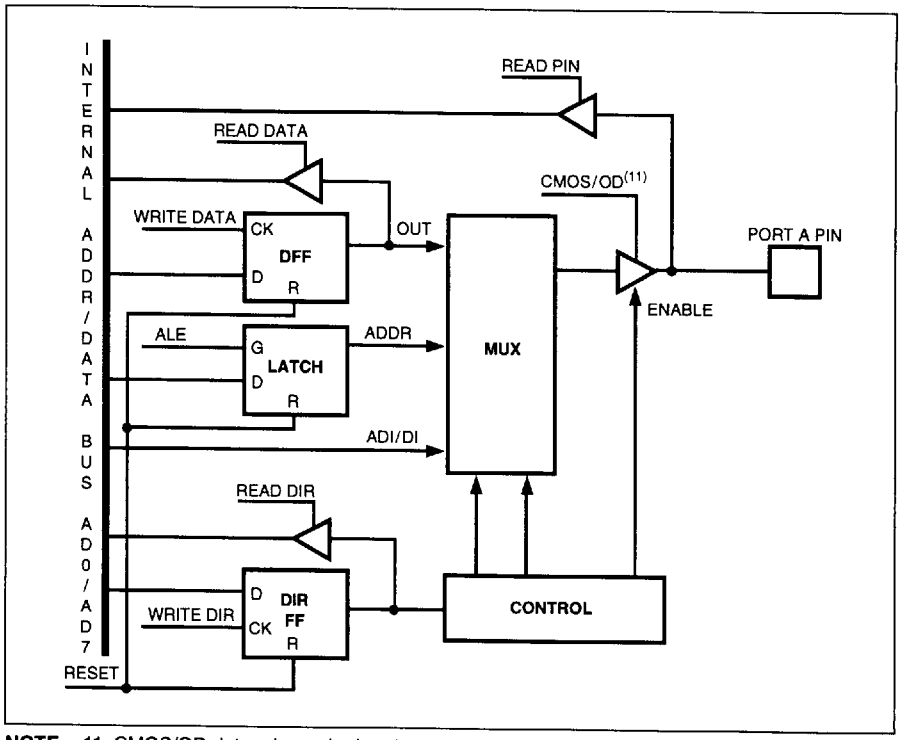
Use This Bit	To
CDATA	Set the data bus width to 8 or 16 bits (ZPSD30X only).
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CEDS	Determine the polarity and functionality of read and write. (Note 10)
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.
CSECURITY	Set the security on or off (a secured part can not be duplicated).
CRESET	Set the RESET polarity. (Note 10a)
$\overline{COMB}$/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 10 and 11).
CPAF1 (8 Bits)	Configure each pin of Port A in multiplexed mode to be an I/O or address out.
CPACOD (8 Bits)	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF (8 Bits)	Configure each pin of Port B as an I/O or a chip-select output'
CPBCOD (8 Bits)	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF (3 Bits)	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16 – A19 to go through a latch or to have their latch transparent.
CADLOG (4 Bits)	Configure A16 – A19 individually as logic or address inputs. (Note 10)
CATD	Configure pins A16–A19 as PAD logic inputs or high-order address inputs (Note 9).
CLOT	Determine in non-multiplexed mode if address inputs are transparent or latched (Note 10).
CRRWR	Set the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins to $\overline{RD}$ and $\overline{WR}$ pulse, or to E strobe and R/$\overline{W}$ status (Note 9).
CRRWR	Configure the polarity and control methods of read and write cycles. (Note 10)
CMISER	Controls the lower-power mode.

NOTES: 9. ZPSD3X1 only.
10. Not available on ZPSD3X1 versions.
10a Not available on ZPSD3XXV versions.

Port Functions

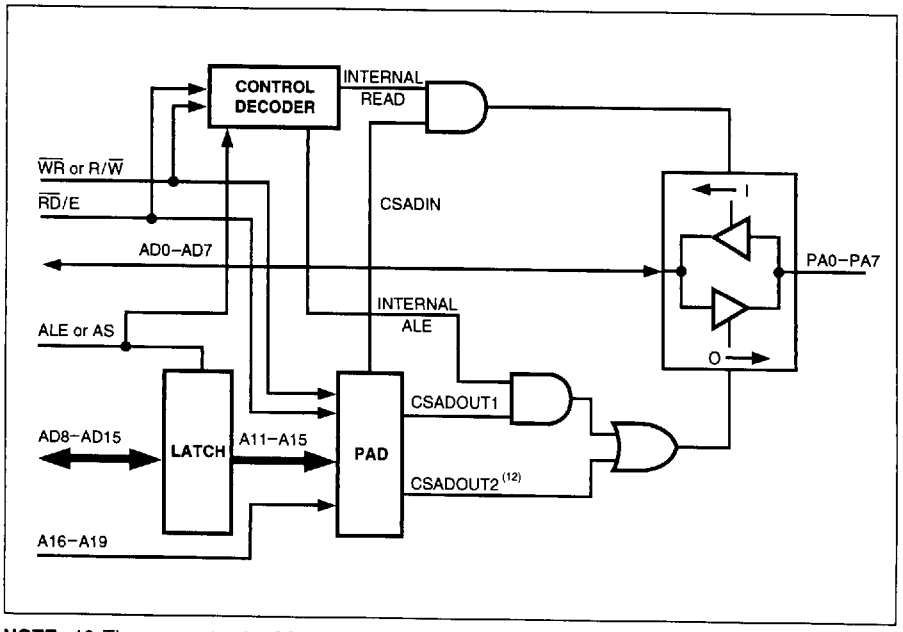
The ZPSD3XX has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 5 shows the pin structure of Port A.

Figure 5. Port A Pin Structure



NOTE: 11. CMOS/OD determines whether the output is open drain or CMOS.

Figure 6. Port A Track Mode



NOTE: 12. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Table 5. ZPSD3XX Configuration Bits[13,14]

Configuration Bits	No. of Bits	Function
CDATA (Note 15)	1	8-bit or 16-bit Data Bus Width CDATA = 0 eight bits CDATA = 1 sixteen bits
CADDRDAT	1	ADDRESS/DATA Multiplexed (separate buses) CADDRDAT = 0, non-multiplexed CADDRDAT = 1, multiplexed
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down CA19/$\overline{CSI}$ = 1, enable A19 input to PAD
CALE	1	Active HIGH or Active LOW CALE = 0, Active high CALE = 1, Active low
CRESET (Note 17a)	1	Active high or active low CRESET = 0, active low reset signal CRESET = 1, active high reset signal
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM 0 = Combined, 1 = Separate
CPAF1	8	Port A I/Os or A0–A7 CPAF1 = 0, Port A pin = I/O CPAF1 = 1, Port A pin = A0 – A7
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CATD (Note 17)	1	A16–A19 address or logic inputs CATD = 0, logic inputs CATD = 1, address inputs
CADDHLT	1	A16–A19 Transparent or Latched CADDHLT = 0, Address latch transparent CADDHLT = 1, Address latched (ALE dependent)
CSECURITY	1	SECURITY On/Off CSECURITY = 0, off CSECURITY = 1, on
CLOT (Note 16)	1	A0–A15 Address Inputs are transparent or ALE-dependent in non-multiplexed modes CLOT = 0, transparent CLOT = 1, ALE-dependent
CRRWR CEDS (Note 16)	2	Determine the polarity and control methods of read and write cycles. CEDS CRRWR 0 0 $\overline{RD}$ and $\overline{WR}$ active low pulses 0 1 R/$\overline{W}$ status and high E pulse 1 1 R/$\overline{W}$ status and low $\overline{DS}$ pulse
CRRWR (Note 17)	1	CRRWR = 0, $\overline{RD}$ and $\overline{WR}$ active low strobes CRRWR = 1, R/$\overline{W}$ status and E active high pulse
CPACOD	8	Port A CMOS or Open Drain Output CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBF	8	Port B is I/O or $\overline{CS0}$– $\overline{CS7}$ CPBF = 0, Port B pin is $\overline{CS0}$ – $\overline{CS7}$ CPBF = 1, Port B pin is I/O

Table 5. ZPSD3XX Configuration Bits (Cont.)

Configuration Bits	No. of Bits	Function
CPBCOD	8	Port B CMOS or Open Drain CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C pin is A16–A18 CPCF = 1, Port C pin is $\overline{CS8}$–$\overline{CS10}$
CADLOG (Note 16)	4	Port C: A16–A19 Address or Logic Input CADLOG = 0, Port C pin or A19/$\overline{CSI}$ is logic input CADLOG = 1, Port C pin or A19/$\overline{CSI}$ is address input
CMISER	1	Default: CMISER = 0 CMISER = 1, lower-power mode

This data sheet provides a complete listing of the function of each configuration bit in all control registers. In general, you will not need to be concerned about the details of most of these bits. The development software will set the bits automatically using information from your design files.

NOTES: 13. WSI's PSD Development software will guide the user to the proper configuration choice.
14. In an unprogrammed or erased part, all configuration bits are 0.
15. ZPSD30X only.
16. ZPSD3X2/3X3/3X4R only.
17. ZPSD3X1 only.
17a. Not included in ZPSD3XXV versions.

Port Functions (Cont.)

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 5). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 5). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature enables the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Another mode of Port A, i.e., Track Mode (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 6). When CSADOUT1 and ALE are true, the address on the input AD0/A0–AD7/A7 pins is output through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse. When CSADOUT2 is active, a write operation is performed (see note to Figure 6). The data on the input AD0/A0–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A0–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal location, data is presented on Port A pins. When writing to an internal location, data present on Port A pins is written to that location.

Port B in Multiplexed Address/Data and in 8-Bit Non-Multiplexed Modes

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 7). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 7). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternately, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Port B in 16-Bit Non-Multiplexed Address/Data Mode (ZPSD30X)

In this mode, Port B becomes the high-order data bus byte of the chip. When reading an internal high-order data bus byte location, the data is presented on Port B pins. When writing to an internal high-order data bus byte location, data present on Port B is written to that location. See Table 9.

Accessing the I/O Port Registers

Tables 6 and 7 show the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

Port C in All Modes

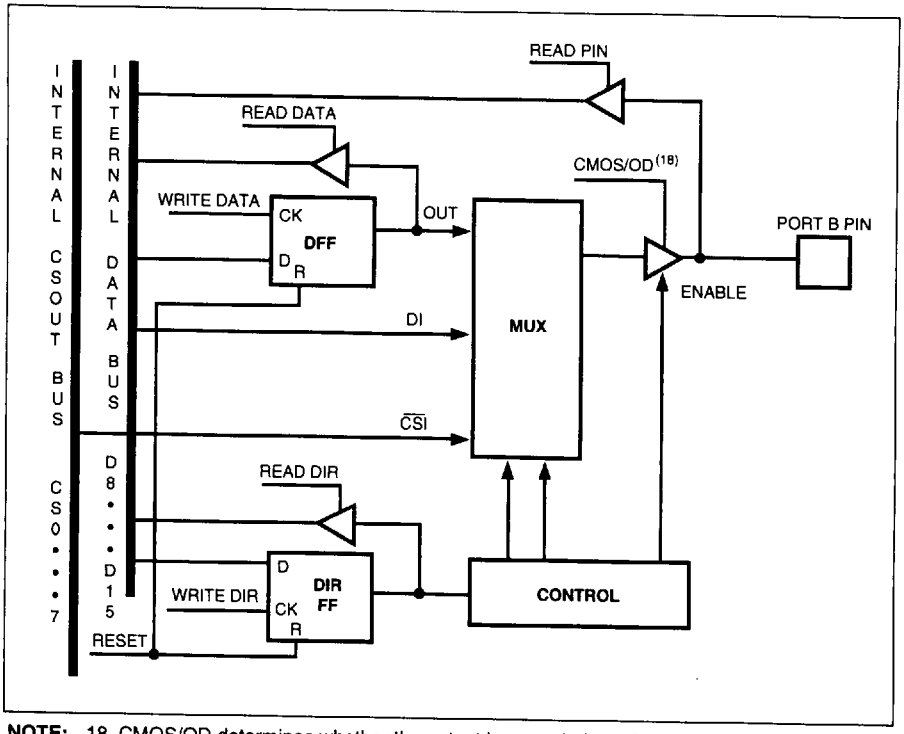
Each pin of Port C (shown in Figure 8) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternately, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

ALE/AS and A0–A15 in Non-Multiplexed Modes (ZPSD3X2/3X3/3X4R)

In non-multiplexed modes, A0–A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

Figure 7. Port B Pin Structure



NOTE: 18. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

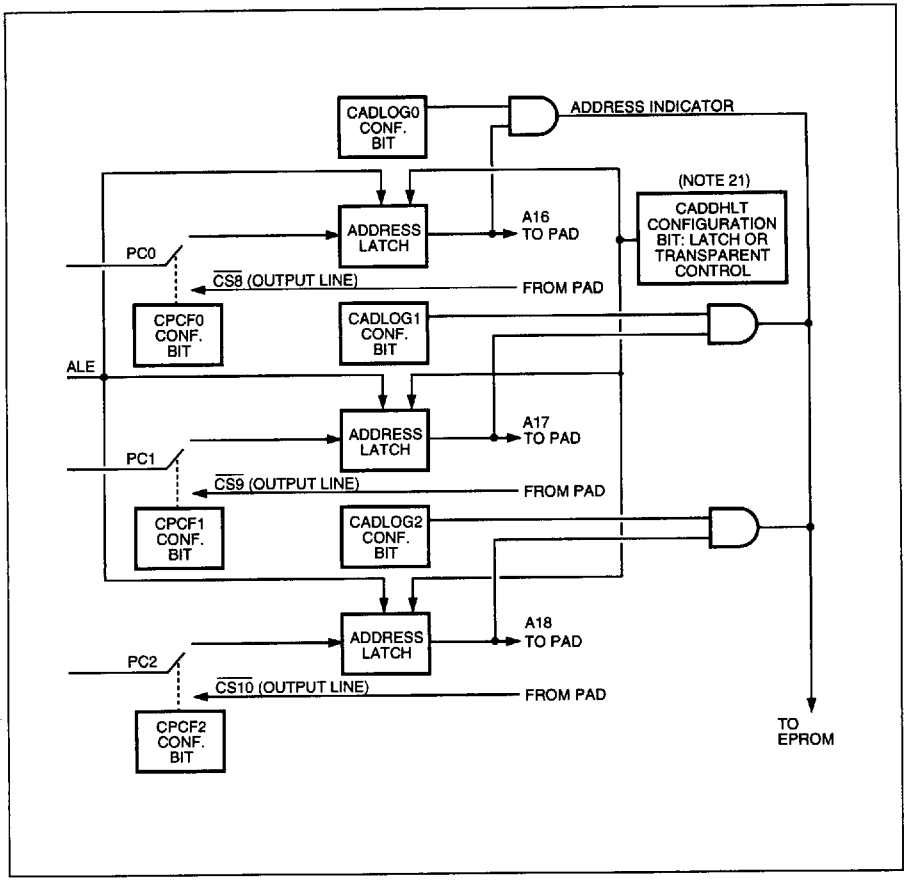
Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7
Power Management Register	+ 10
Page Register	+ 18

Table 7. I/O Port Addresses in a 16-bit Data Bus Mode[19,20] (ZPSD30X)

Register Name	Word Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Ports B and A	+ 2 (accessible during read operation only)
Direction Register of Ports B and A	+ 4
Data Register of Ports B and A	+ 6
Power Management Register	+ 10
Page Register	+ 18

NOTES: 19. When the data bus width is 16, Port B registers can only be accessed if the $\overline{BHE}$ signal is low.
20. I/O Ports A and B are still byte-addressable, as shown in Table 6. For I/O Port B register access, $\overline{BHE}$ must be low.

Figure 8. Port C Structure



NOTES: 21. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

22. ZPSD3X2/3X3/3X4R: Individual pins can be configured independently as address or logic inputs (CADLOG, bits 0–2).

ZPSD3X1: All Port C pins are either address or logic inputs (CATD).

A16–A19 Inputs

If one or more of the pins PC0, PC1 PC2 and CSI/A19 are configured as inputs, the configuration bits CADDHLT and CATD define their functionality inside the part. CADDHLT determines if these inputs are to be latched by the trailing edge of the ALE or AS signal (CADDHLT = 1), or enabled into the ZPSD3XX at all times (CADDHLT = 0, transparent mode). CATD determines whether these lines are high-order address lines, that take part in the derivation of EPROM select signals inside the chip (CATD = 1), or logic input lines that have no impact on memory or I/O selections (CATD = 0). Logic input lines typically participate in the Boolean expressions implemented in the PAD B. Unused input pins should be tied to V_{CC} or GND.

EPROM

The zero power EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 is selected by PAD outputs ES0–ES7, respectively.

The EPROM powers up only on address change and consumes power for the necessary time to latch data on its outputs. It then powers down and remains in standby mode.

Device	EPROM Size	EPROM Architecture		EPROM Bank Architecture (8 ea)	
		x8	x16	x8	x16
ZPSD301	256Kb	32K x 8	16K x 16	4K x 8	2K x 16
ZPSD311	256Kb	32K x 8	–	4K x 8	–
ZPSD302	512Kb	64K x 8	32K x 16	8K x 8	4K x 16
ZPSD312	512Kb	64K x 8	–	8K x 8	–
ZPSD303	1Mb	128K x 8	64K x 16	16K x 8	8K x 16
ZPSD313	1Mb	128K x 8	–	16K x 8	–
ZPSD304R	2Mb	256K x 8	128K x 16	32K x 8	16K x 16
ZPSD314R	2Mb	256K x 8	–	32K x 8	–

SRAM

Each ZPSD3XX device (except SRAMless Versions) has 16K bits of zero power SRAM. Depending on the configuration of the data bus, the SRAM organization can be 2K x 8 (8-bit data bus) or 1K x 16 (16-bit data bus). The SRAM is selected by the RS0 output of the PAD.

The SRAM powers up only on address change and consumes power for the necessary time to latch data on its outputs. It then powers down and remains in standby mode.

Memory Paging (ZPSD3X2/3X3/3X4R)

The page register consists of four flip-flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3–D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3–P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 9.

Figure 9. Page Register (ZPSD3X2/3X3/ 3X4R)

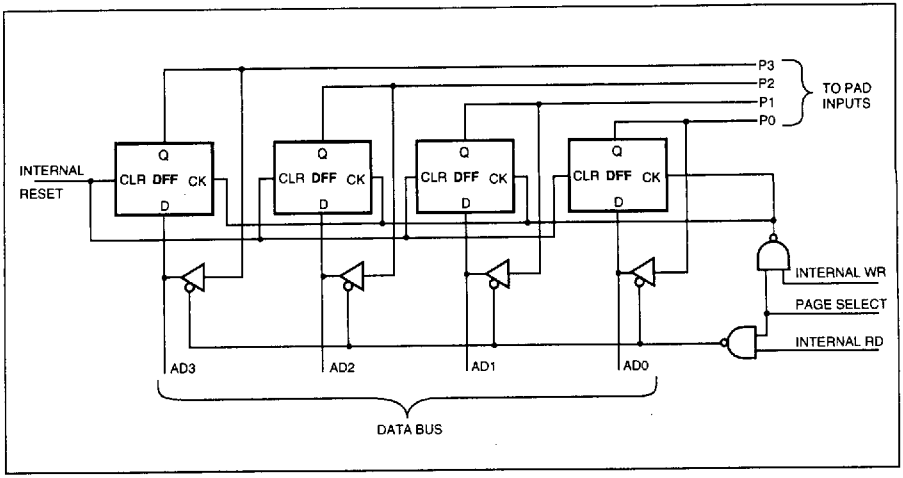


Table 8. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD8/A8–AD15/A15	CDATA , CADDRDAT, CLOT = 0	8-bit data, non-multiplexed	Transparent
	CDATA, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 1, CADDRDAT, CLOT = 0	16-bit data, non-multiplexed	Transparent
	CDATA = 1, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 0, CADDRDAT = 1	8-bit data, multiplexed	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed	ALE Dependent
AD0/A0-AD7/A7	CADDRDAT = 0, CLOT = 0	non-multiplexed modes	Transparent
	CADDRDAT = 0, CLOT = 1		ALE Dependent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
$\overline{BHE}$/$\overline{PSEN}$	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed mode, $\overline{BHE}$ is active	Transparent
A19 and PC2–PC0	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed mode, $\overline{BHE}$ is active	ALE Dependent
	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

Control Signals

The ZPSD3XX control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{BHE}$/$\overline{PSEN}$ or $\overline{PSEN}$, $\overline{RESET}$, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations are activated by an active low signal on this pin. As R/$\overline{W}$, the pin operates with the E strobe of the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$ (or $\overline{RD}$/E on ZPSD3X1)

In operational mode, this signal can be configured as $\overline{RD}$, E, or $\overline{DS}$. As $\overline{RD}$, all read operations are activated by an active low signal on this pin. As E, the pin operates with the R/$\overline{W}$ signal of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

As $\overline{DS}$, the pin functions with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write).

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{BHE}$/$\overline{PSEN}$

This pin's function depends on the ZPSD3XX data bus width. If it is 8 bits, the pin is $\overline{PSEN}$; if it is 16 bits, the pin is $\overline{BHE}$. In 8-bit mode, the $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read if selected. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1).

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the $\overline{PSEN}$ pin must be connected to the $\overline{PSEN}$ pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the $\overline{PSEN}$ pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1). See Figures 10 and 11.

In $\overline{BHE}$ mode, this pin enables accessing of the upper-half byte of the data bus. A low on this pin enables a write or read operation to be performed on the upper half of the data bus (see Table 9).

RESET

This is an asynchronous input pin that clears and initializes the ZPSD3XX. Reset polarity is programmable (active low or active high). Whenever the ZPSD3XX reset input is driven active for at least 100 ns, the chip is reset. The ZPSD3XX must be reset at power up before it can be used. Tables 10 and 11, and Figure 12 indicate the state of the part during and after reset.

Figure 10. Combined Address Space

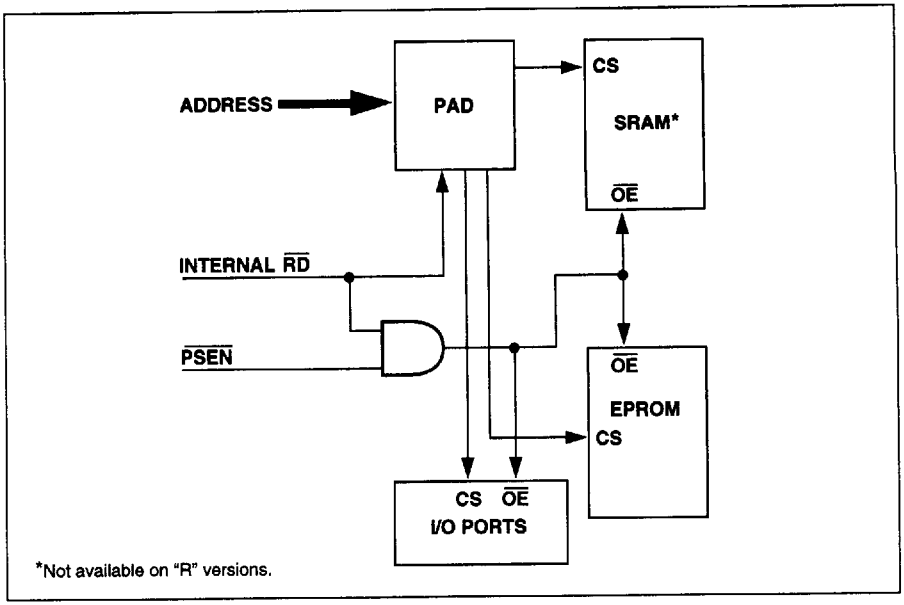


Figure 11. 8031-Type Separate Code and Data Address Spaces

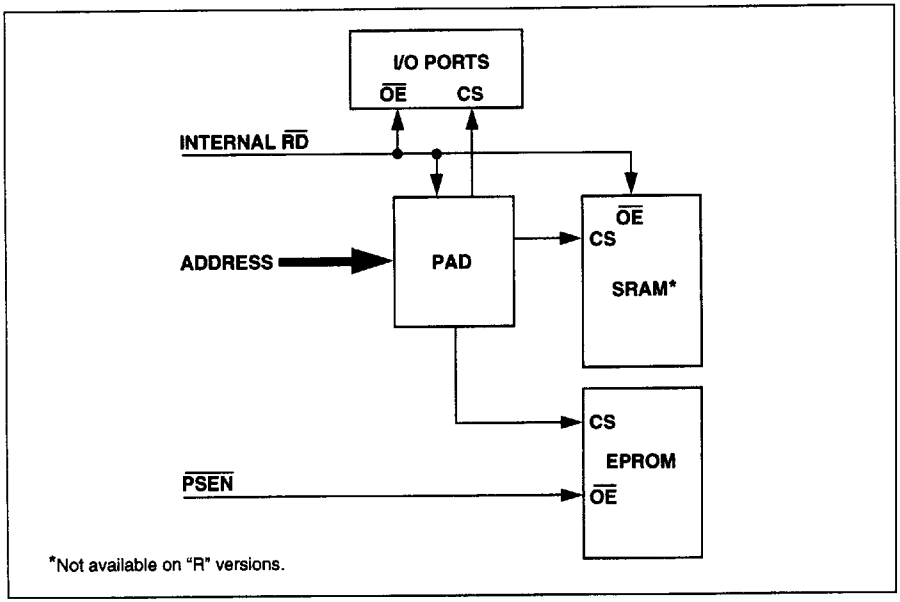


Table 9. High/Low Byte Selection Truth Table (in 16-Bit Configuration Only)

$\overline{BHE}$	A_0	Operation
0	0	Whole Word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

Table 10. Signal States During Reset Active (RESET)

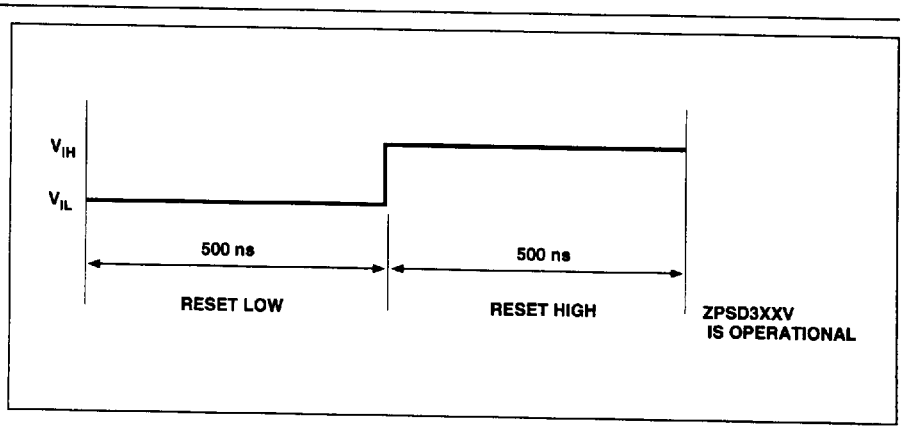
Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Table 11. Internal States During and After Reset Cycle

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 23)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0 – ES7	All = 0 (Note 23)
	Turbo Bit	0
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	0 0 0 0

NOTE: 23. All PAD outputs are in a non-active state.

Figure 12. The Reset Cycle (RESET) (ZPSD3XXV Versions)



Power Management

The power consumption of ZPSD is controlled by the A19/$\overline{CSI}$ input pin and two power management bits:

- ***Turbo Bit***
- ***CMiser Bit***

Turbo Bit

The Turbo bit is an "on the fly" configurable volatile bit. This bit enables the MCU to control the PAD power consumption and propagation delay. When Turbo is OFF (Logic "1"), the PAD is in Zero Power Mode and the PAD propagation delay is slower (see parameter tables). The EPROM or SRAM access time is not affected. When the Turbo bit is ON (Logic "0"), the Zero Power option of the PAD is disabled placing the PAD in high speed mode. The Turbo bit is located in the Power Management Register at address CSIOP + displacement of 10 H at data bus bit zero. Upon reset the Turbo bit is ON.

Power Management Register (PMR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	*	*	Turbo Bit
1 = OFF	1 = OFF	1 = OFF	1 = OFF	1 = OFF	1 = OFF	1 = OFF	1 = OFF

*Future Configuration bits are reserved and should be set to one.

EPROM

The EPROM power consumption in the PSD is controlled by bit 3 in the PMMR0 – EPROM CMiser. Upon reset the CMiser bit is OFF. This will cause the EPROM to be ON at all times as long as CSI is enabled (low). The reason this mode is provided is to reduce the access time of the EPROM by 10 ns relative to the low power condition when CMiser is ON. If CSI is disabled (high) the EPROM will be deselected and will enter standby mode (OFF) overriding the state of the CMiser.

If CMiser is set (ON) then the EPROM will enter the standby mode when not selected. This condition can take place when CSI is high or when CSI is low and the EPROM is not accessed. For example, if the MCU is accessing the SRAM, the EPROM will be deselected and will be in low power mode.

An additional advantage of the CMiser is achieved when the PSD is configured in the by 8 mode (8 bit data bus). In this case an additional power savings is achieved in the EPROM (and also in the SRAM) by turning off 1/2 of the array even when the EPROM is accessed (the array is divided internally into odd and even arrays).

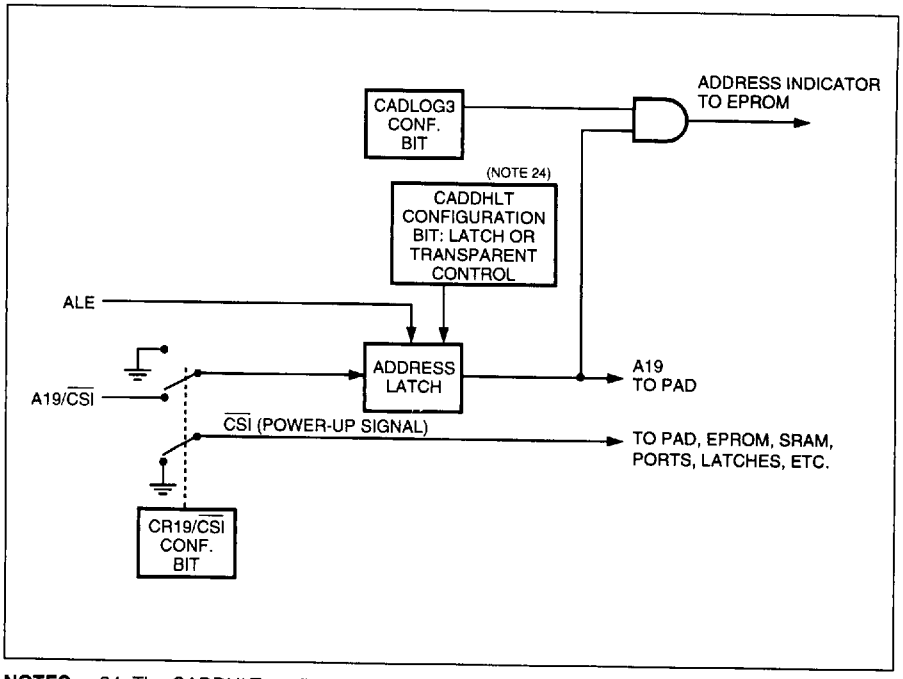
The power consumption for the different EPROM modes is given in the DC Characteristics table under I_{CC} (DC) EPROM Adder.

A19/$\overline{CSI}$

When configured as $\overline{CSI}$, a high on this pin deselects and powers down the chip. A low on this pin puts the chip in normal operational mode. When $\overline{CSI}$ is enabled and none of the inputs are changing, the ZPSD is in power-down mode (Turbo Bit = OFF). For ZPSD3XX states during the power-down mode, see Tables 12 and 13, and Figure 13.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADLOG3 = 1) or as a general-purpose logic input (CADLOG3 = 0). A19 can be configured as ALE dependent or as a transparent input (see Table 8). In this mode, the chip is always enabled.

Figure 13. A19/$\overline{CSI}$ Cell Structure



NOTES: 24. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.
25. In the ZPSD3X1, the CATD configuration bit performs this function for all the A16–A19 lines.

Table 12a. Signal States During Power-Down Mode (ZPSD30X)

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

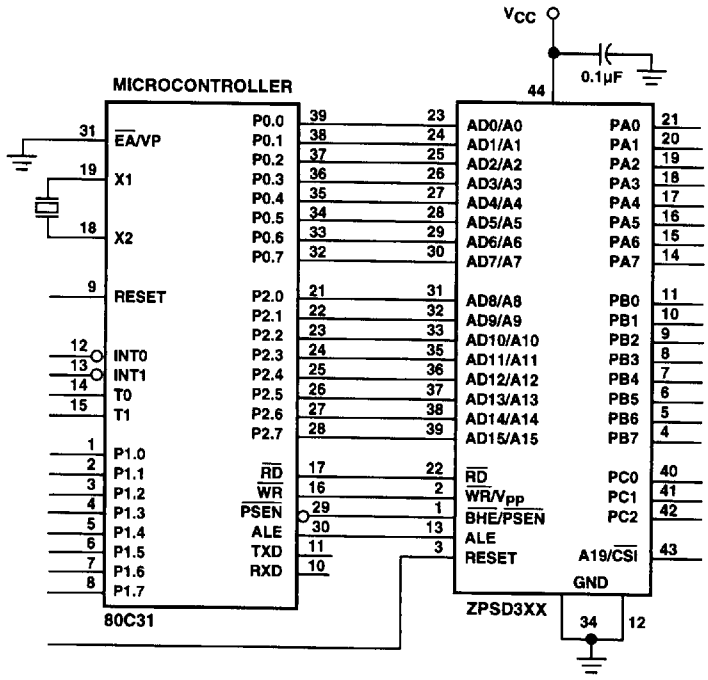
Table 12b. Signal States During Power-Down Mode (ZPSD31X)

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs CS0–CS7 open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 13. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Figure 14. ZPSD3XX Interface With Intel's 80C31



NOTE: RESET to the ZPSD3XX must be the output of a RESET chip or buffer. If RESET to the 80C31 is the output of an RC circuit, a separate buffered RC RESET to the ZPSD3XX (shorter than the 80C31 RC RESET) must be provided to avoid a race condition.

The configuration bits for Figure 14 are:

CALE	0	COMB/SEP	0 or 1 (both valid)
CDATA	0	CRRWR	0
CADDRDAT	1	CEDS	0
CRESET	1		

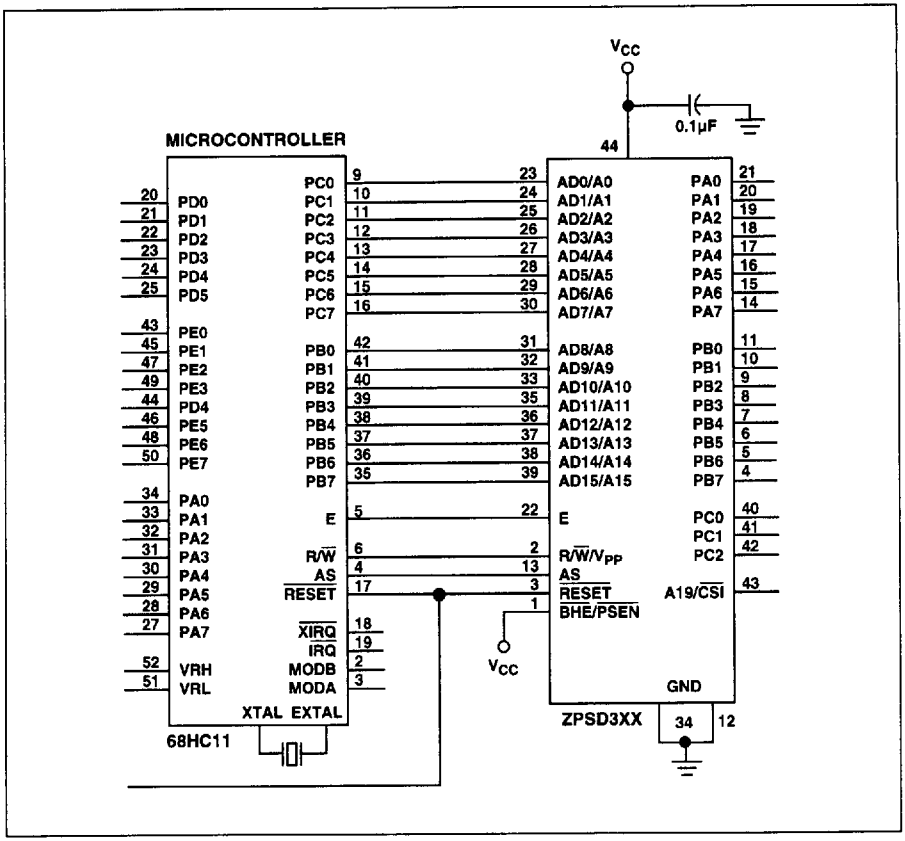
All other configuration bits may vary according to the application requirements.

System Applications

In Figure 14, the ZPSD3XX is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

In Figure 15, the ZPSD3XX is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/W signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are specific and, thus, user dependent.

Figure 15. ZPSD3XX Interface With Motorola's 68HC11



The configuration bits for Figure 15 are:

CALE	0	COMB/SEP	0
CDATA	0	CRRWR	1
CADDRDAT	1	CEDS	0
CRESET	0		

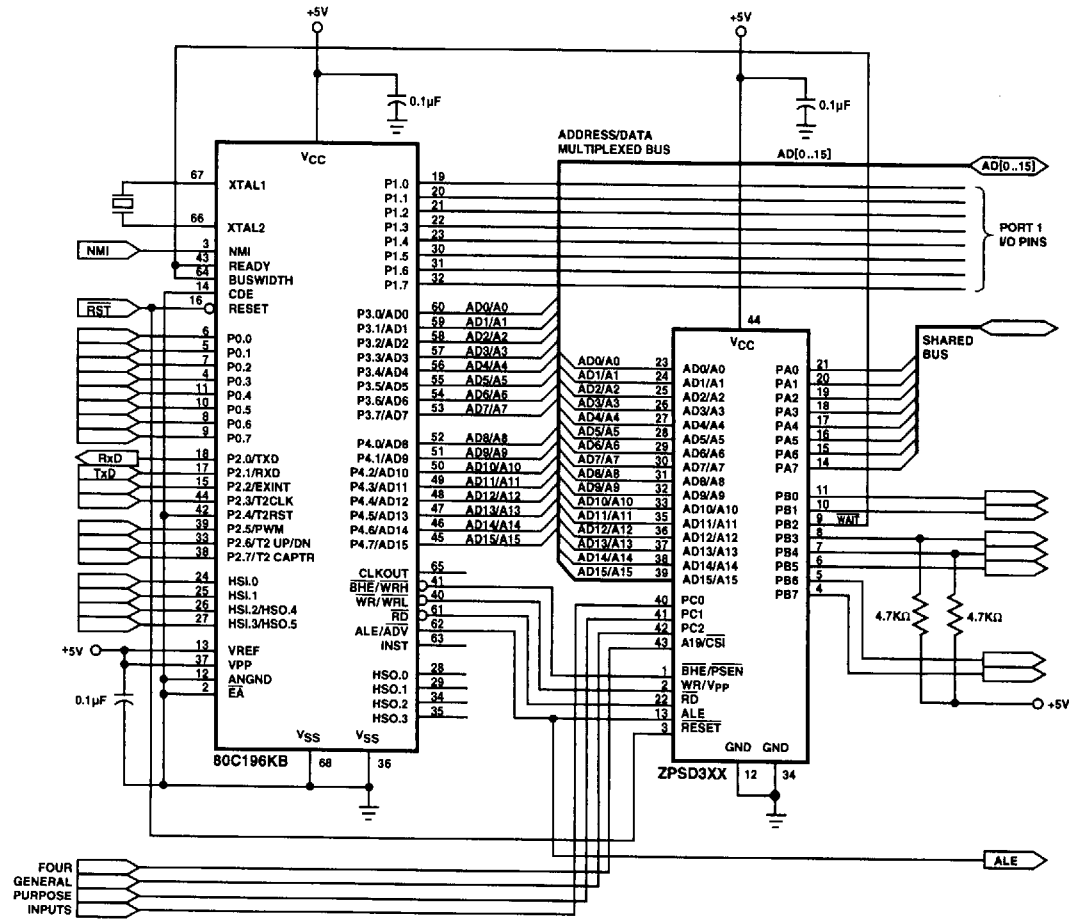
All other configuration bits may vary according to the application requirements.

System Applications (Cont.)

In Figure 16, the ZPSD3XX is configured to work directly with Intel's 80C196KB microcontroller, which is a 16-bit address/16-bit data bus processor. Address and data lines multiplexed. In the example shown, all configuration bits are set. The ZPSD3XX is configured to use PC0, PC1, PC2, and A19/$\overline{CSI}$ as A16, A17, A18, and A19 inputs, respectively. These signals are independent of the ALE pulse (latch-transparent). They are used as four general-purpose logic inputs that take part in the PAD equations implementation.

Port A is configured to work in the special track mode, in which (for certain conditions) PA0–PA7 tracks lines AD0/A0–AD7/A7. Port B is configured to generate $\overline{CS0}$–$\overline{CS7}$. In this example, PB2 serves as a $\overline{WAIT}$ signal that slows down the 80C196KB during the access of external peripherals. These 8-bit wide peripherals are connected to the shared bus of Port A. The $\overline{WAIT}$ signal also drives the buswidth input of the microcontroller, so that every external peripheral cycle becomes an 8-bit data bus cycle. PB3 and PB4 are open-drain output signals; thus, they are pulled up externally.

Figure 16. ZPSD3XX Interface With Intel's 80C196KB.



The configuration bits for Figure 16 are:

CALE	0	CSECURITY	Don't care
CDATA	1	CPCF2, CPCF1, CPCF0	0, 0, 0
CADDRDAT	1	CPACOD7–CPACOD0	00H
CPAF1	Don't care	CPBF7–CPBF0	00H
CPAF2	1	CPBCOD7–CPBCOD0	18H
CA19/$\overline{CSI}$	1	CEDS	0
CRRWR	0	CADLOG3—CADLOG0	0H
COMB/SEP	0		
CADDHLT	0		
CRESET	0		

Security Mode

Security Mode in the ZPSD3XX locks the contents of the PAD A, PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the PSD Development software or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the ZPSD3XX contents cannot be copied on a programmer.

Absolute Maximum Ratings[26]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection		>2000		V

NOTE: 26. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance
Commercial	0° C to +70°C	+ 3 V, + 5 V	± 10%
Industrial	–40° C to +85°C	+ 3 V, + 5 V	± 10%
Military	–55° C to +125°C	+ 3 V, + 5 V	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	ZPSD Versions, All Speeds	4.5	5	5.5	V
V_{CC}	Supply Voltage	ZPSD V Versions Only, All Speeds	2.7	3.0	5.5	V

DC Characteristics – Commercial

(5 V ± 10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage	4.5 V < V_{CC} > 5.5 V	2		V_{CC} + .1	V
V_{IL}	Low-Level Input Voltage	4.5 V < V_{CC} > 5.5 V	−0.5		0.8	V
V_{OH}	Output High Voltage	I_{OH} = −20 µA, V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = −2 mA, V_{CC} = 4.5 V	2.4	3.9		V
V_{OL}	Output Low Voltage (See Figure 17)	I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	V
I_{SB}	Standby Supply Current	$\overline{CSI}$ > V_{CC} −.3 V		10	20	µA
I_{LI}	Input Leakage Current	V_{SS} < V_{IN} > V_{CC}	−1	±.1	1	µA
I_{LO}	Output Leakage Current	.45 < V_{IN} > V_{CC}	−10	±5	10	µA
I_{CC} (DC) (Note 28a)	Operating Supply Current	ZPLD_TURBO = OFF, f = 0 MHz		10	20	µA
		ZPLD_TURBO = ON, f = 0 MHz		0.5	1	mA/PT
I_{CC} (AC) (Note 28a)	ZPLD AC Base	(See Figure 18)				mA/MHz
	EPROM Access AC Adder	CMiser = ON and 8-Bit Bus Mode		0.8	2.0	mA/MHz
		All Other Cases (Note 30)		1.8	4.0	mA/MHz
	SRAM Access AC Adder	CMiser = ON and 8-Bit Bus Mode		1.4	2.7	mA/MHz
		CMiser = ON and 16-Bit Bus Mode		2	4	mA/MHz
		CMiser = OFF		3.8	7.5	mA/MHz

NOTES: 27. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
28. TTL inputs: V_{IL} ≤ 0.8 V, V_{IH} ≥ 2.0 V.
28a. I_{OUT} = 0 mA.
29. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
30. All other cases include CMiser = ON and 16-bit bus mode and CMiser = OFF and 8- or 16-bit bus mode.

Example of ZPSD3XX Typical Power Calculation at V_{CC} = 5 V

Conditions	
MCU ALE Frequency	2 MHz
% of EPROM Access	80%
% of SRAM Access	15%
% of I/O Access	5% (No additional power above the ZPLD AC Base)
Number of PAD Product Terms Used	10 PT
8 Bit Data Bus, CMiser = ON, Turbo = OFF	

Calculation

I_{SB} = I_{CC} (DC) = 10 µ A

I_{CC} (AC) = ZPLD AC Base @ 2 MHz (see Figure 18)
+ 80% of EPROM Access x EPROM Access AC Adder x 2 MHz
+ 15% of SRAM Access x SRAM Access AC Adder x 2 MHz
= .75 mA + 80% x 2 MHz x 0.8 mA/MHz + 15% x 2 MHz x 1.4 mA/MHz = 2.45 mA

Figure 17. I_{OL} vs. V_{OL} (5 V ± 10%)

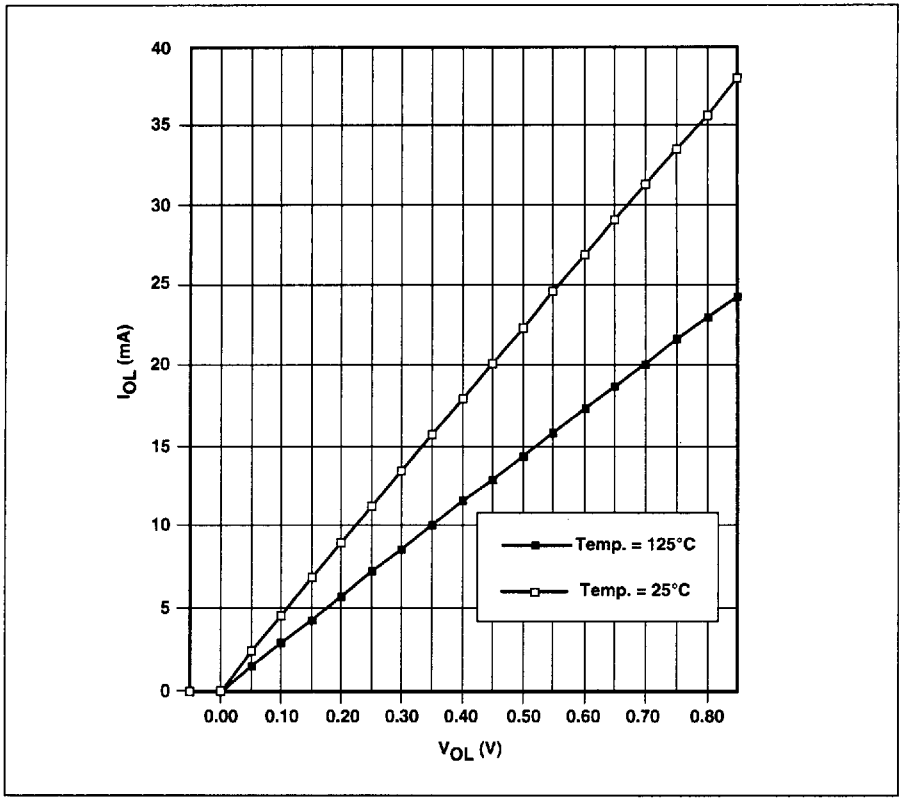
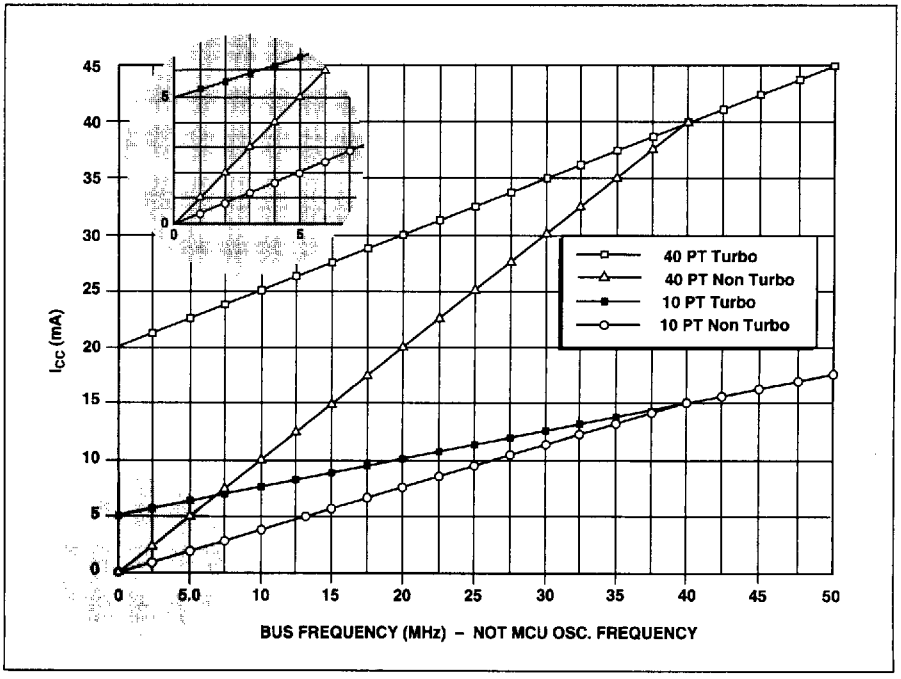


Figure 18. PAD Typical I_{CC} vs. Frequency (5 V ± 10%)



DC Characteristics – Commercial

(ZPSD V Versions Only) (3 V ± 10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	2.7	3	5.5	V
V_{IH}	High-Level Input Voltage	2.7 V < V_{CC} > 5.5 V	.7 V_{CC}		V_{CC} + .5	V
V_{IL}	Low-Level Input Voltage	2.7 V < V_{CC} > 5.5 V	−0.5		.3 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = −20 µA, V_{CC} = 2.7 V	2.6	2.69		V
		I_{OH} = −1 mA, V_{CC} = 2.7 V	2.3	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 20 µA, V_{CC} = 2.7 V		0.01	0.1	V
		I_{OL} = 4 mA, V_{CC} = 2.7 V		0.15	0.45	V
I_{SB}	Standby Supply Current	$\overline{CSI}$ > V_{CC} −.3 V (V_{CC} = 3.0 V)		1	5	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	−1	±.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	−1	.1	1	µA
I_{CC} (DC) (Note 32a)	Operating Supply Current	ZPLD_TURBO = OFF, f = 0 MHz (V_{CC} = 3.0 V)		1	5	µA
		ZPLD_TURBO = ON, f = 0 MHz (V_{CC} = 3.0 V)		.17	.35	mA/PT
I_{CC} (AC) (Note 32a)	ZPLD AC Base	See Figure 19 (V_{CC} = 3.0 V)				mA/MHz
	EPROM Access AC Adder	CMiser = ON and 8-Bit Bus Mode (V_{CC} = 3.0 V)		0.4	1	mA/MHz
		All Other Cases (Note 34) (V_{CC} = 3.0 V)		0.9	1.7	mA/MHz
	SRAM Access AC Adder	CMiser = ON and 8-Bit Bus Mode (V_{CC} = 3.0 V)		0.7	1.4	mA/MHz
		CMiser = ON and 16-Bit Bus Mode (V_{CC} = 3.0 V)		1	2	mA/MHz
		CMiser = OFF (V_{CC} = 3.0 V)		1.9	3.8	mA/MHz

NOTES: 31. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
32. TTL inputs: V_{IL} ≤ 0.8 V, V_{IH} ≥ 2.0 V.
32a. I_{OUT} = 0 mA.
33. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
34. All other cases include CMiser = ON and 16-bit bus mode and CMiser = OFF and 8- or 16-bit bus mode.

Example of ZPSD3XXV Typical Power Calculation at V_{CC} = 3.0 V

Conditions	
MCU ALE Frequency	2 MHz
% of EPROM Access	80%
% of SRAM Access	15%
% of I/O Access	5% (No additional power above the ZPLD AC Base)
Number of PAD Product Terms Used	10 PT
8 Bit Data Bus, CMiser = ON, Turbo = OFF	

Calculation

I_{SB} = I_{CC} (DC) = 1 µ A

I_{CC} (AC) = ZPLD AC Base @ 2 MHz (see Figure 19)
+ 80% of EPROM Access x EPROM Access AC Adder x 2 MHz
+ 15% of SRAM Access x SRAM Access AC Adder x 2 MHz
= 0.6 mA + 80% x 2 MHz x 0.4 mA/MHz + 15% x 2 MHz x .7 mA/MHz = 1.45 mA

NOTE: at 2.7 V, I_{CC} (AC) = 1.45 mA x 0.9 = 1.3 mA

Figure 19. Typical PLD AC I_{CC} Curve (V_{CC} = 3.0 V)

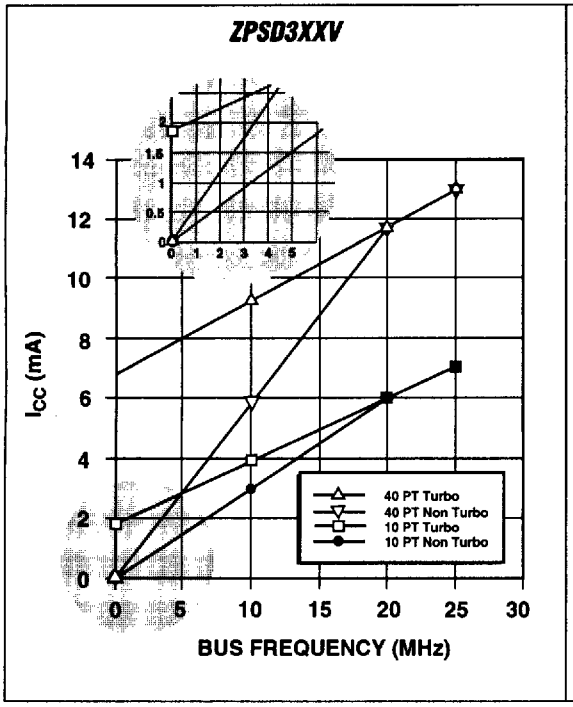


Figure 20. Normalized I_{CC} (DC vs. V_{CC}) (V_{CC} = 3.0 V)

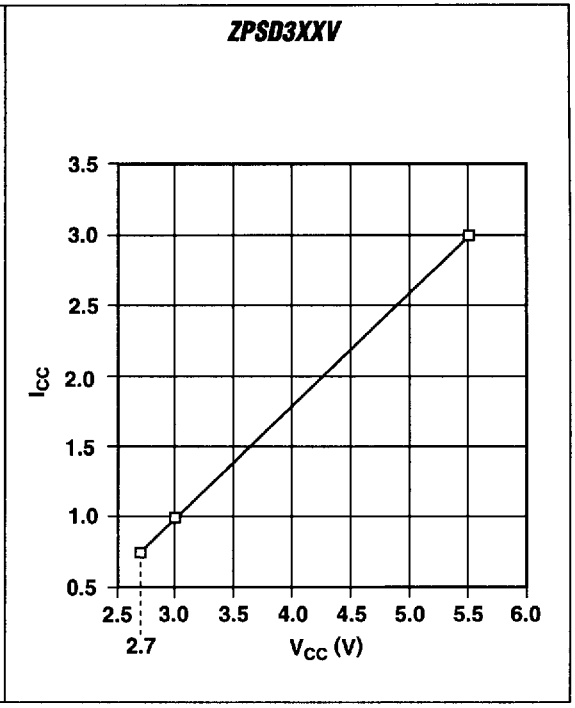


Figure 21. Normalized I_{CC} (AC) (V_{CC} = 3.0 V)

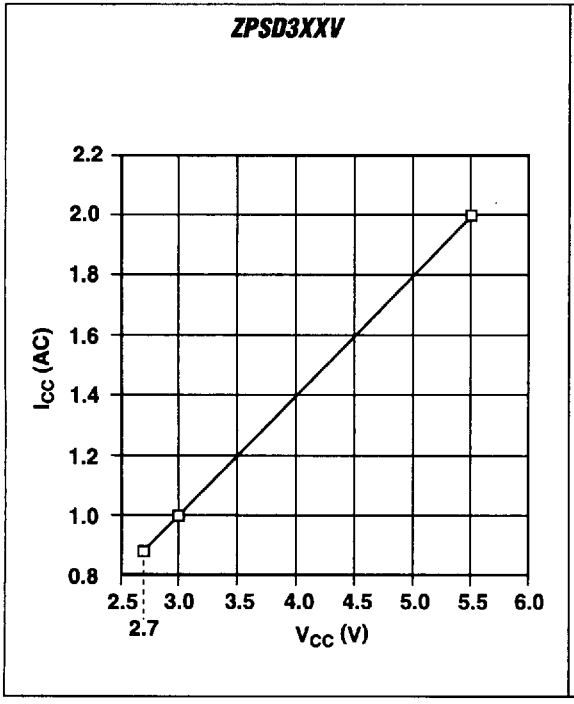
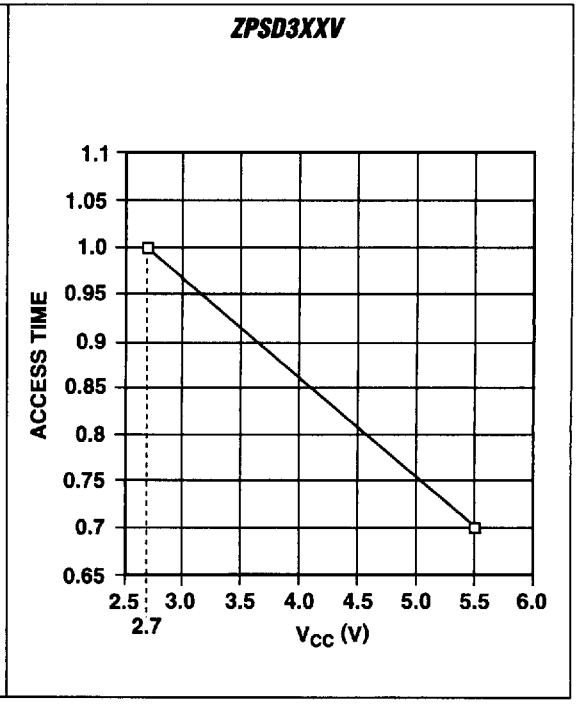


Figure 22. Normalized Access Time (T6) (V_{CC} = 3.0 V)



AC Characteristics

(5 V ± 10%)

Symbol	Parameter	-70		-90		-15		CMiser On = Add	Turbo Off = Add	Unit
		Min	Max	Min	Max	Min	Max			
T1	ALE or AS Pulse Width	18		20		40		0	0	ns
T2	Address Set-up Time	5		5		12		0	0	ns
T3	Address Hold Time	7		8		10		0	0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0	0	ns
T5	ALE Valid to Data Valid		80		100		160	10	0	ns
T6	Address Valid to Data Valid		70		90		150	10	0	ns
T7	$\overline{CSI}$ Active to Data Valid		80		100		160	10	0	ns
T8	Leading Edge of Read to Data Valid		20		32		55	0	0	ns
T8A	Leading Edge of Read to Data Valid in 8031-Based Architecture Operating with $\overline{PSEN}$ and $\overline{RD}$ in Separate Mode		32		32		55	0	0	ns
T9	Read Data Hold Time	0		0		0		0	0	ns
T10	Trailing Edge of Read to Data High-Z		20		32		35	0	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0	0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	35		40		60		0	0	ns
T12A	$\overline{WR}$ Pulse Width	18		20		35		0	0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	5		5		5		0	0	ns
T14	Address Valid to Trailing Edge of Write	70		90		150		0	0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	80		100		160		0	0	ns
T16	Write Data Set-up Time	18		20		30		0	0	ns
T17	Write Data Hold Time	5		5		10		0	0	ns
T18	Port to Data Out Valid Propagation Delay		25		30		35	0	0	ns
T19	Port Input Hold Time	0		0		0		0	0	ns
T20	Trailing Edge of Write to Port Output Valid		30		40		50	0	0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	20	6	25	6	35	0	10	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	20	5	25	4	35	0	10	ns

AC Characteristics (Cont.)

(5 V ± 10%)

Symbol	Parameter	-70		-90		-15		CMiser On = Add	Turbo Off = Add	Unit
		Min	Max	Min	Max	Min	Max			
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		28	0	0	ns
	Latched Address Outputs, Port A		22		22		28	0	0	
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		33		50	0	10	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		30		32		35	0	0	ns
T25	Track Mode Read Propagation Delay		27		29		35	0	0	ns
T26	Track Mode Read Hold Time	5	29	11	29	11	29	0	0	ns
T27	Track Mode Write Cycle, Data Propagation Delay		18		20		30	0	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	6	30	8	30	9	40	0	10	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		2		2		0	0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	8	37	9	40	9	50	0	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	8	37	9	40	9	50	0	0	ns
T32	Direct PAD Input as Hold Time	0		10		12		0	0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	18		20		30		0	0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	18		20		30		0	0	ns
T35	AS Inactive to E high	0		0		0		0	0	ns
T36	Address to Leading Edge of Write	18		20		25		0	0	ns

NOTES: 35. ADi = any address line.
36. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
37. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
38. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

AC Characteristics

(ZPSD V Versions Only) (3.0 V ± 10%)

Symbol	Parameter	-15		-20		-25		CMiser On = Add	Turbo Off = Add	Unit
		Min	Max	Min	Max	Min	Max			
T1	ALE or AS Pulse Width	40		50		60		0	0	ns
T2	Address Set-up Time	12		15		20		0	0	ns
T3	Address Hold Time	10		15		20		0	0	ns
T4	Leading Edge of Read to Data Active	0		0		0		0	0	ns
T5	ALE Valid to Data Valid		170		200		250	20	0	ns
T6	Address Valid to Data Valid		150		200		250	20	0	ns
T7	$\overline{CSI}$ Active to Data Valid		160		200		250	20	0	ns
T8	Leading Edge of Read to Data Valid		45		50		60	0	0	ns
T8A	Leading Edge of Read to Data Valid in 8031-Based Architecture Operating with $\overline{PSEN}$ and $\overline{RD}$ in Separate Mode		65		70		80	0	0	ns
T9	Read Data Hold Time	0		0		0		0	0	ns
T10	Trailing Edge of Read to Data High-Z		45		50		55	0	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write	0		0		0		0	0	ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, or $\overline{DS}$ Pulse Width	60		75		85		0	0	ns
T12A	$\overline{WR}$ Pulse Width	35		45		55		0	0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	5		5		5		0	0	ns
T14	Address Valid to Trailing Edge of Write	150		200		250		0	0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	160		200		250		0	0	ns
T16	Write Data Set-up Time	30		40		50		0	0	ns
T17	Write Data Hold Time	10		12		15		0	0	ns
T18	Port to Data Out Valid Propagation Delay		45		50		60	0	0	ns
T19	Port Input Hold Time	0		0		0		0	0	ns
T20	Trailing Edge of Write to Port Output Valid		50		60		70	0	0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	50	5	55	5	60	0	20	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	4	50	4	55	4	60	0	20	ns

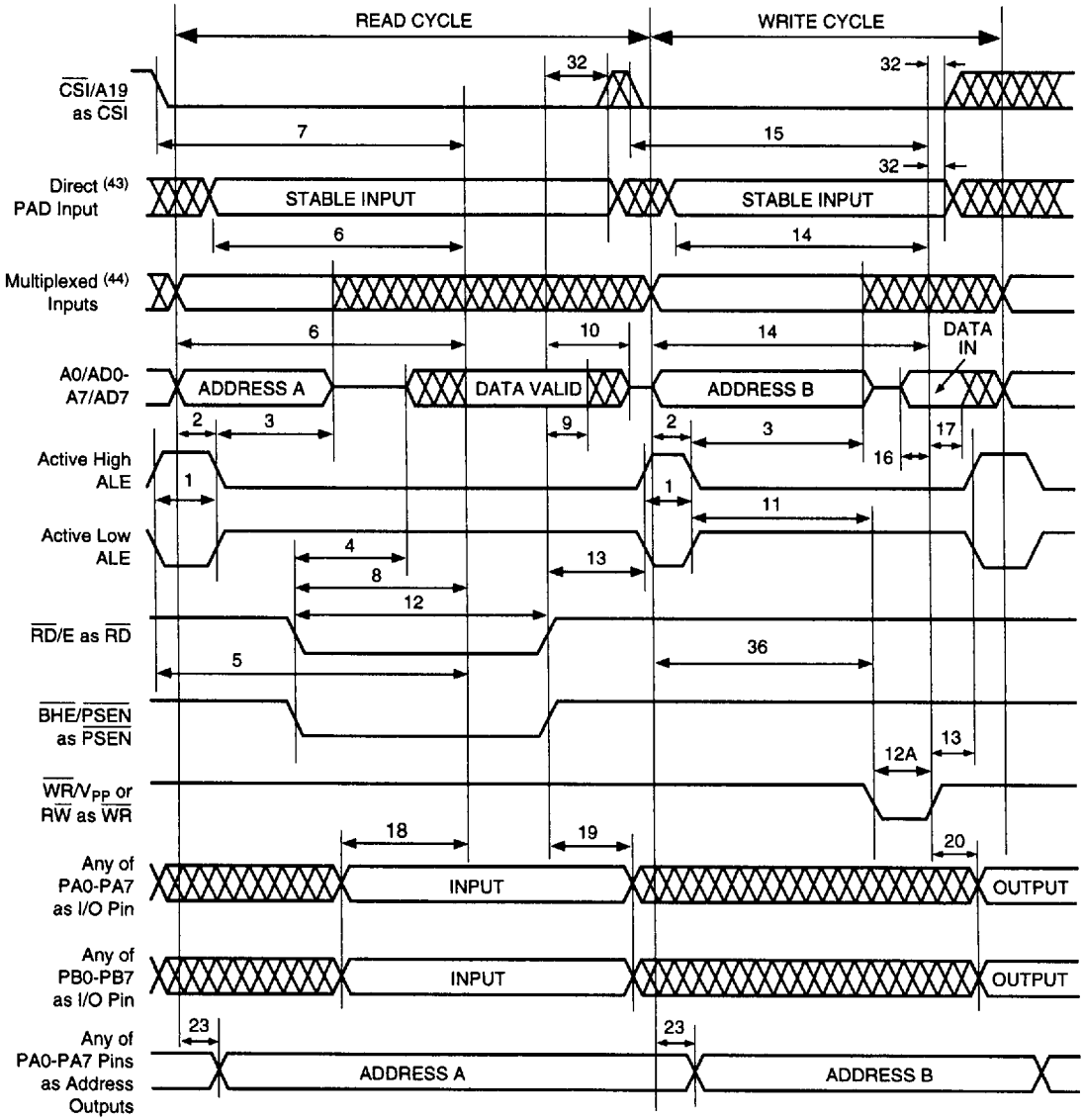
AC Characteristics (Cont.)

(ZPSD V Versions Only) (3.0 V ± 10%)

Symbol	Parameter	-15		-20		-25		CMiser On = Add	Turbo Off = Add	Unit
		Min	Max	Min	Max	Min	Max			
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		50		60		60	0	0	ns
	Latched Address Outputs, Port A		50		60		60	0	0	
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		70		80		90	0	20	ns
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		50		60		60	0	0	ns
T25	Track Mode Read Propagation Delay		45		55		60	0	0	ns
T26	Track Mode Read Hold Time	10	70	10	70	10	70	0	0	ns
T27	Track Mode Write Cycle, Data Propagation Delay		45		55		60	0	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	8	65	8	75	8	80	0	20	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		3		3		0	0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	70	9	80	9	90	0	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	70	9	80	9	90	0	0	ns
T32	Direct PAD Input as Hold Time	0		0		0		0	0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	30		40		50		0	0	ns
T34	E or $\overline{DS}$ End to R/$\overline{W}$	30		40		50		0	0	ns
T35	AS Inactive to E high	0		0		0		0	0	ns
T36	Address to Leading Edge of Write	30		35		40		0	0	ns

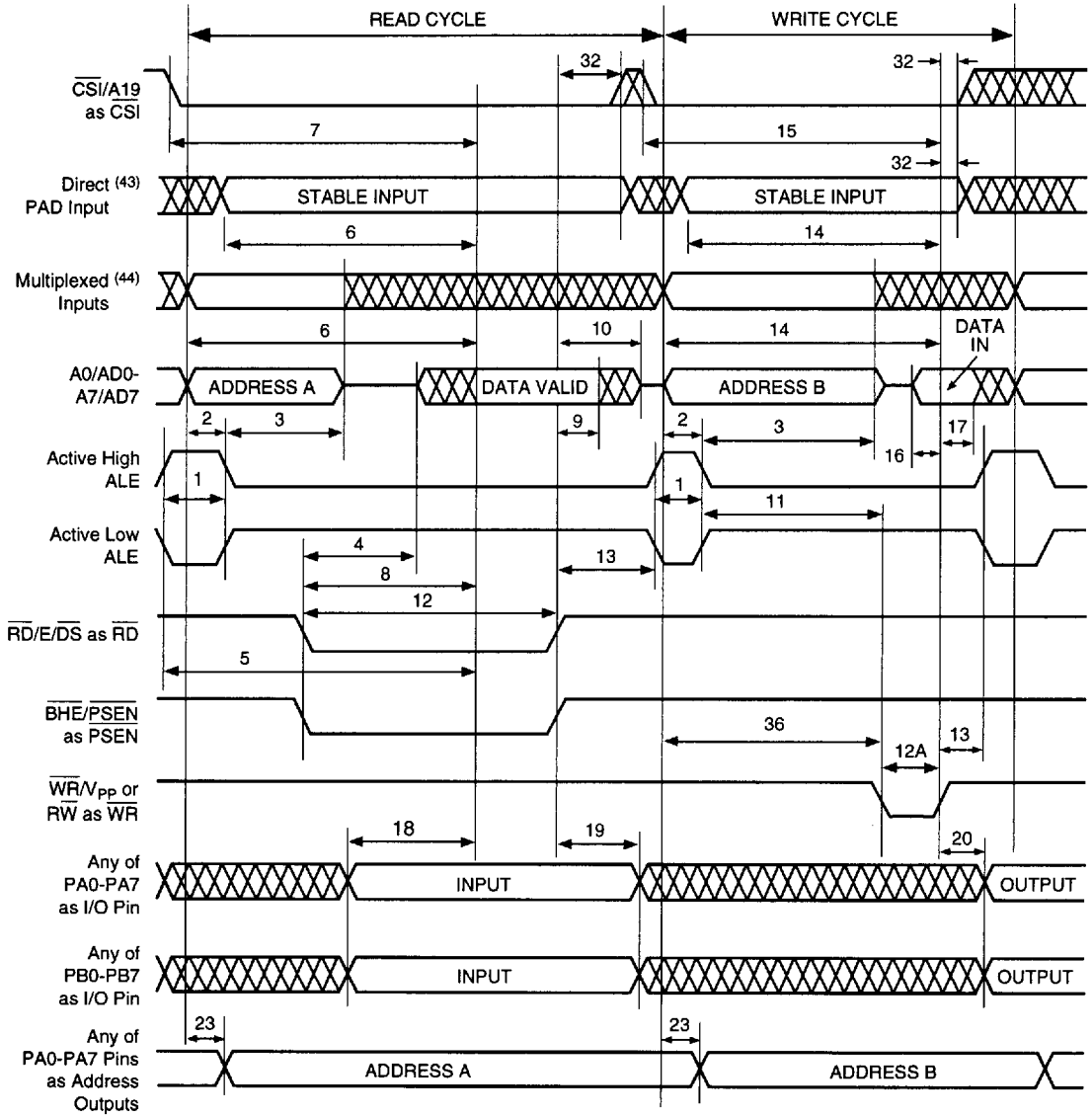
NOTES: 39. ADi = any address line.
40. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
41. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
42. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 23. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0 (ZPSD3X1)



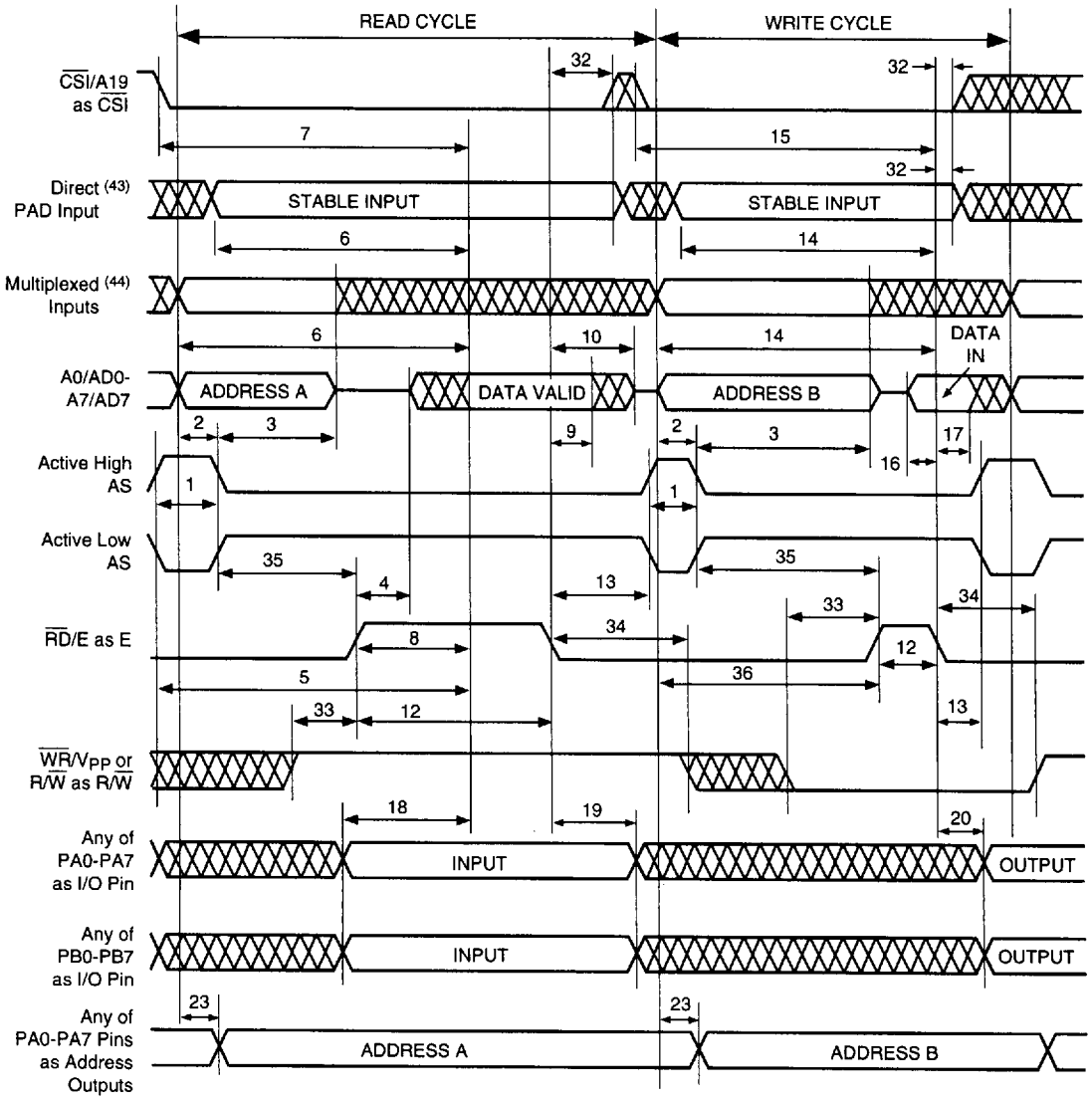
See referenced notes on page 3-63.

Figure 24. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0 (ZPSD3X2/3X3/3X4R)



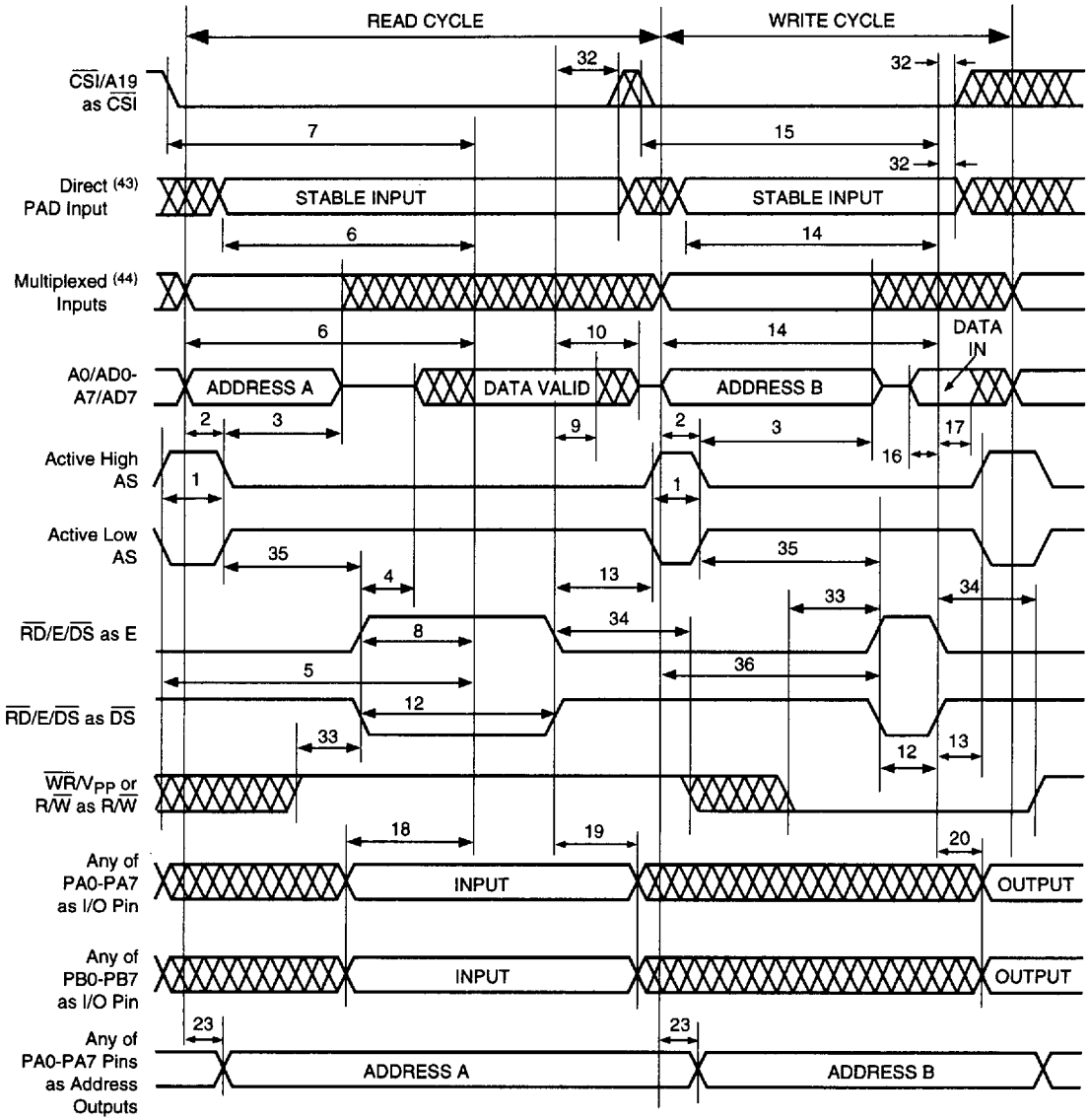
See referenced notes on page 3-63.

Figure 25. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1 (ZPSD3X1)



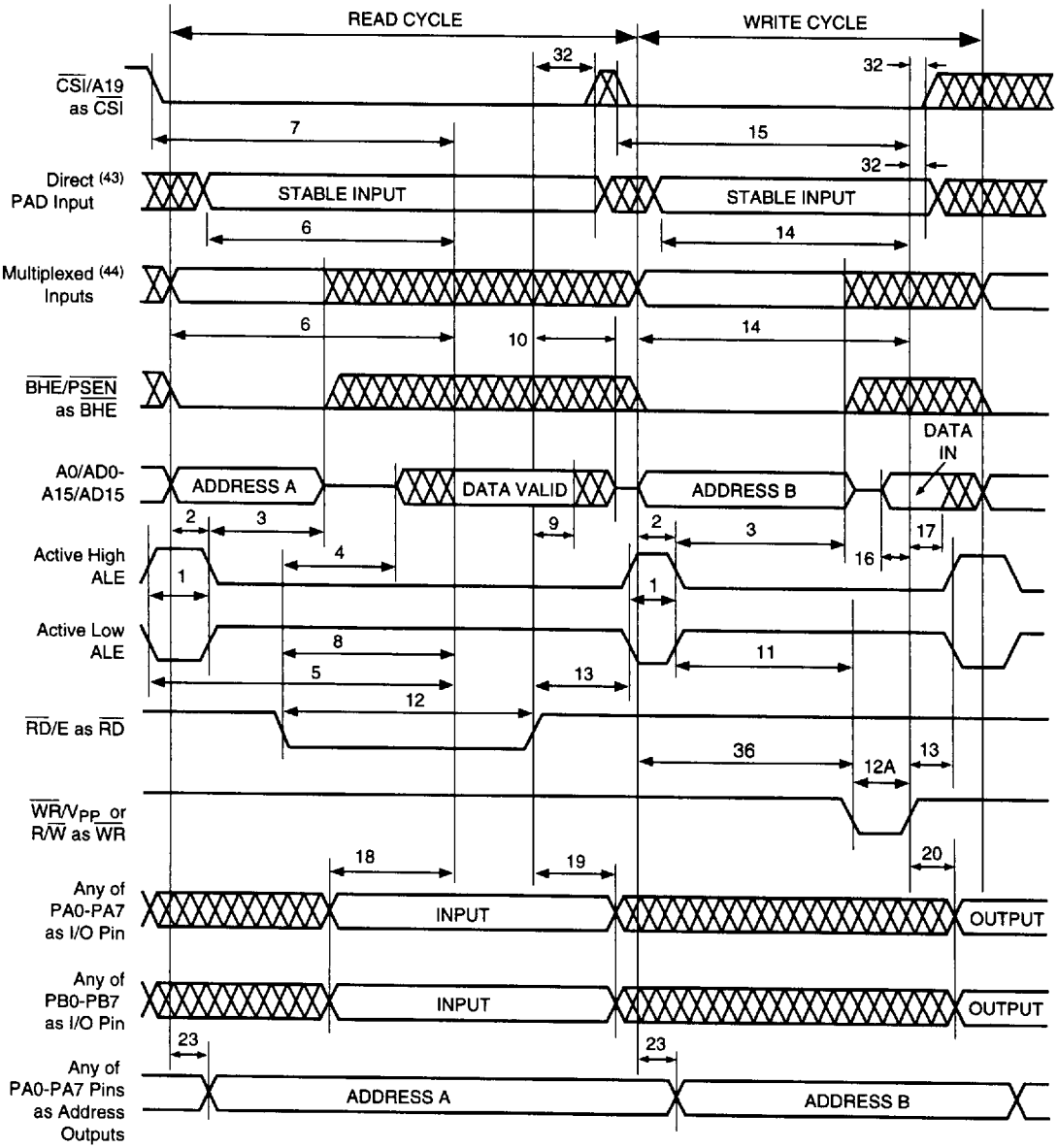
See referenced notes on page 3-63.

Figure 26. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1 (ZPSD3X2/3X3/3X4R)



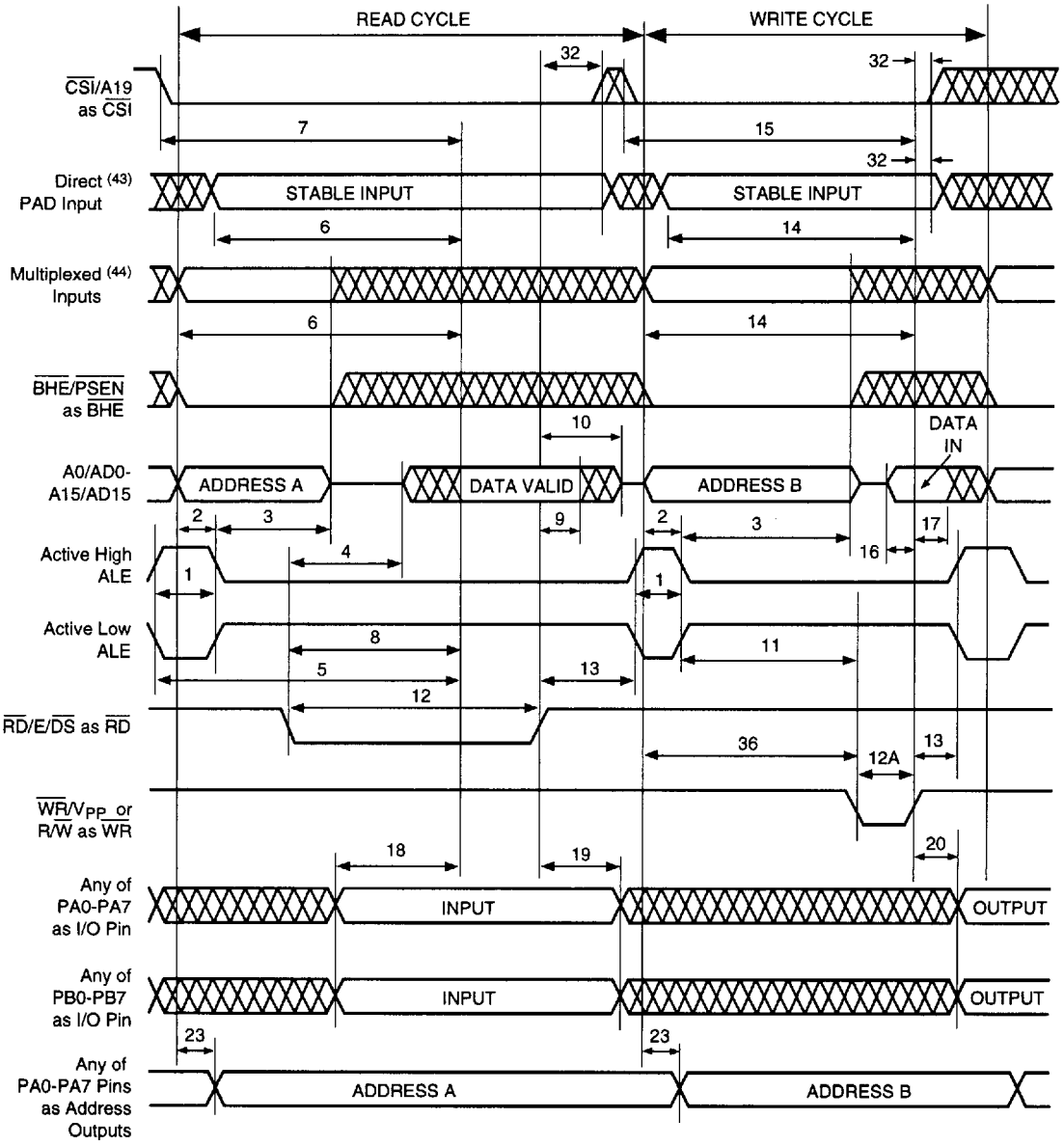
See referenced notes on page 3-63.

Figure 27. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0 (ZPSD3X1)



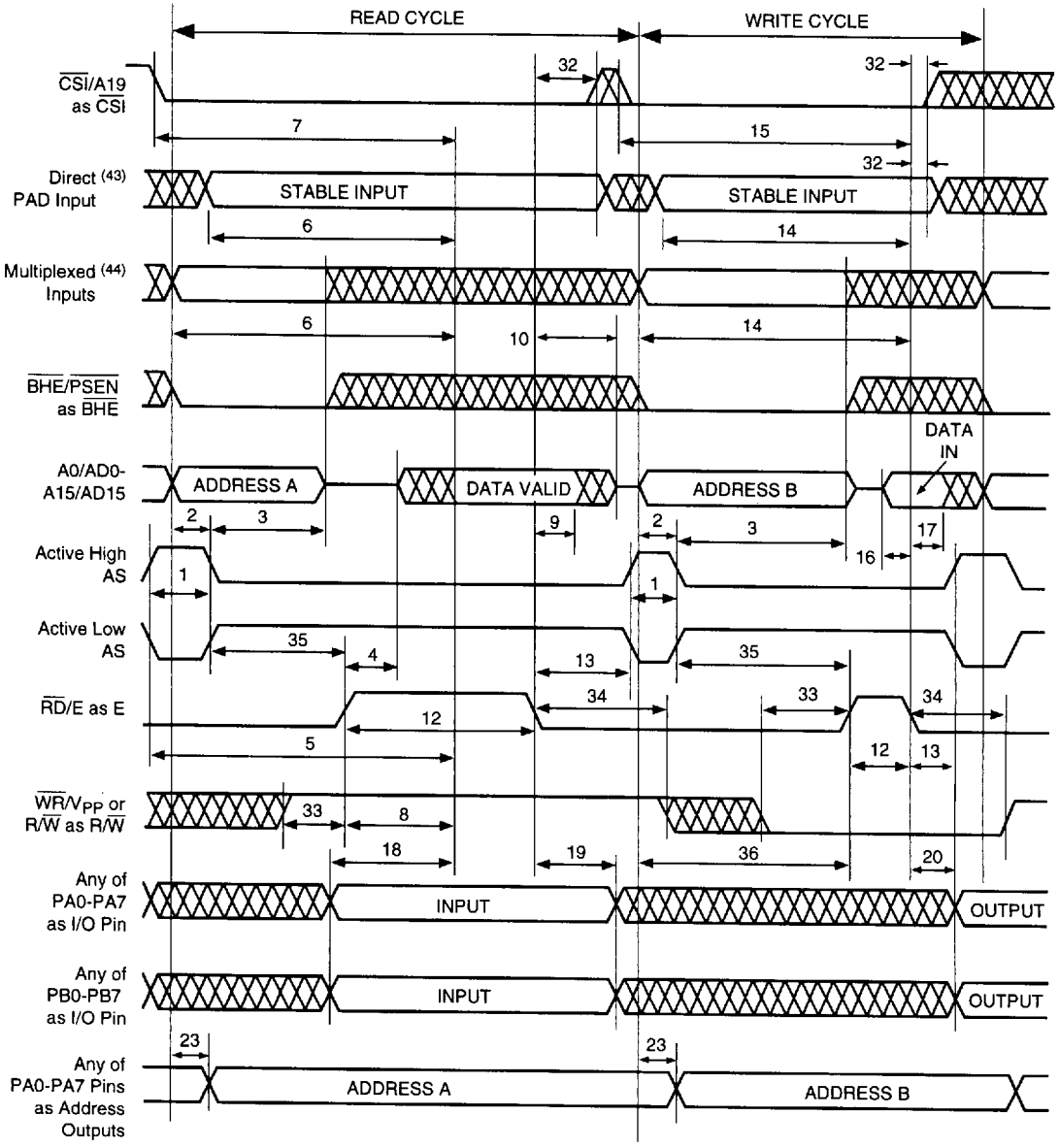
See referenced notes on page 3-63.

Figure 28. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0 (ZPSD3X2/3X3/3X4R)



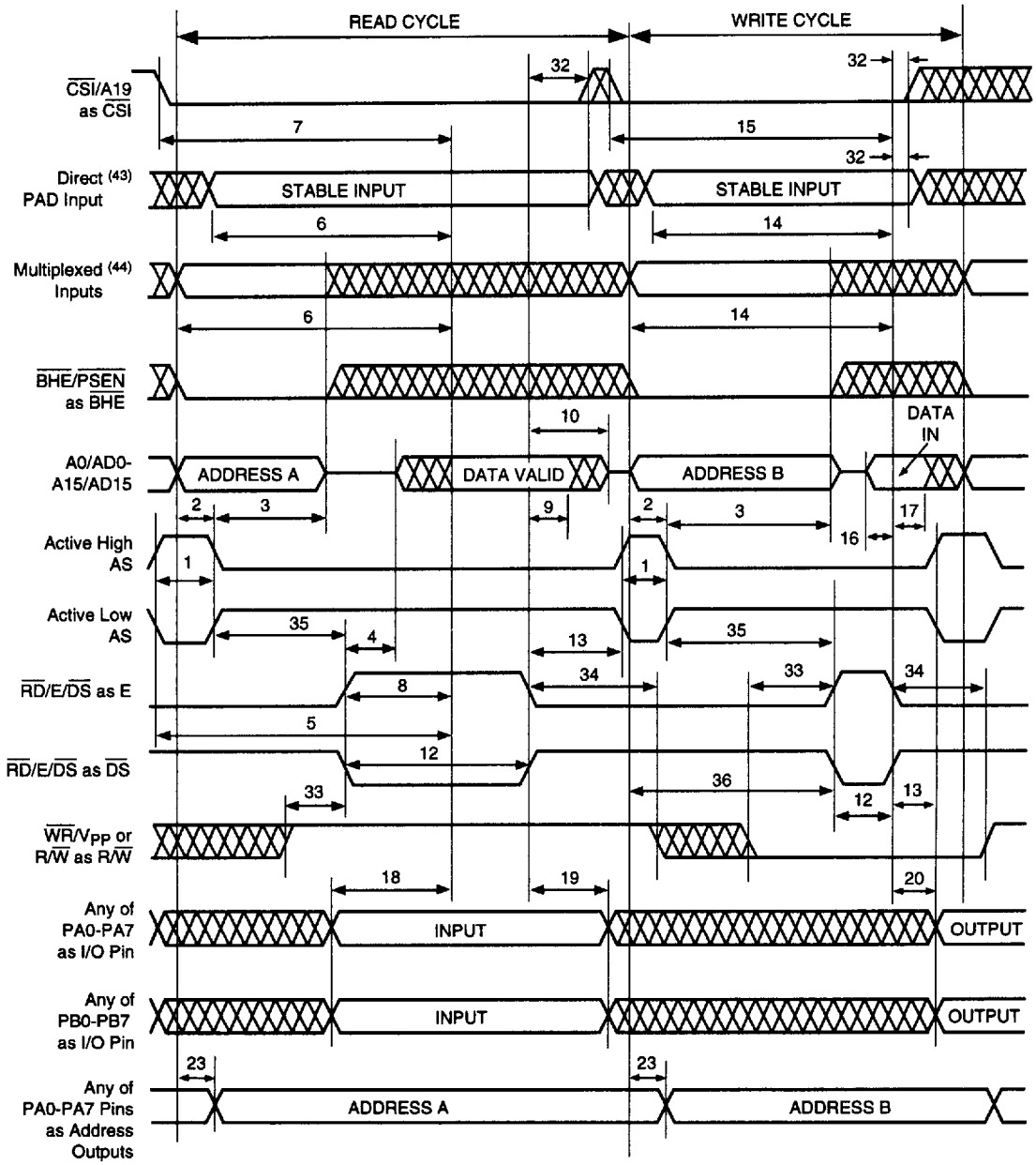
See referenced notes on page 3-63.

Figure 29. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1 (ZPSD3X1)



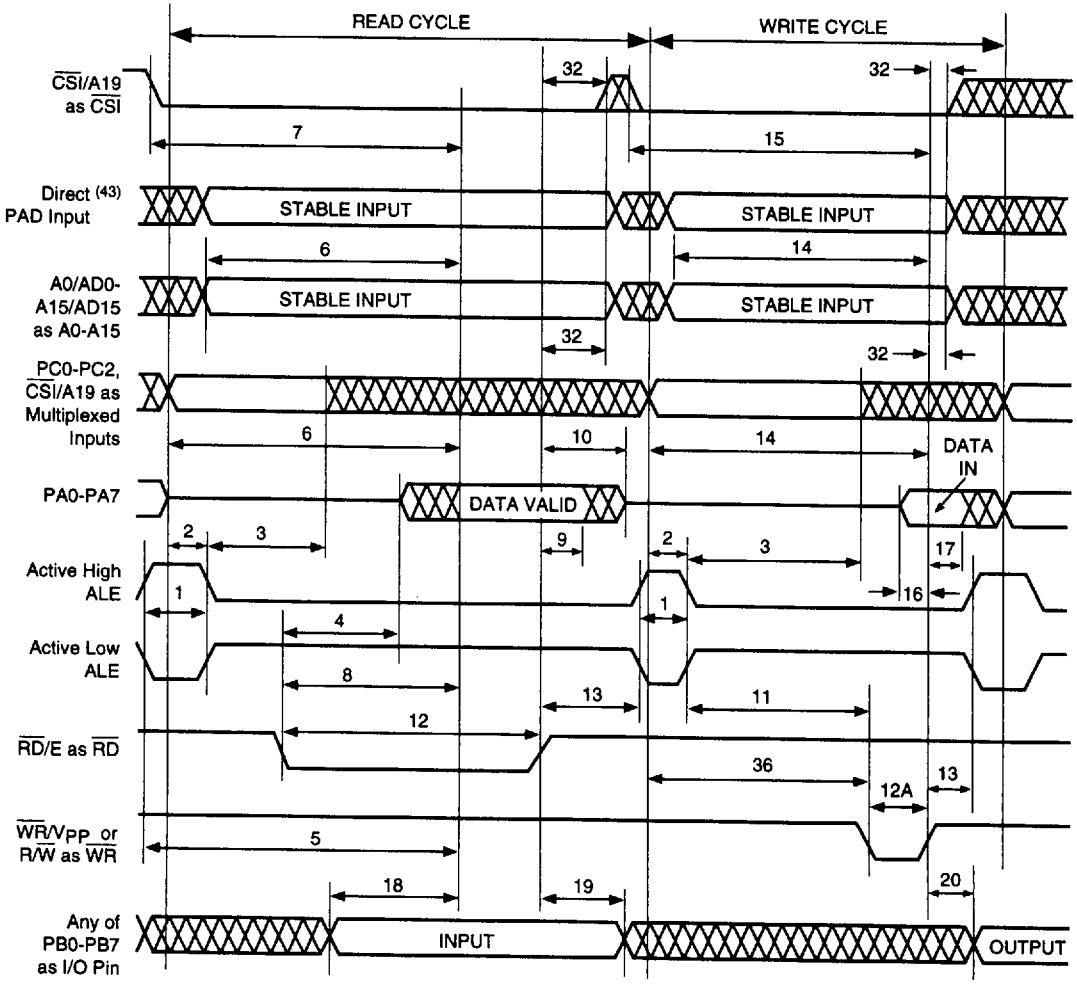
See referenced notes on page 3-63.

Figure 30. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1 (ZPSD3X2/3X3/3X4R)



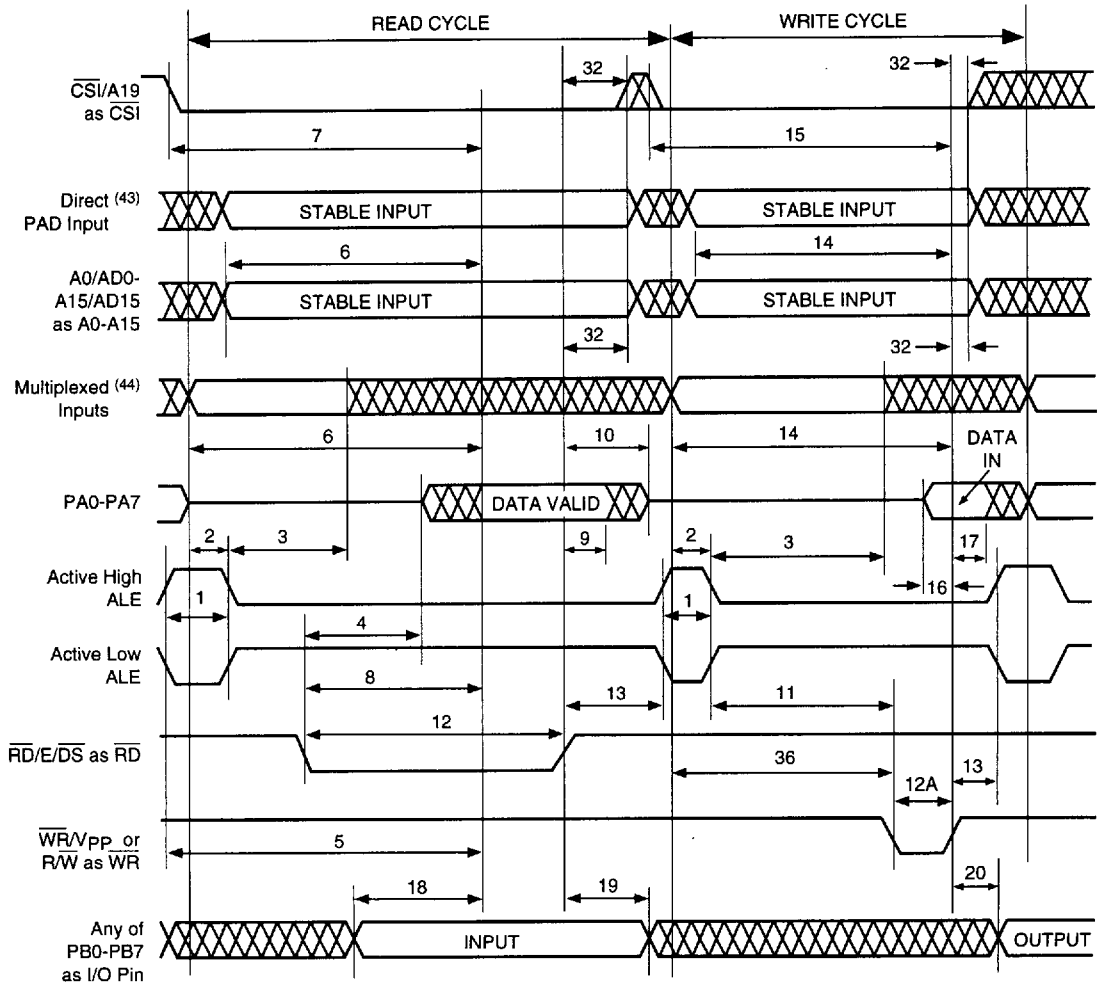
See referenced notes on page 3-63.

Figure 31. Timing of 8-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0 (ZPSD3X1)



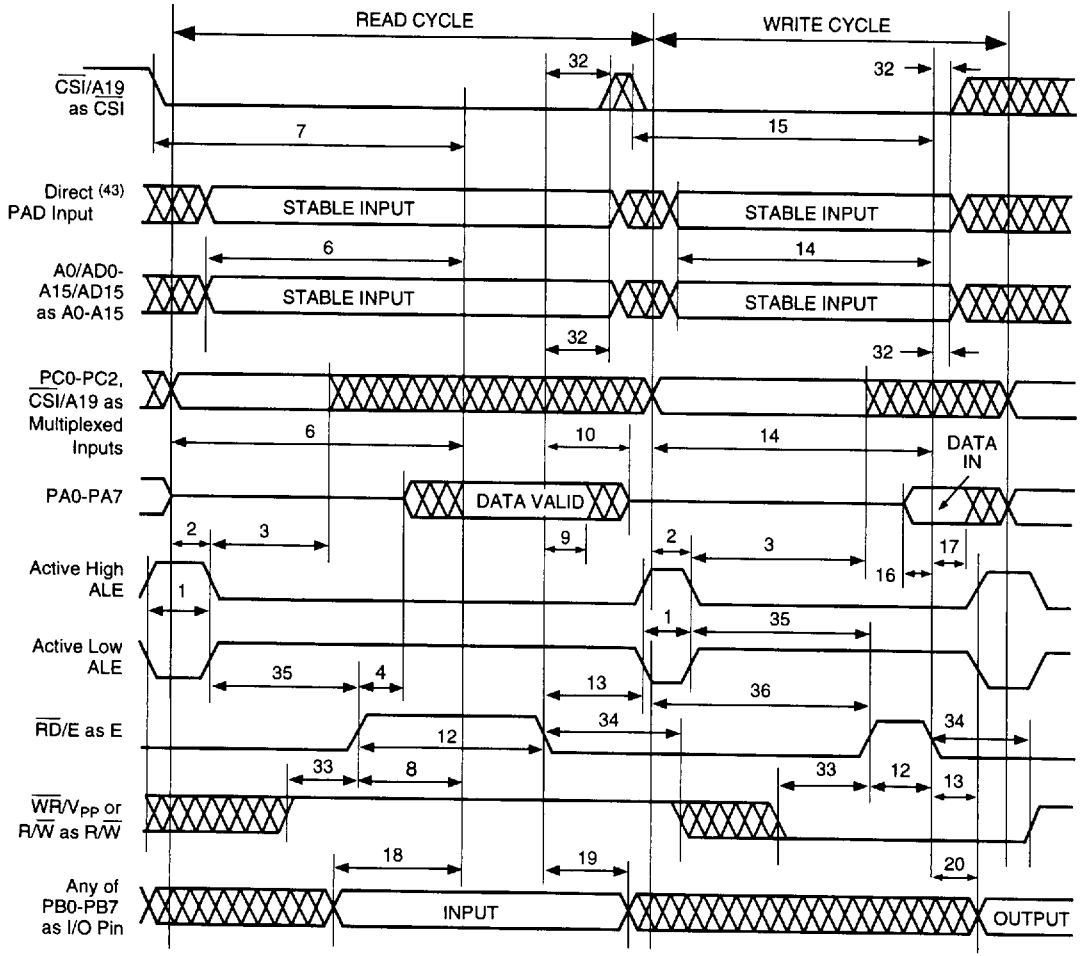
See referenced notes on page 3-63.

Figure 32. Timing of 8-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0 (ZPSD3X2/3X3/3X4R)



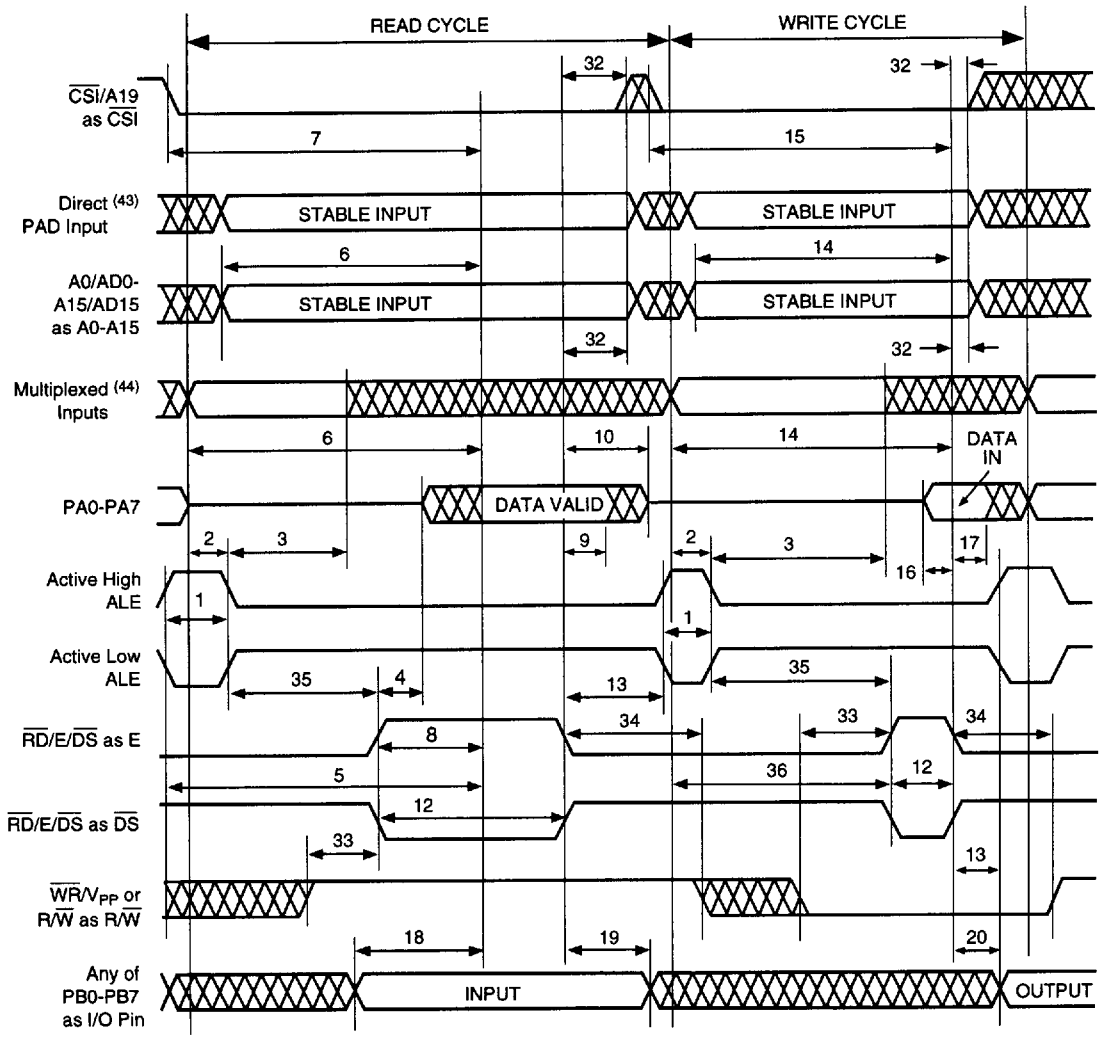
See referenced notes on page 3-63.

Figure 33. Timing of 8-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1 (ZPSD3X1)



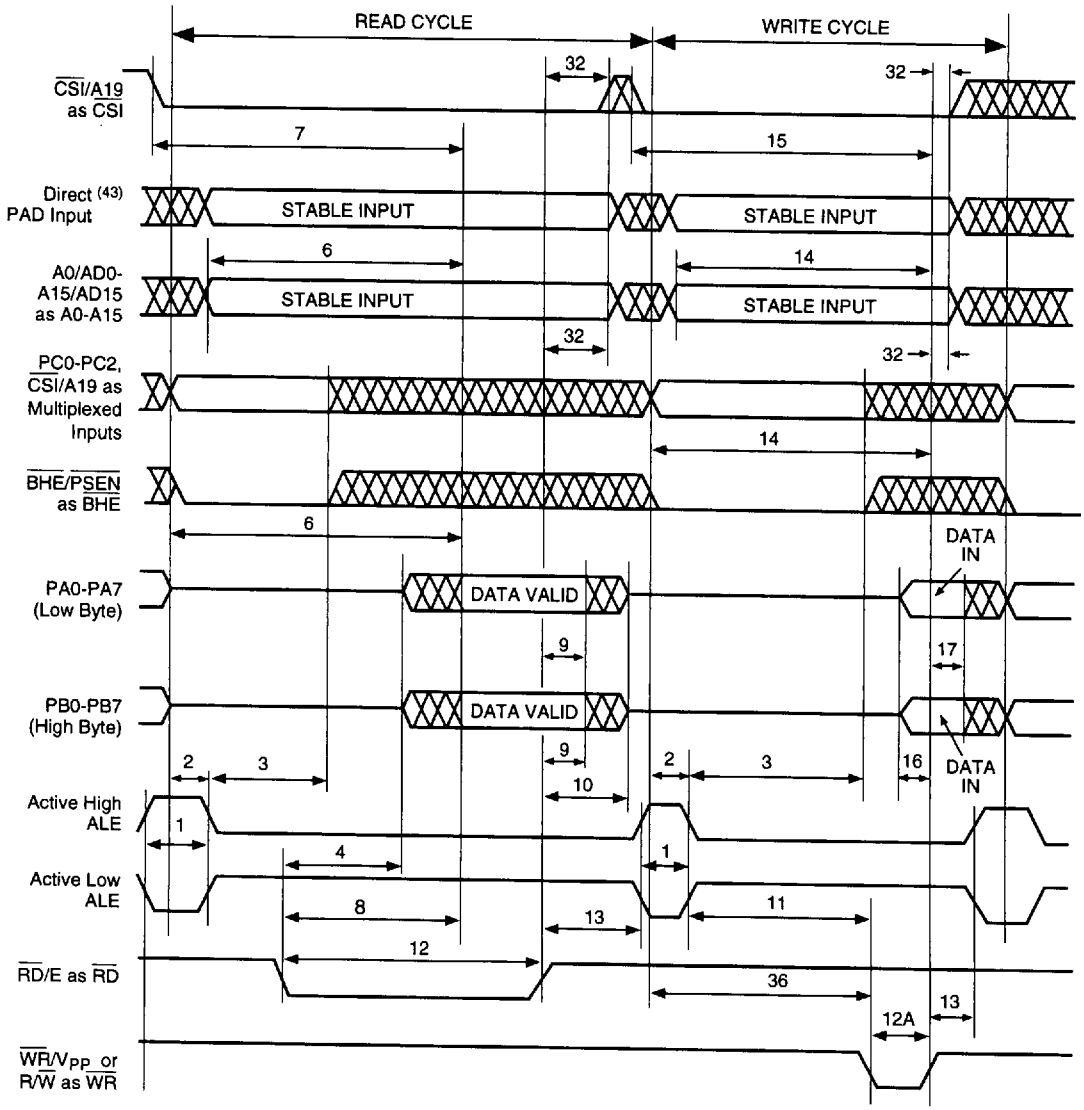
See referenced notes on page 3-63.

Figure 34. Timing of 8-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1 (ZPSD3X2/3X3/3X4R)



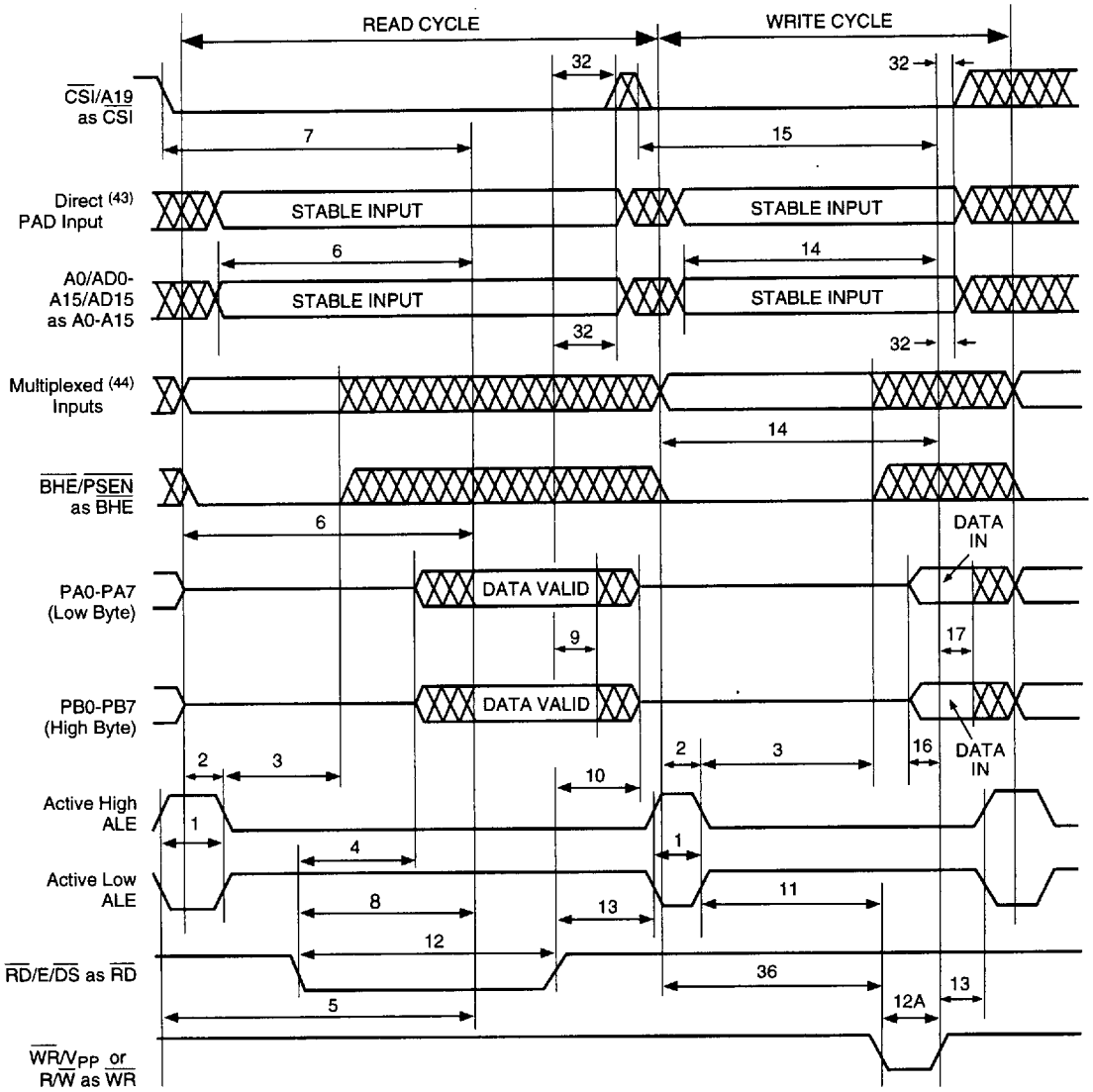
See referenced notes on page 3-63.

Figure 35. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0 (ZPSD3X1)



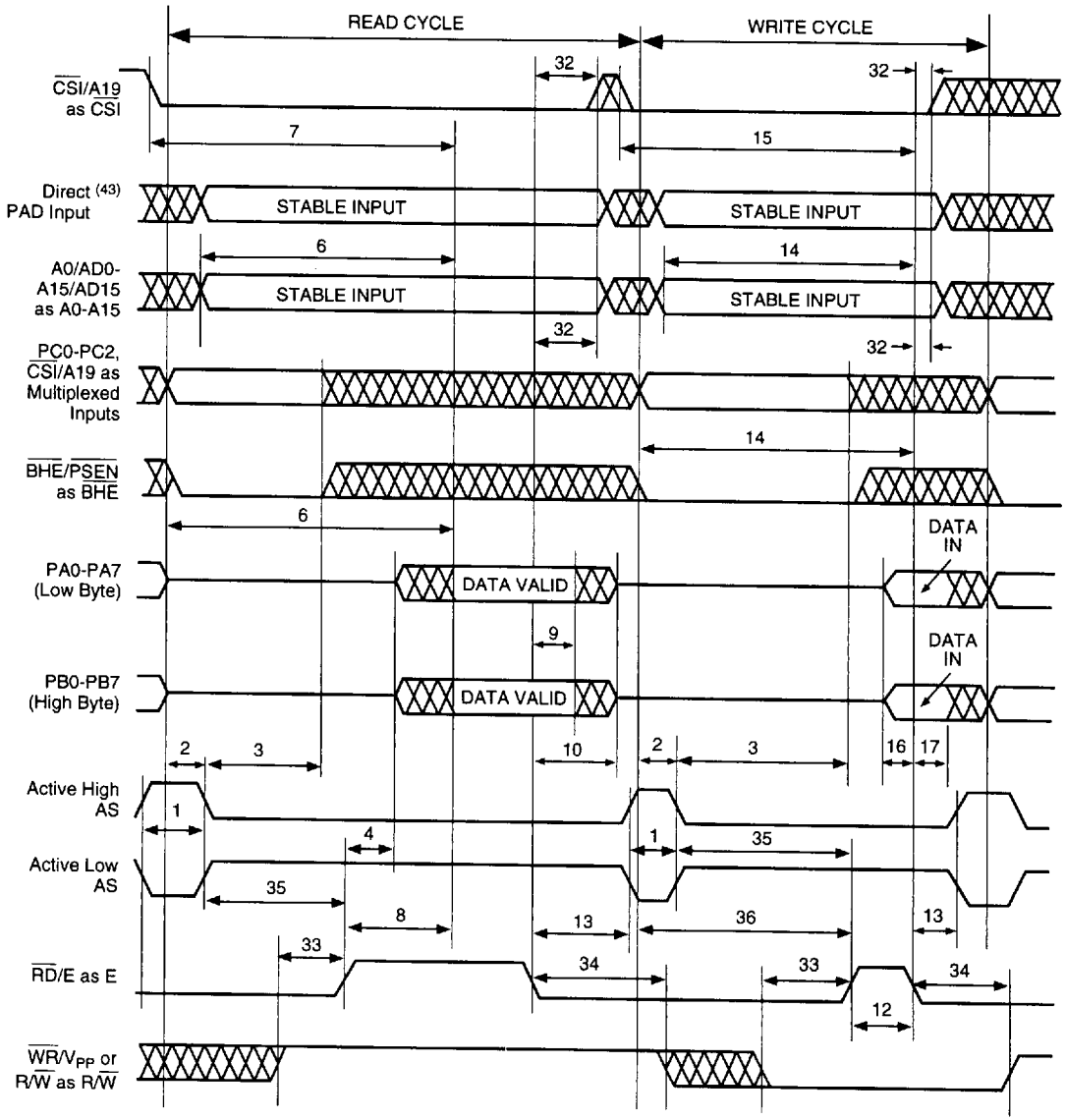
See referenced notes on page 3-63.

Figure 36. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0 (ZPSD3X2/3X3/3X4R)



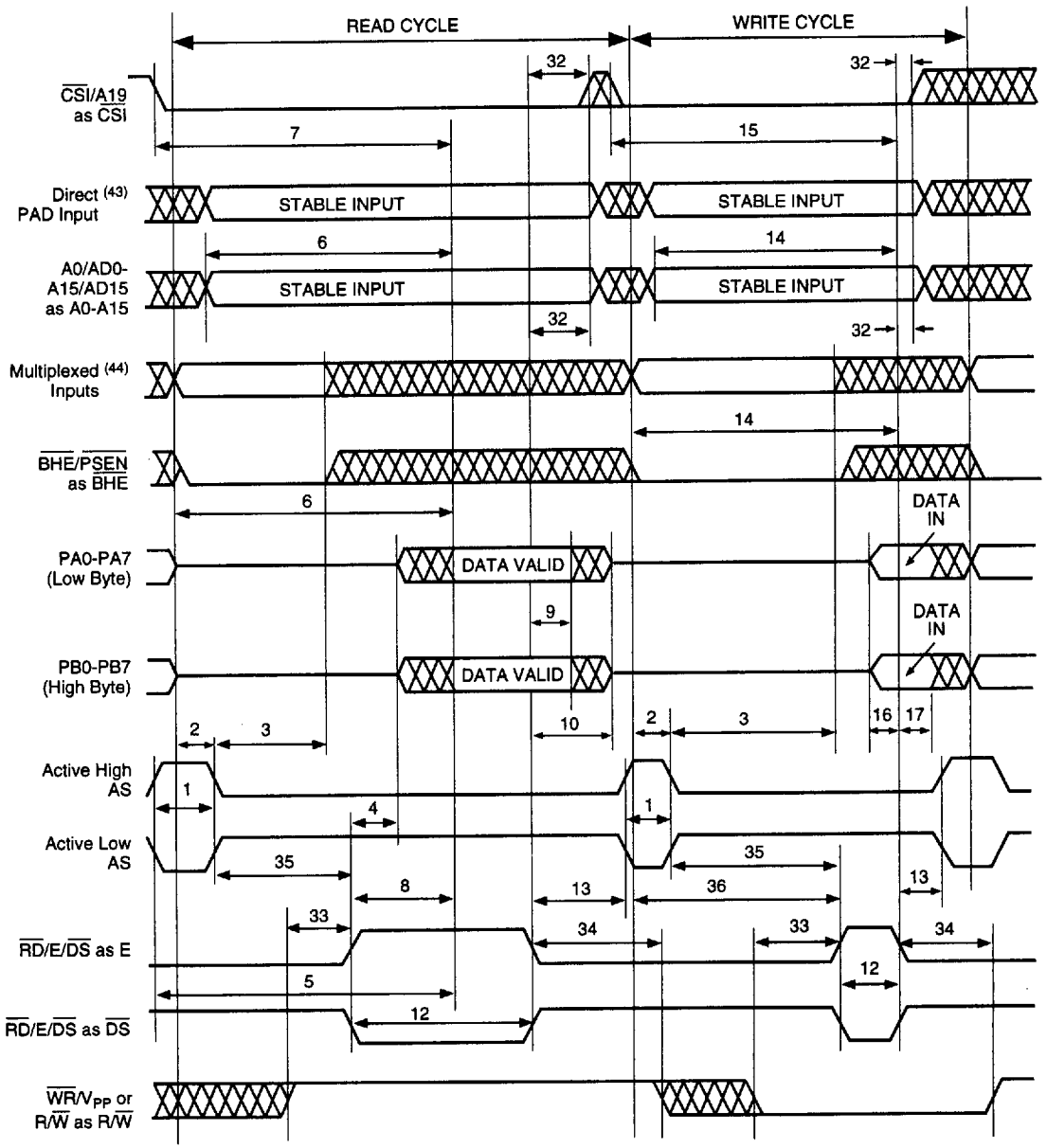
See referenced notes on page 3-63.

Figure 37. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1 (ZPSD3X1)



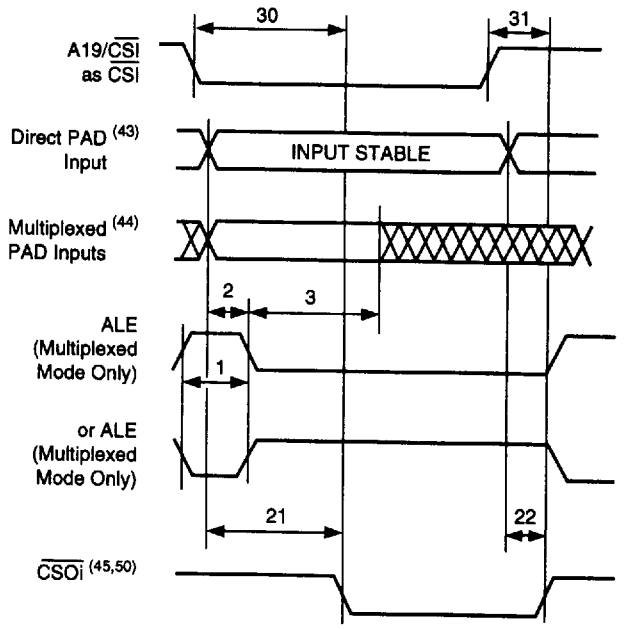
See referenced notes on page 3-63.

Figure 38. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1 (ZPSD3X2/3X3/3X4R)



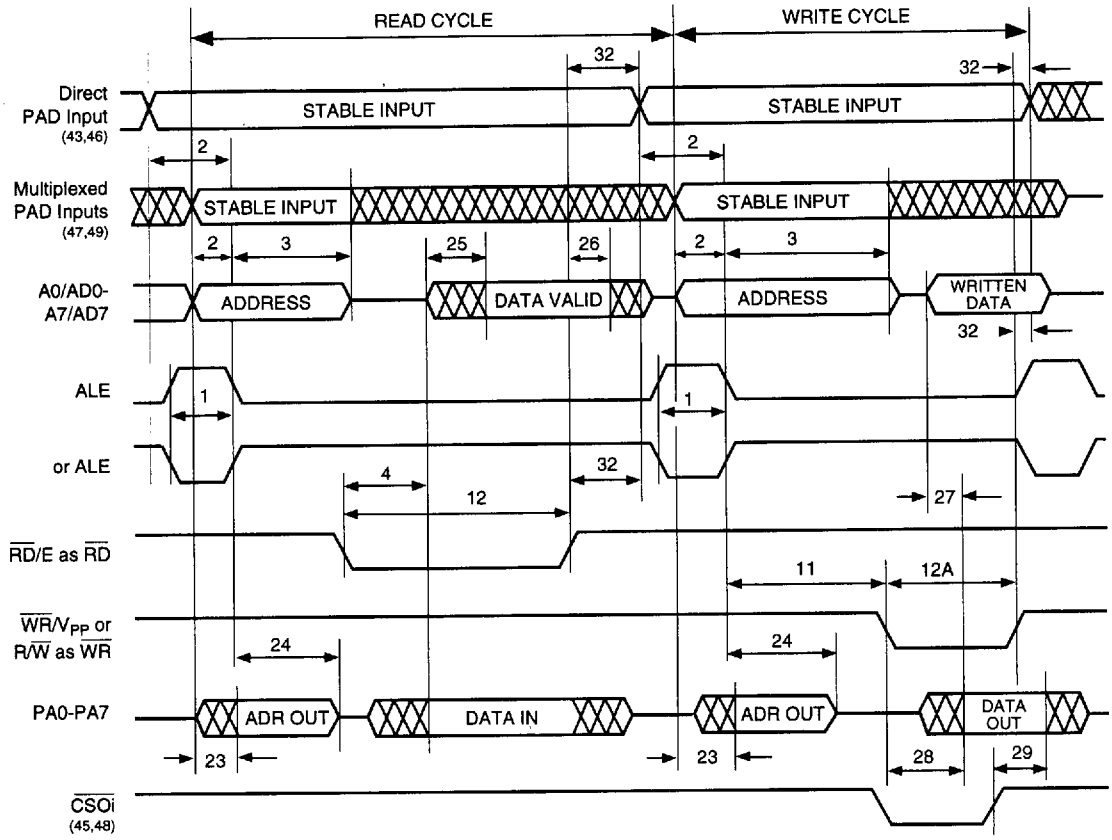
See referenced notes on page 3-63.

Figure 39. Chip-Select Output Timing (ZPSD30X)



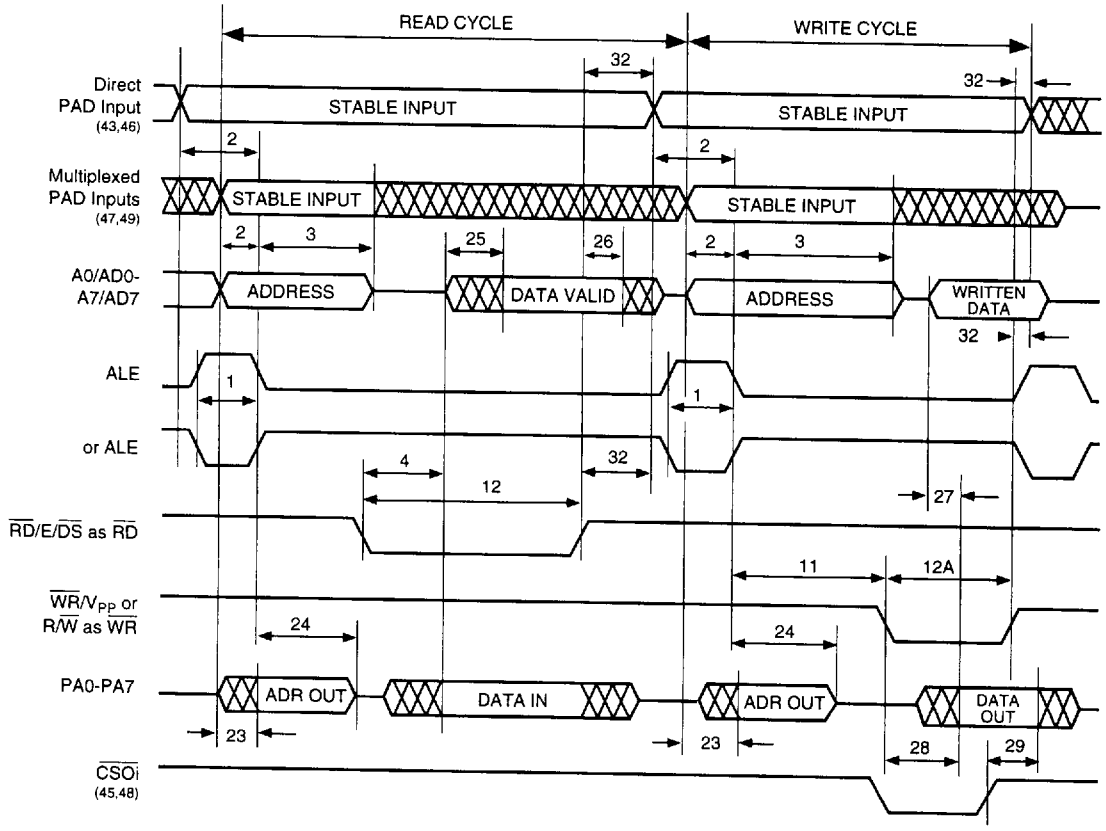
See referenced notes on page 3-63.

Figure 40. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0 (ZPSD3X1)



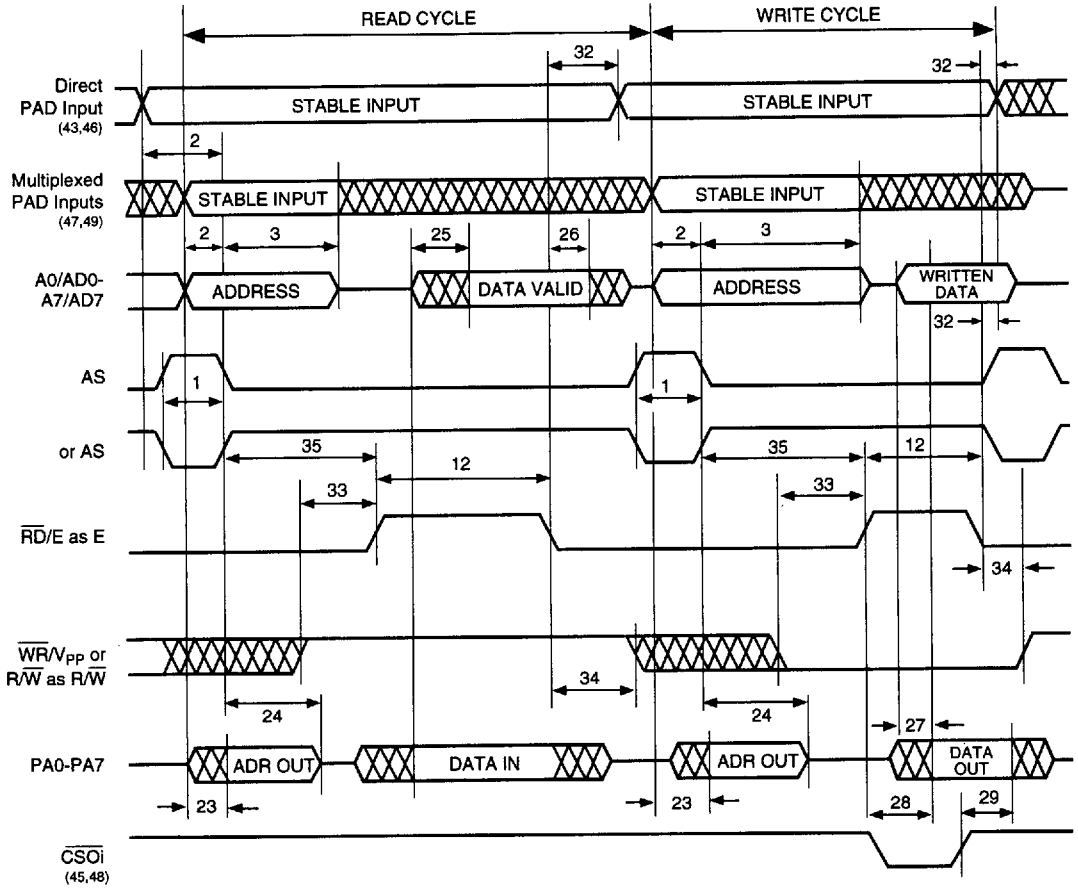
See referenced notes on page 3-63.

Figure 41. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0 (ZPSD3X2/3X3/3X4R)



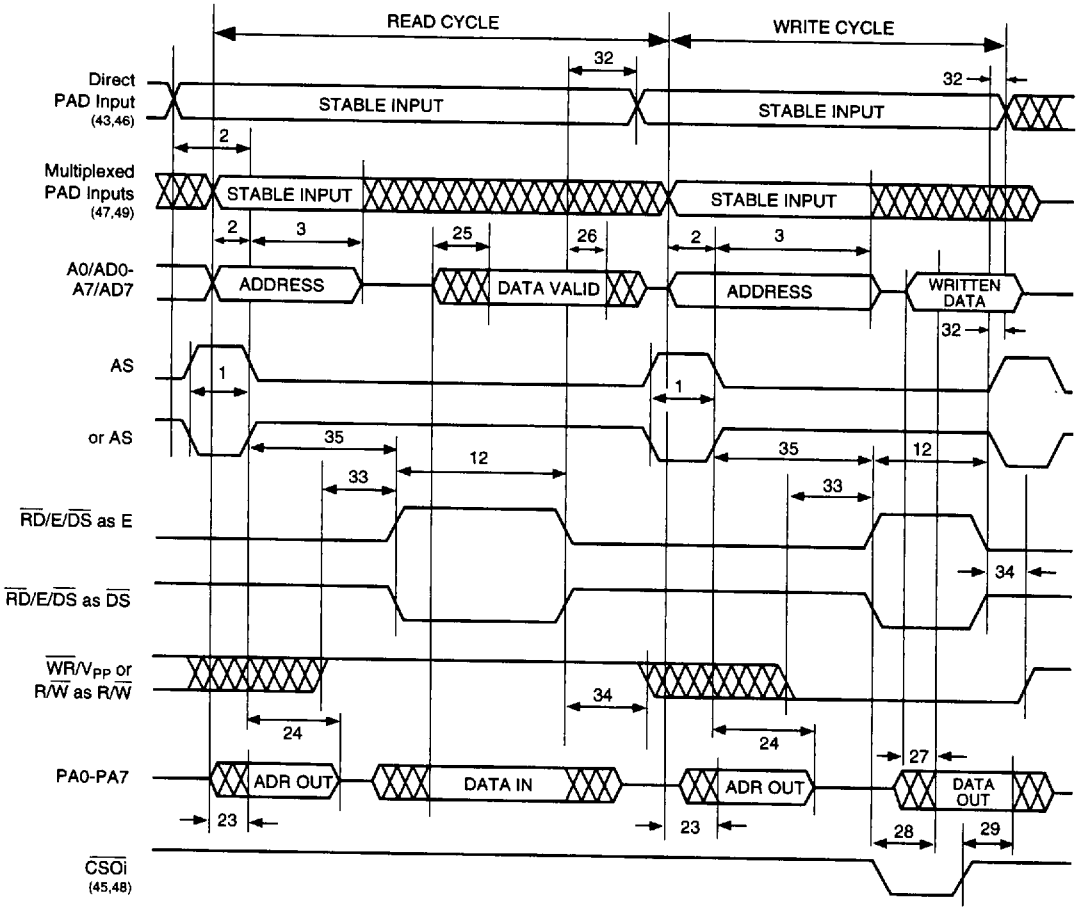
See referenced notes on page 3-63.

Figure 42. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1 (ZPSD3X1)



See referenced notes on page 3-63.

Figure 43. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1 (ZPSD3X2/3X3/3X4R)



Notes for Timing Diagrams

43. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E/DS, WR or R/W, transparent PC0–PC2, ALE in non-multiplexed modes.
44. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
45. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
46. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
47. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
48. The write operation signals are included in the CSOi expression.
49. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
50. CSOi product terms can include any of the PAD input signals shown in Figure 4, except for reset and CSI.

Table 14. Pin Capacitance[51]

Symbol	Parameter	Conditions	Typical[52]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 51. This parameter is only sampled and is not 100% tested.
52. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 44. AC Testing Input/Output Waveform

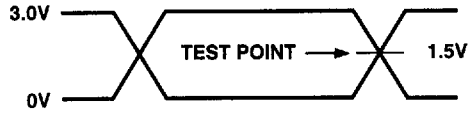


Figure 44a. AC Testing Input/Output Waveform (ZPSD3XX V Versions)

Figure 45. AC Testing Load Circuit

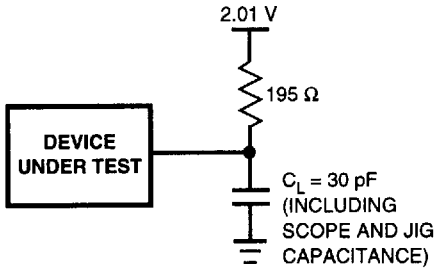
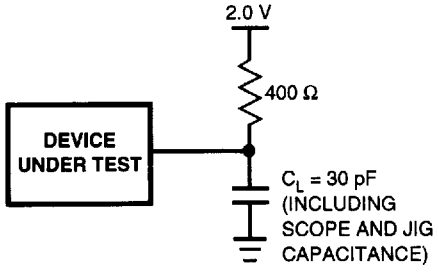


Figure 45a. AC Testing Load Circuit (ZPSD3XX V Versions)



Erasure and Programming

To clear all locations of their programmed contents, expose the window packaged device to an ultra-violet light source. A dosage of 30 W second/cm^2 is required (40 W second/cm^2 for ZPSD3XXV versions). This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 40 to 45 minutes (55 to 60 minutes for ZPSD3XXV versions). The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The ZPSD3XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the ZPSD3XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.