

3.3 Volt, Byte Alterable E²PROM

FEATURES

- Access Time: 70, 90, 120, 150ns
- Simple Byte and Page Write
 - Single 3.3V±10% supply
 - No external high voltages or V_{PP} control circuits
 - Self-timed
 - no erase before write
 - no complex programming algorithms
 - no overerase problem
- Low Power CMOS
 - Active: 20mA
 - Standby: 20µA
- Software Data Protection
 - Protects data against system level inadvertent writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
 - Endurance: 100,000 write cycles
 - Data retention: 100 Years
- Early End of Write Detection
 - DATA polling
 - Toggle bit polling

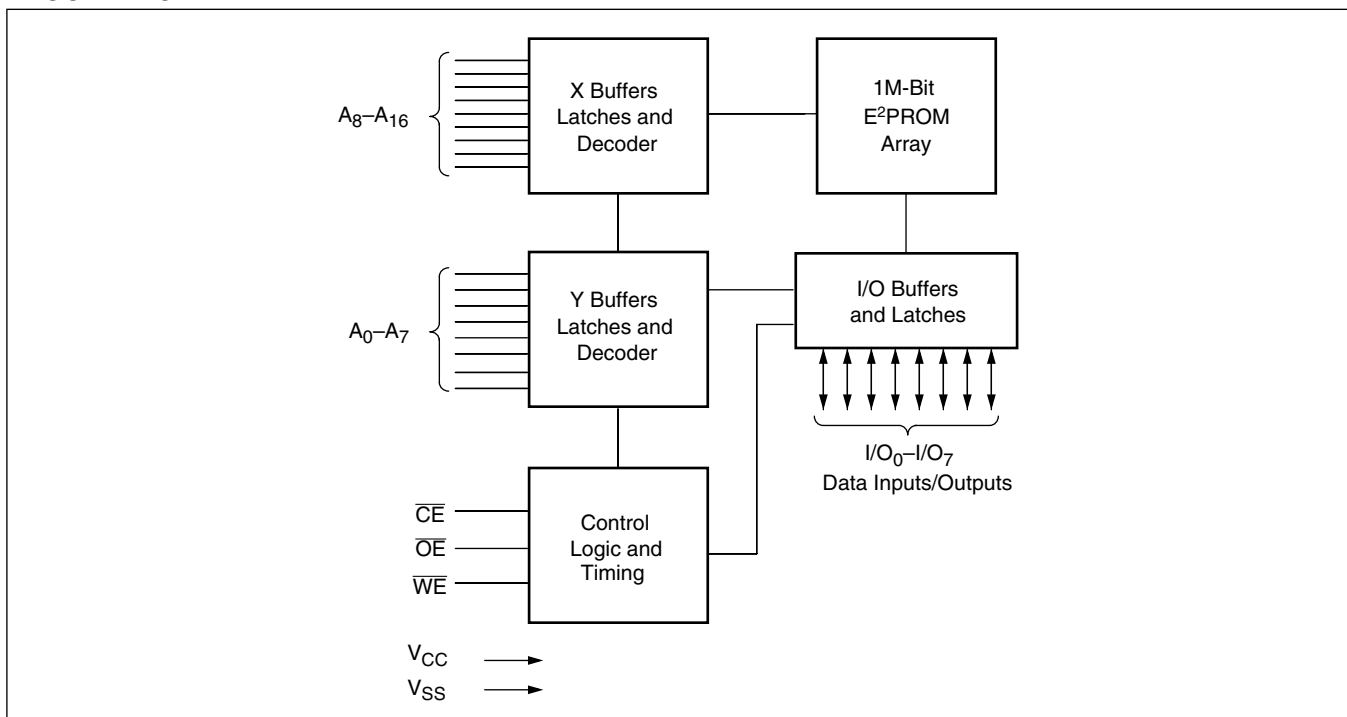
DESCRIPTION

The Xicor X28LV010 is a 128K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28LV010 requires a single voltage supply. The X28LV010 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard EPROMs.

The X28LV010 supports a 256-byte page write operation, effectively providing a 12µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28LV010 also features DATA Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28LV010 supports Software Data Protection option.

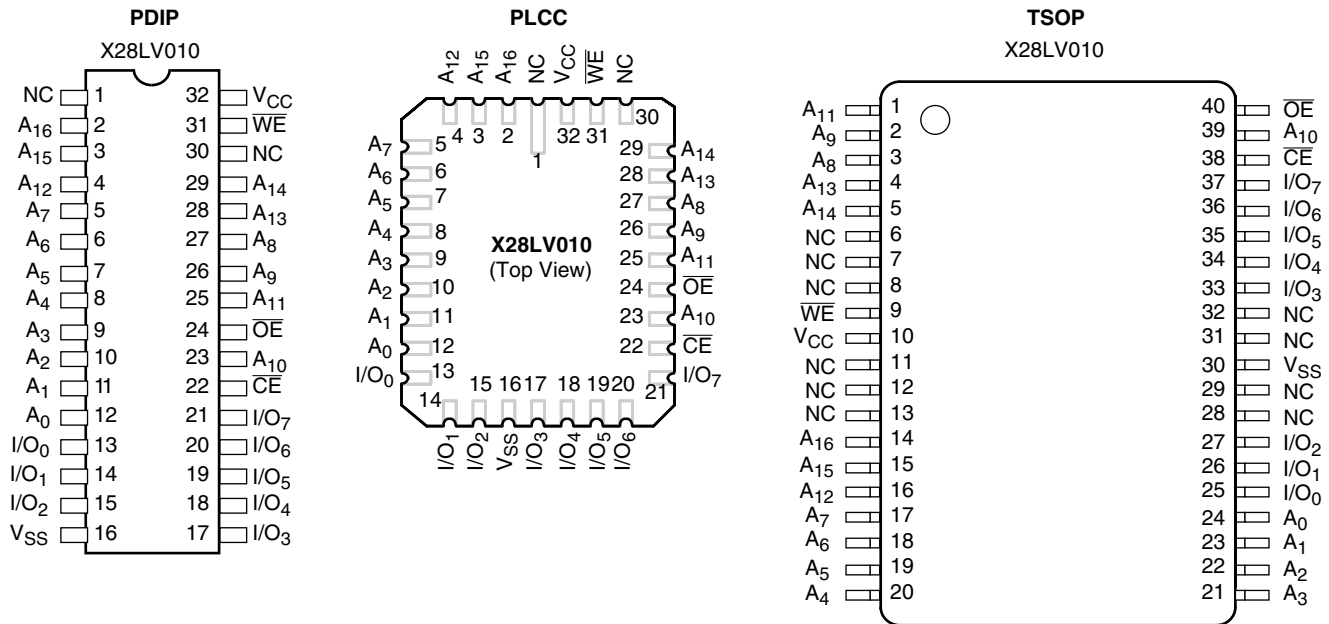
Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

BLOCK DIAGRAM



X28LV010

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Addresses (A₀–A₁₆)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (\overline{CE})

The Chip Enable input must be LOW to enable all read/write operations. When \overline{CE} is HIGH, power consumption is reduced.

Output Enable (\overline{OE})

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O₀–I/O₇)

Data is written to or read from the X28LV010 through the I/O pins.

Write Enable (\overline{WE})

The Write Enable input controls the writing of data to the X28LV010.

PIN NAMES

Symbol	Description
A ₀ –A ₁₆	Address Inputs
I/O ₀ –I/O ₇	Data Input/Output
\overline{WE}	Write Enable
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
V _{CC}	+3.3V
V _{SS}	Ground
NC	No Connect

DEVICE OPERATION

Read

Read operations are initiated by both \overline{OE} and \overline{CE} LOW. The read operation is terminated by either \overline{CE} or \overline{OE} returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either \overline{OE} or \overline{CE} is HIGH.

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Write

Write operations are initiated when both \overline{CE} and \overline{WE} are LOW and \overline{OE} is HIGH. The X28LV010 supports both a \overline{CE} and \overline{WE} controlled write cycle. That is, the address is latched by the falling edge of either \overline{CE} or \overline{WE} , whichever occurs last. Similarly, the data is latched internally by the rising edge of either \overline{CE} or \overline{WE} , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

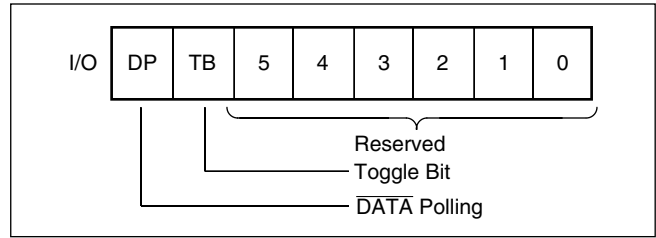
The page write feature of the X28LV010 allows the entire memory to be written in 2.5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28LV010 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_8 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty five bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the \overline{WE} HIGH to LOW transition, must begin within 100 μ s of the falling edge of the preceding \overline{WE} . If a subsequent \overline{WE} HIGH to LOW transition is not detected within 100 μ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μ s.

Write Operation Status Bits

The X28LV010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



DATA Polling (I/O_7)

The X28LV010 features \overline{DATA} Polling as a method to indicate to the host system that the byte write or page write cycle has completed. \overline{DATA} Polling allows a simple bit test operation to determine the status of the X28LV010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28LV010 is in the protected state and an illegal write operation is attempted \overline{DATA} Polling will not operate.

Toggle Bit (I/O_6)

The X28LV010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

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DATA Polling I/O₇

Figure 2. DATA Polling Bus Sequence

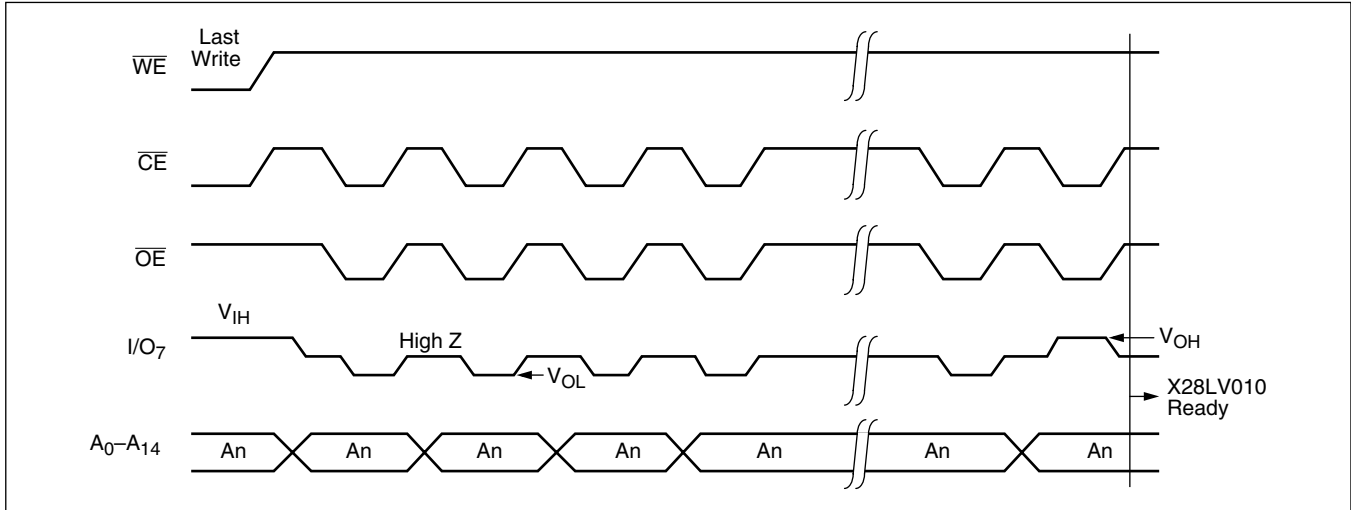
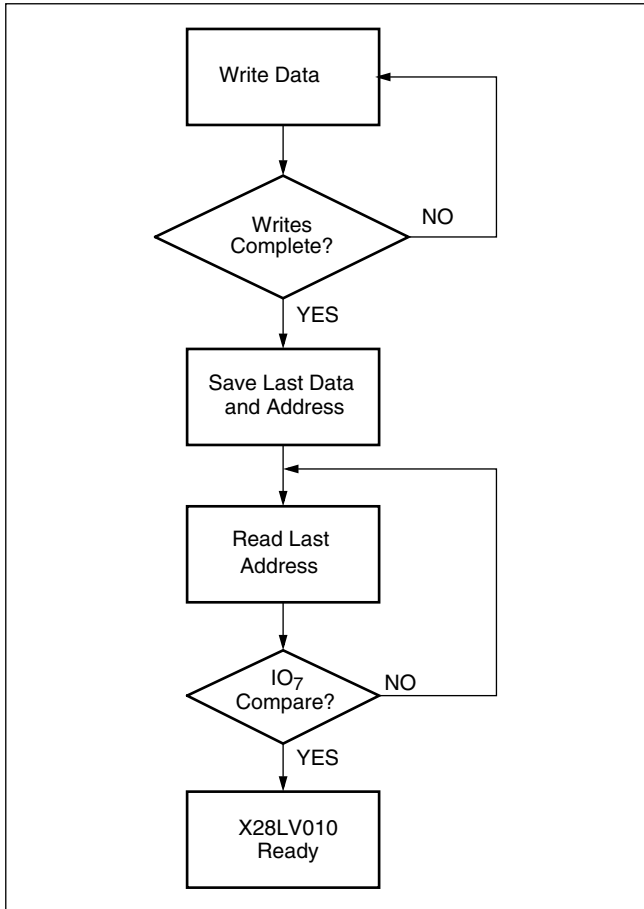


Figure 3. DATA Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28LV010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

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The Toggle Bit I/O₆

Figure 4. Toggle Bit Bus Sequence

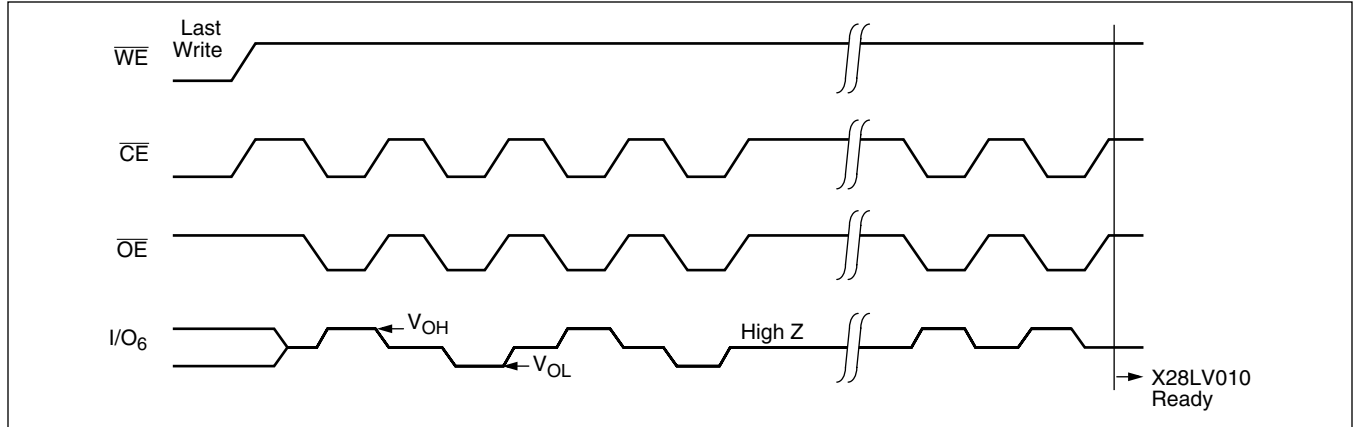
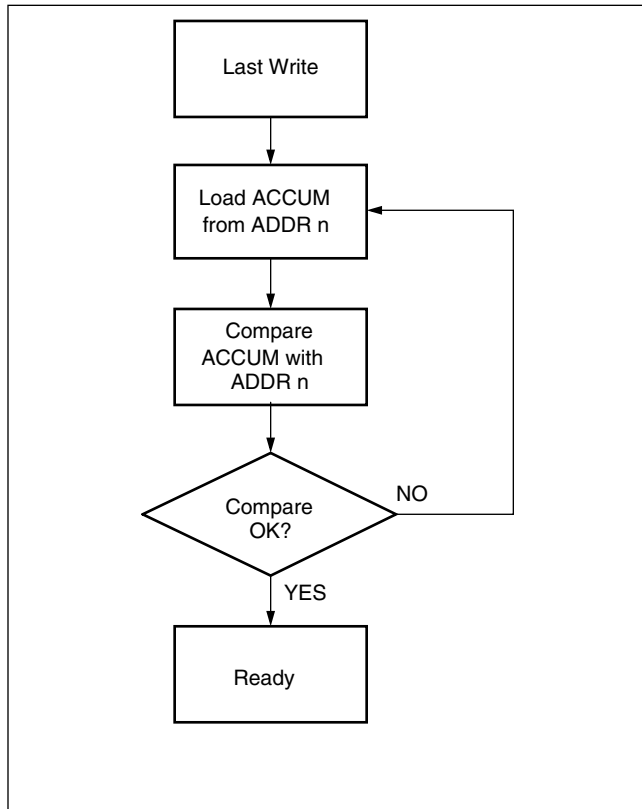


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement \overline{DATA} Polling. This can be especially helpful in an array com-

prised of multiple X28LV010 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28LV010 provides three hardware features that protect nonvolatile data from inadvertent writes.

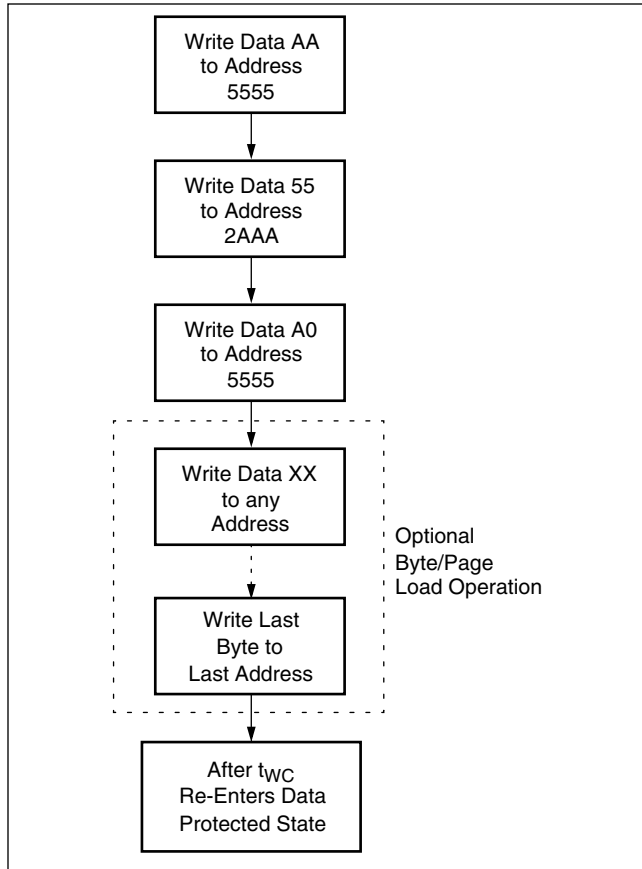
- Noise Protection—A \overline{WE} pulse less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq 2.5V$.
- Write inhibit—Holding either \overline{OE} LOW, \overline{WE} HIGH, or \overline{CE} HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28LV010 offers a software controlled data protection feature. The X28LV010 is shipped from Xicor with the software data protection NOT ENABLED; that is the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

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Figure 7. Write Sequence for Software Data Protection

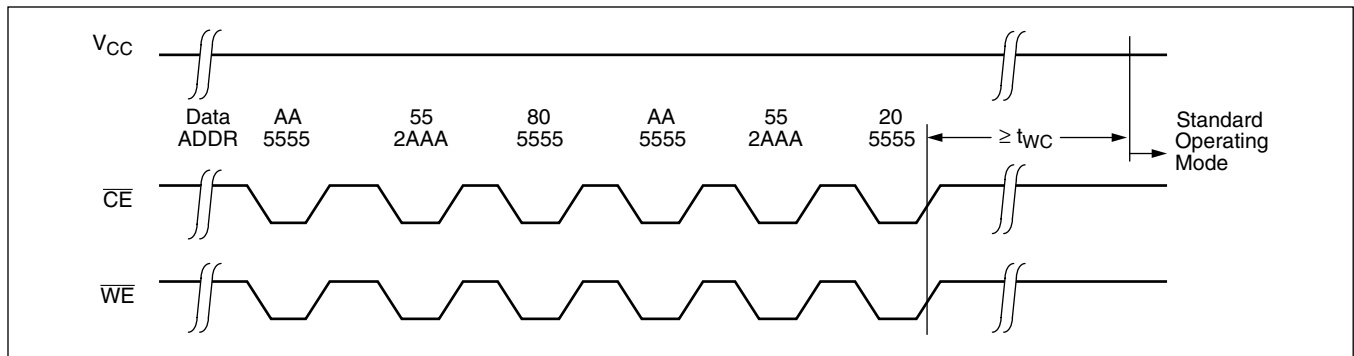


Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28LV010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28LV010 will be write protected during power-down and after any subsequent power-up. The state of A₁₅ and A₁₆ while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

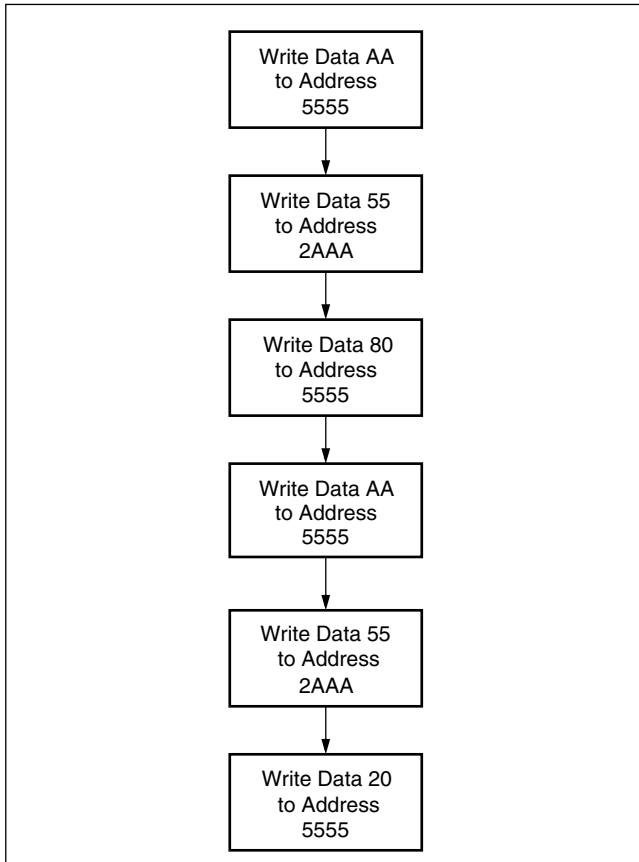
Resetting Software Data Protection

Figure 8. Reset Software Data Protection Timing Sequence



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Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC} , the X28LV010 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

Because the X28LV010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that \overline{CE} be decoded from the address bus and be used as the primary device selection input. Both \overline{OE} and \overline{WE} would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28LV010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling \overline{CE} will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μ F high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μ F electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage drop caused by the inductive effects of the PC board traces.

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ABSOLUTE MAXIMUM RATINGS

Temperature under bias
 X28LV010 -10°C to +85°C
 X28LV010I -65°C to +135°C
 Storage temperature -65°C to +150°C
 Voltage on any input pins (including
 NC pins) with respect to ground -0.5 to 6.25V
 Voltage on any output pins with
 respect to ground -0.5 to $V_{CC} + 0.5V$
 D.C. output current 5mA
 Lead temperature (soldering, 10 seconds) 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

Supply Voltage	Limits
X28LV010	3.3V ±10%

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		20	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 10MHz
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)	Com.	20	μA	$\overline{CE} = V_{CC} - 0.3V$, $\overline{OE} = V_{IL}$, All I/O's = Open, Other Inputs = V_{CC}
		Ind.	50	μA	
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = V_{SS}$ to V_{CC} , $\overline{CE} = V_{IH}$
$V_{IL}^{(1)}$	Input LOW Voltage	0.5	0.8	V	
$V_{IH}^{(1)}$	Input HIGH Voltage	2	$V_{CC} + 0.3$	V	
V_{OL}	Output LOW Voltage		0.4	V	$I_{OL} = 2.1mA$
V_{OH}	Output HIGH Voltage	2.4		V	$I_{OH} = -400\mu A$

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(2)}$	Power-up to Read Operation	100	μs
$t_{PUW}^{(2)}$	Power-up to Write Operation	5	ms

CAPACITANCE $T_A = +25^\circ C$, $f = 1MHz$, $V_{CC} = 5V$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0V$
$C_{IN}^{(2)}$	Input Capacitance	10	pF	$V_{IN} = 0V$

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ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance ⁽²⁾	10,000		Cycles Per Byte
Endurance ⁽²⁾	100,000		Cycles Per Page
Data Retention ⁽²⁾	100		Years

Notes: (2) This parameter is periodically sampled and not 100% tested.

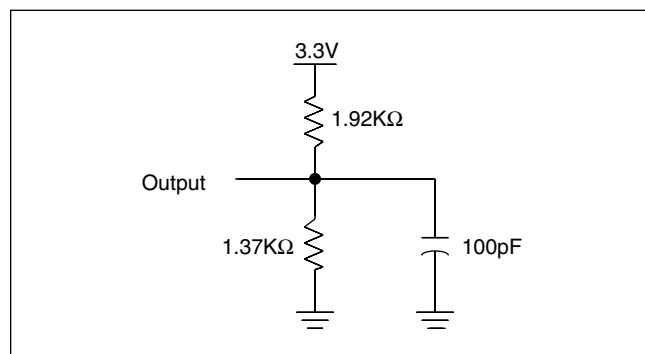
A.C. CONDITIONS OF TEST

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input and output timing levels	1.5V

MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	D _{OUT}	Active
L	H	L	Write	D _{IN}	Active
H	X	X	Standby and write inhibit	High Z	Standby
X	L	X	Write inhibit	—	—
X	X	H	Write inhibit	—	—

EQUIVALENT A.C. LOAD CIRCUIT



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

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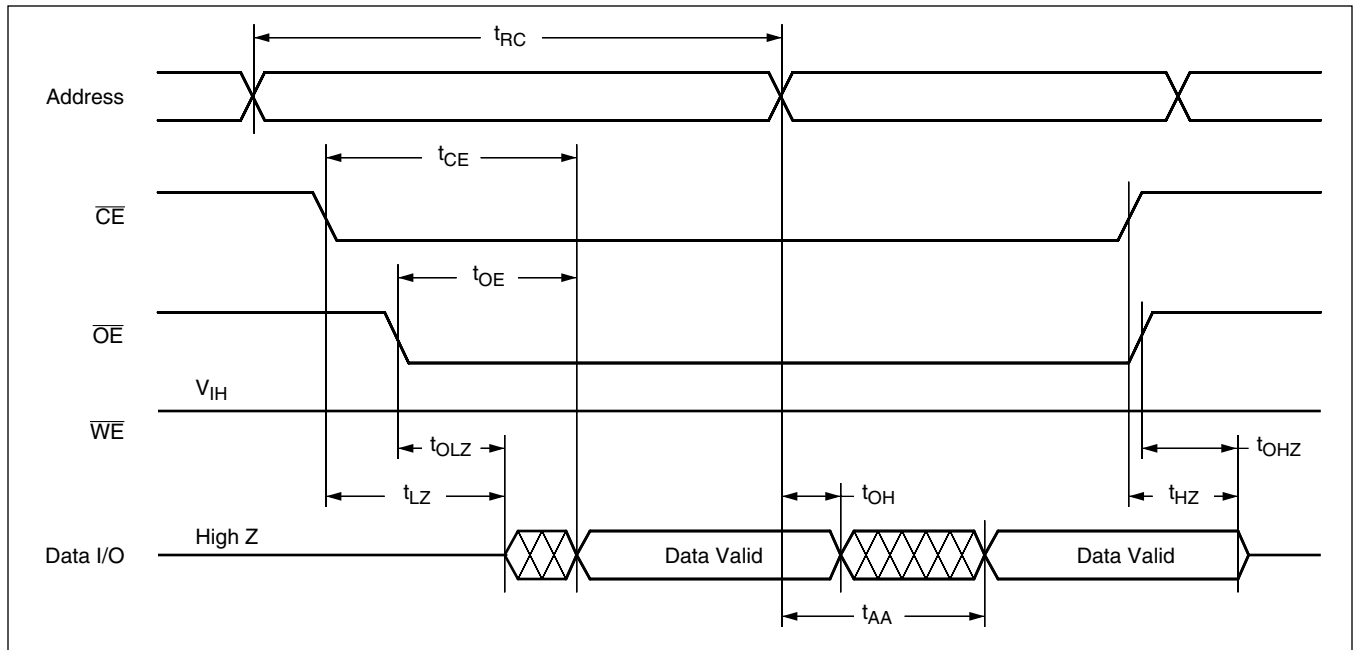
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28LV010-70		X28LV010-90		X28LV010-120		X28LV010-150		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CE}	Chip Enable Access Time		70		90		120		150	ns
t_{AA}	Address Access Time		70		90		120		150	ns
t_{OE}	Output Enable Access Time		35		40		40		40	ns
$t_{LZ}^{(3)}$	\overline{CE} LOW to Active Output	0		0		0		0		ns
$t_{OLZ}^{(3)}$	\overline{OE} LOW to Active Output	0		0		0		0		ns
$t_{HZ}^{(3)}$	\overline{CE} HIGH to High Z Output		40		50		50		50	ns
$t_{OHZ}^{(3)}$	\overline{OE} HIGH to High Z Output		40		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Notes: (3) t_{LZ} min., t_{HZ} , t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with $C_L = 5pF$, from the point when \overline{CE} or \overline{OE} return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Read Cycle



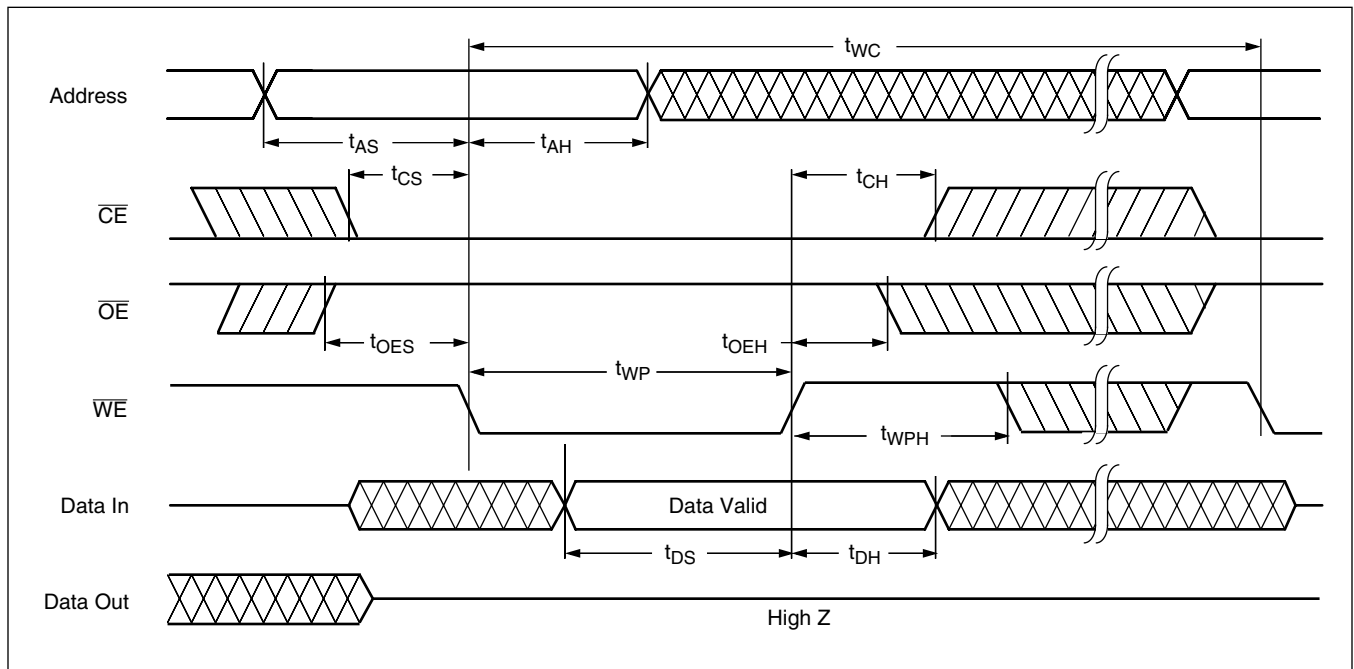
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Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$t_{WC}^{(4)}$	Write Cycle Time		5	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	\overline{CE} Pulse Width	50		ns
t_{OES}	\overline{OE} HIGH Setup Time	0		ns
t_{OEH}	\overline{OE} HIGH Hold Time	0		ns
t_{WP}	\overline{WE} Pulse Width	50		ns
t_{WPH}	\overline{WE} HIGH Recovery	50		ns
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	10		ns
t_{DW}	Delay to Next Write	10		μ s
t_{BLC}	Byte Load Cycle	0.2	100	μ s

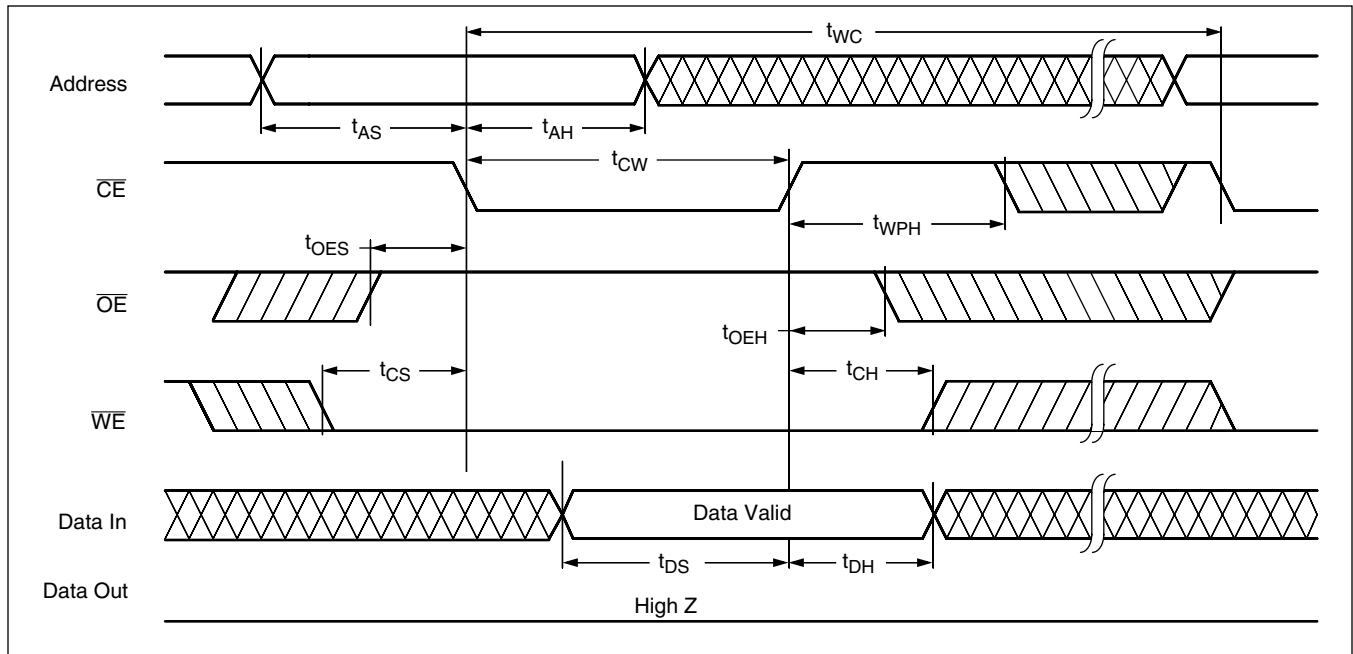
Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete internal write operation.

\overline{WE} Controlled Write Cycle

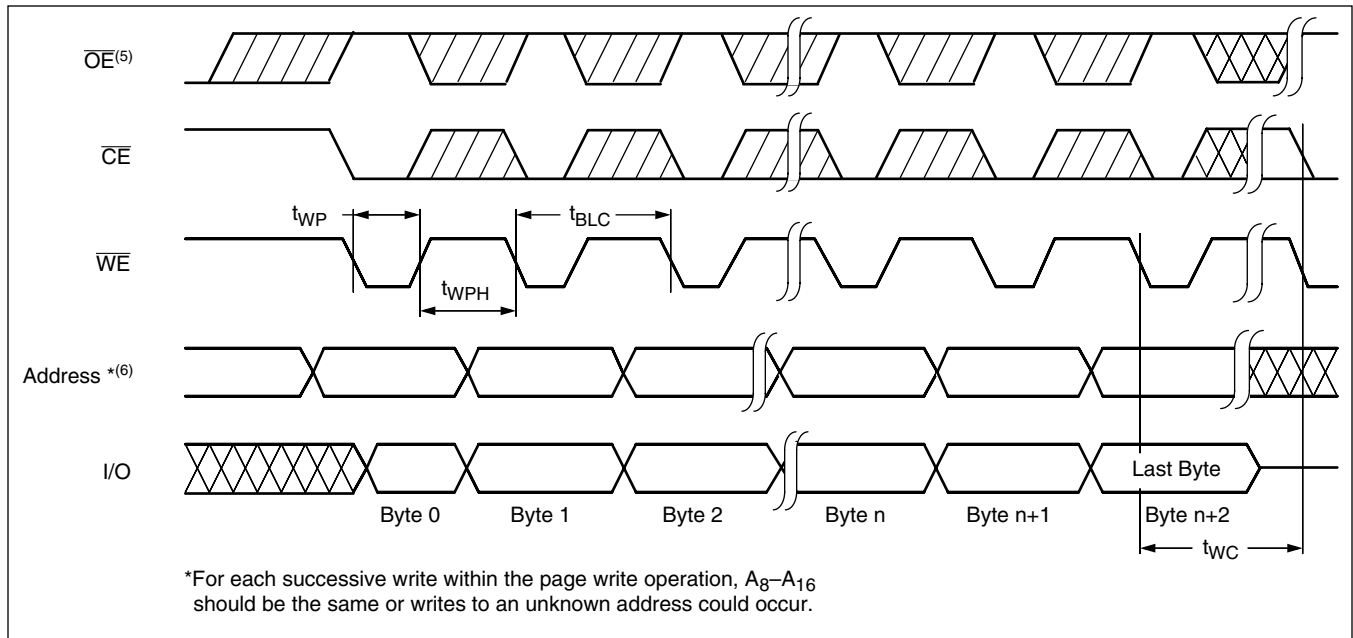


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$\overline{\text{CE}}$ Controlled Write Cycle



Page Write Cycle

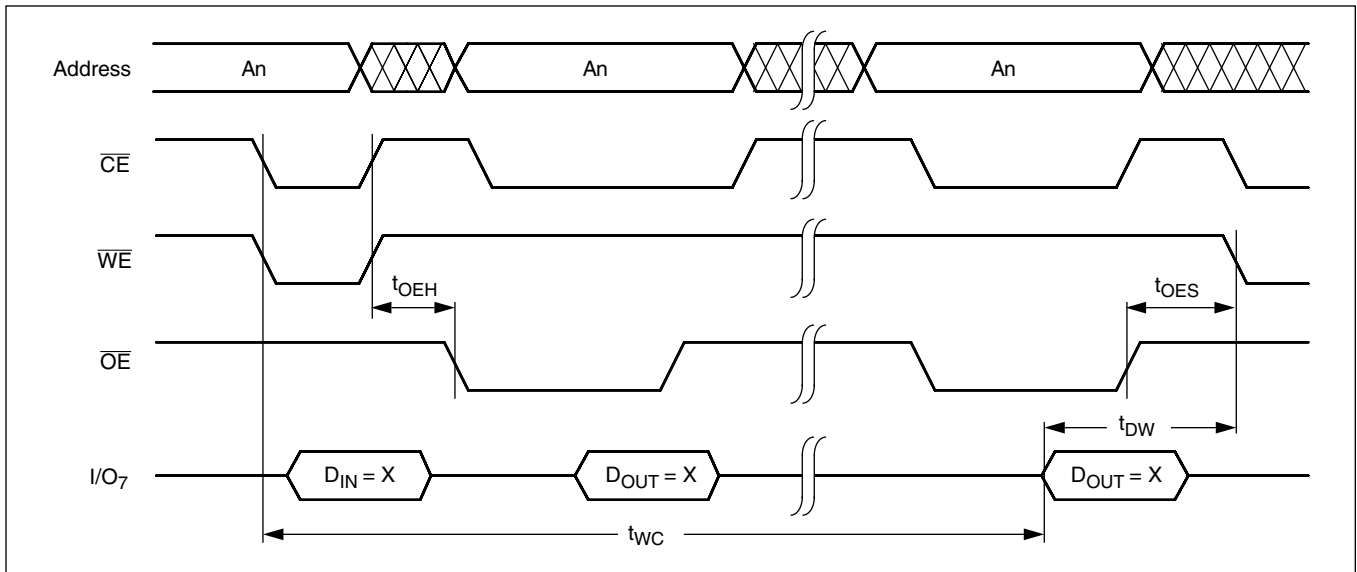


Notes: (5) Between successive byte writes within a page write operation, $\overline{\text{OE}}$ can be strobed LOW: e.g. this can be done with $\overline{\text{CE}}$ and $\overline{\text{WE}}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{\text{WE}}$ HIGH and $\overline{\text{CE}}$ LOW effectively performing a polling operation.

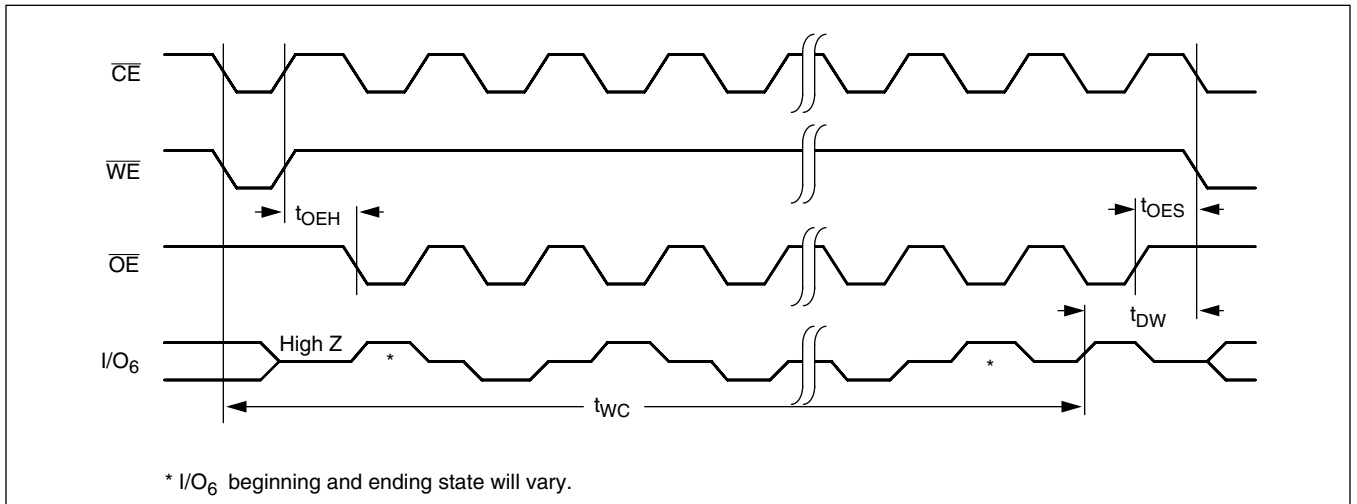
(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{\text{CE}}$ or $\overline{\text{WE}}$ controlled write cycle timing.

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DATA Polling Timing Diagram⁽⁷⁾



Toggle Bit Timing Diagram

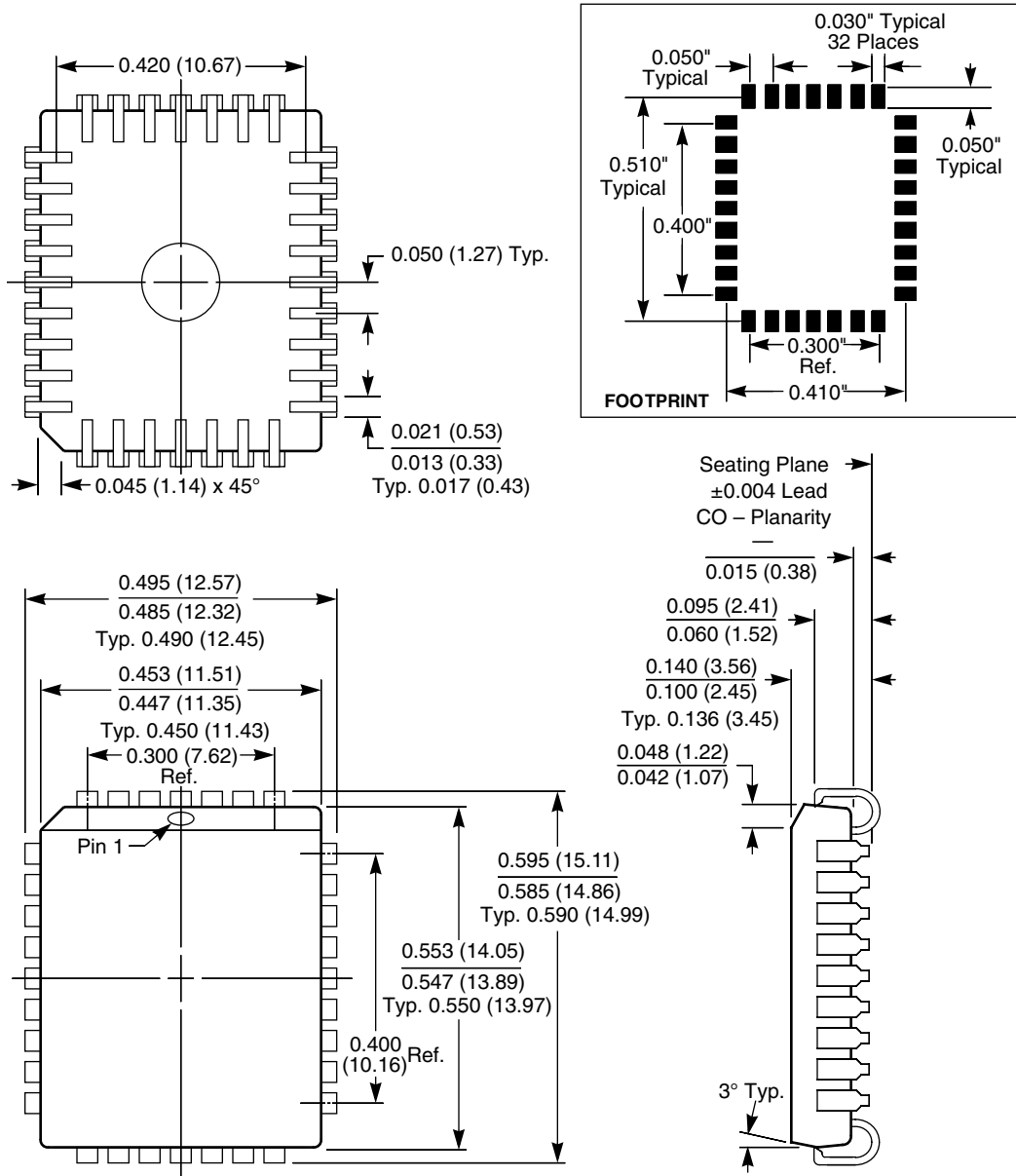


Notes: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

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PACKAGING INFORMATION

32-Lead Plastic Leaded Chip Carrier Package Type J



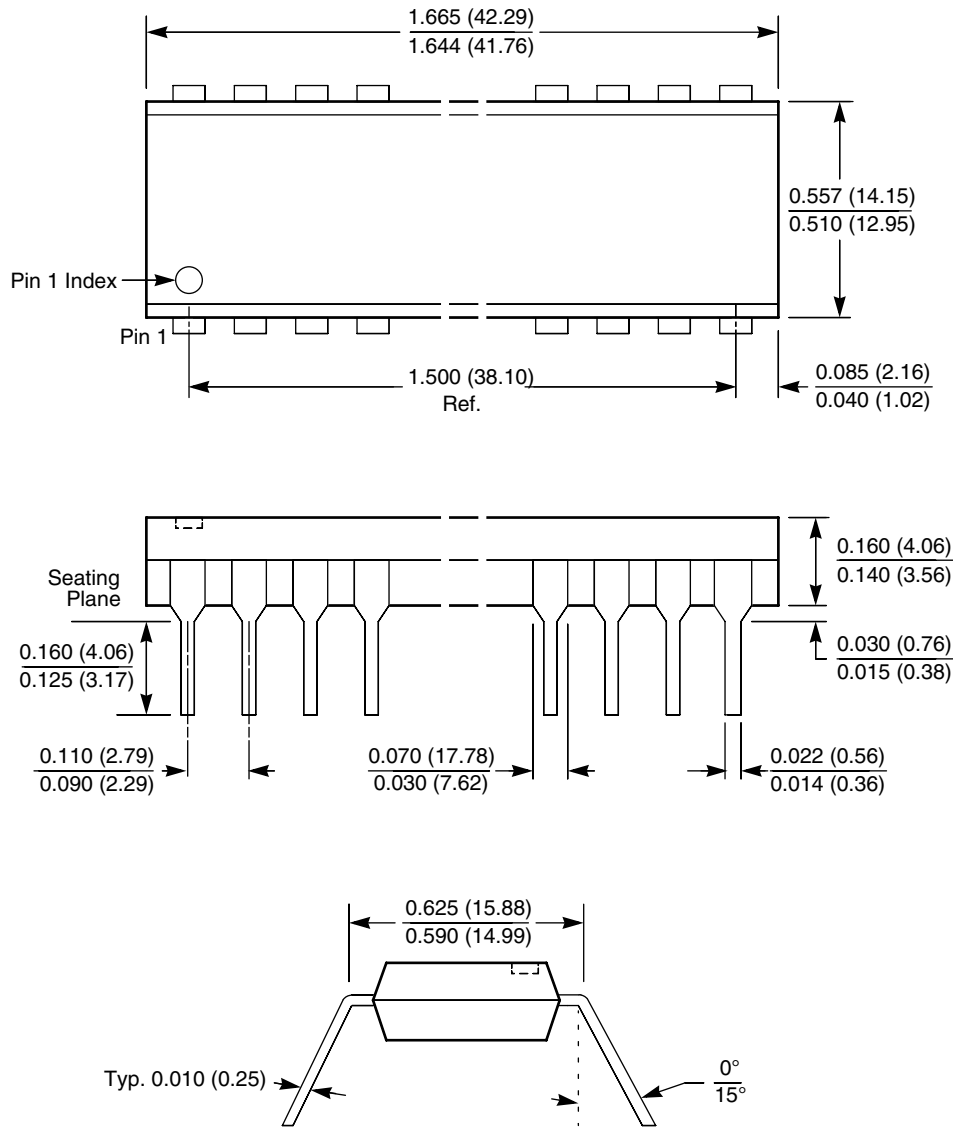
NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

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PACKAGING INFORMATION

32-Lead Plastic Dual In-Line Package Type P



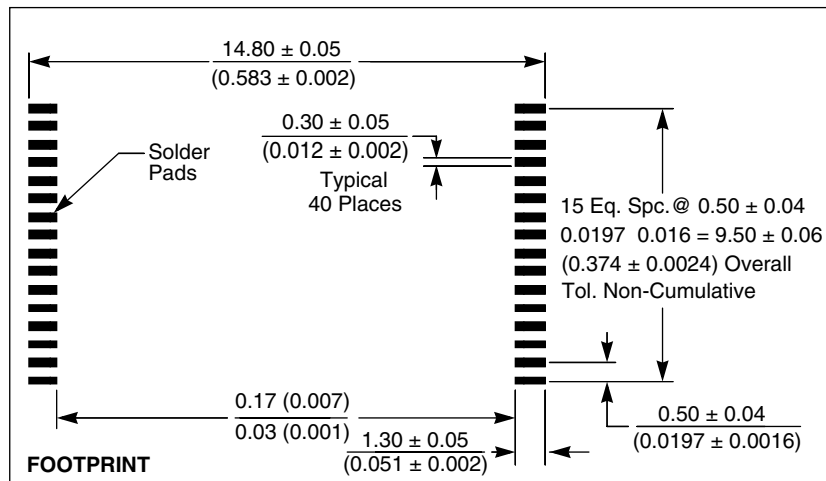
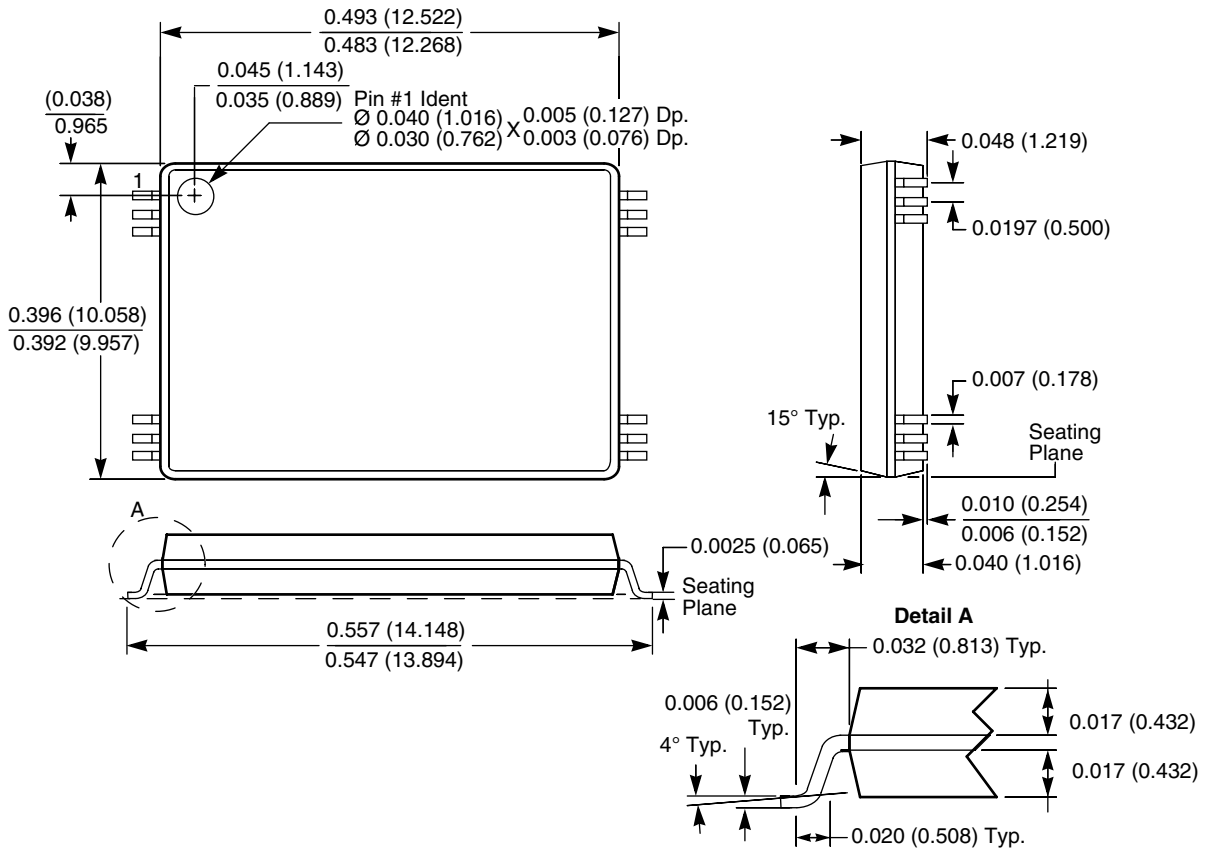
NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

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PACKAGING INFORMATION

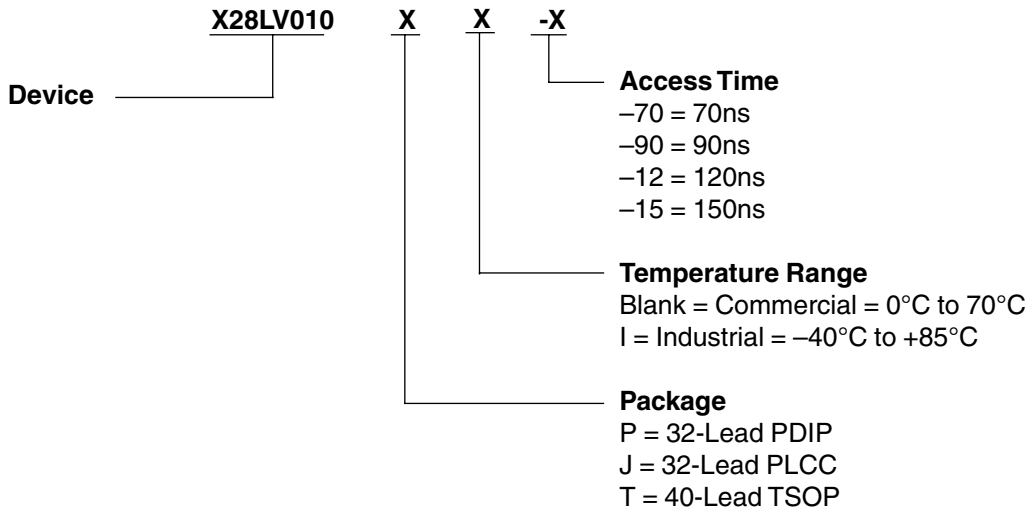
40-Lead Thin Small Outline Package (TSOP) Type T



NOTE: ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES IN PARENTHESES).

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Ordering Information



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LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.