VX1129 / VX1128

HIGH QUALITY VIDEO DECODER

PROGRESSIVE PROCESSOR AND

TIMING CONTROLLER

Headquarters
5F-1, No. 9, Prosperity Rd. I, Science Based Industrial Park, Hsin-Chu 300, Taiwan, R.O.C.
Tel : 886-3-5630888
Fax: 886-3-5630889

VXIS Technology Corp.
http://www.vxis.com

1 OVERVIEW

1.1 DESCRIPTION

VX1129/VX1128 is a progressive video processor IC, consists of video decoder, 3-D deinterlacer, picture enhancement engine, the scaling engine specially designed for video apps – the Relács, T-con for LCD panel timing control. It receives NTSC / PAL / SECAM analog video signal from DVD or TV, or digitized interlaced video stream (BT. 656 or bt. 601) from video decoder or MPEG video decoder. VX1129/VX1128 can perform high quality picture enhancement such as video noise reduction, sharpening, black-level extension, and Gamma correction, and converts it into non-interlaced formats for direct display on progressive devices, such as LCD displays, DTV, projectors, or PC monitors. Its output resolution covers 640x480, 720x480 800x480, 854x480, 800x600, 1024x768, 1280x720, 1280x768, 1280x1024. VX1129/VX1128 provides theater quality progressive scan video with VXIS's innovated *Motion Adaptive-3D Deinterlace Algorithm*, 3-2 pull down with automatic film mode detection, *Edge Preserving Pixel Interpolation*, frame-rate conversion, synchronization regeneration, and automatic source mode detection. The font-based on-screen-display(OSD), universal rogrammable timing control makes it become a highly integrated, most cost-efficient LCD video processor. The VX1129 (VX1128 without this function) can also receives progressive digital R,G,B signal from PC or DVD to perform PIP processing or direct progressive output for Mutimedia panel.

1.2 APPLICATION

- Portable DVD
- Car TV
- Small/middle size LCD TV
- PDP TV
- Multimedia panel

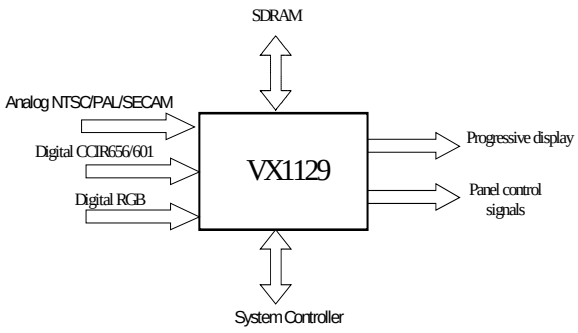


Figure 1.1 Interface for VX1129

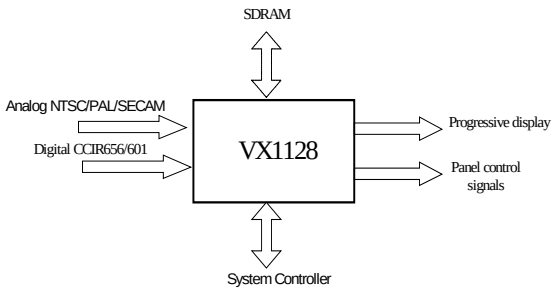


Figure 1.2 Interface for /VX1128

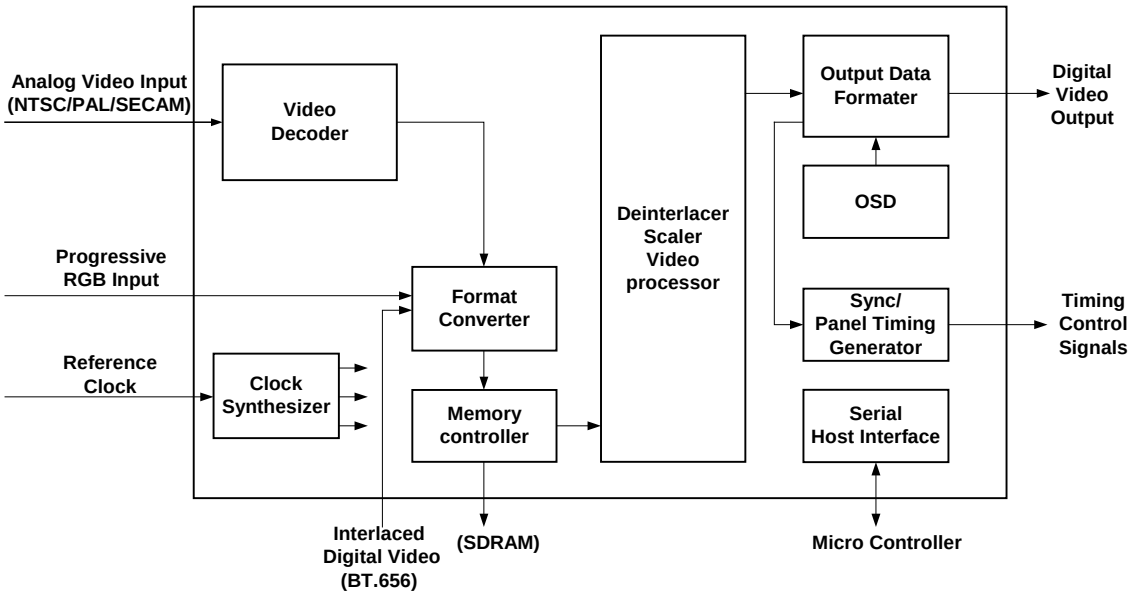
1.3 FEATURES

- Support Various Analog Video Input Formats
  - 6 Analog inputs : 6x CVBS or 4x CVBS + 1x S-video or 3x S-video or 1x CVBS + 1x S-video + 1x YpbPr
  - Support NTSC, NTSC-Japan, PAL (B, D, G, H, I, M, N, Nc) and SECAM video standard
- 10-bit A/D converters with fixed sampling clock
- Automatic Clamp Control (ACC) for CVBS and S-video
- Automatic gain control (AGC) / automatic chroma gain control
- Three analog preprocessing channels with digitally controlled AGC/clamp
- Horizontal and vertical Sync Detection
- Automatic detection of 50/60Hz field frequency and automatic switching between standards PAL, (Nc), PAL M, SECAM and NTSC
- Adaptive comb filter for two dimensions chrominance / luminance separation
- PAL delay line for correcting PAL phase errors and chroma noise cancellation
- VBI slicer supporting closed caption
- Macro-vision copyright detection
- Support Various Digital Video Input Formats
  - ITU-R BT.656
  - 8/16-Bit ITU-R BT.601 + Horizontal Sync + Vertical Sync
  - 24-Bit 4:4:4 YUV + Horizontal Sync + Vertical Sync
  - 24-Bit progressive RGB + Horizontal Sync + Vertical Sync for PIP
- Support Various Digital Video Output Formats
  - 24/18/16-Bit RGB + Horizontal Sync + Vertical Sync
  - 24/18/16-Bit 4:4:4 YUV + Horizontal Sync + Vertical Sync
  - 24/18/16-Bit 4:4:4 YPbPr (with Embedded Horizontal and Vertical Sync on Y)
  - 16-Bit 4:2:2 YUV + Horizontal Sync + Vertical Sync
  - 24-Bit 4:4:4 Interlaced YPbPr (with Embedded Horizontal and Vertical Sync on Y)
- Support Video-on-Progressive_RGB with Build-In PIP
- Frame rate up-conversion to 60 Hz for PAL & SECAM
- 2D or Motion-Adaptive 3D(with SDRAM) Deinterlace
- Edge-Preserving Pixel Interpolation
- Automatic Video Source Detection
- Embedded Scaling Engine (Relács), Supporting Output Resolution 640x480, 720x480 800x480, 854x480, 800x600, 1024x768, 1280x720, 1280x768, 1280x1024.
- Programmable Zoom/Shrink Scale with Anamorphic / Panoramic /4:3 / 16:9 Zoom Support
- Brightness, Contrast, Saturation, and Hue Adjustment

- Color Transient Improvement, Adaptive Black-Level Extension, Skin Tone Enhancement.
- Video Noise Reduction
- Frequency Directive Picture Sharpening
- 3-Channel 10-Bit Build-In Color gamma Look-Up Table for Video Fine-Tune
- Synchronization Re-Generation to Perform Stable Video.
- Host Interface Compatible with Two-Wire IIC, Serial Interface
- OSD with 128 Build-in and 64 Programmable Font and Attribute Table, 16 Colors at same Time from 16,777,216-Color Template, Blinking, and Blending
- R/G/B input/output port swap & rotation control
- 8 pins of programmable panel timing control signals
- One 20 MHz crystal request only
- 2.5V / 3.3V power supply with 5V tolerant digital I/O

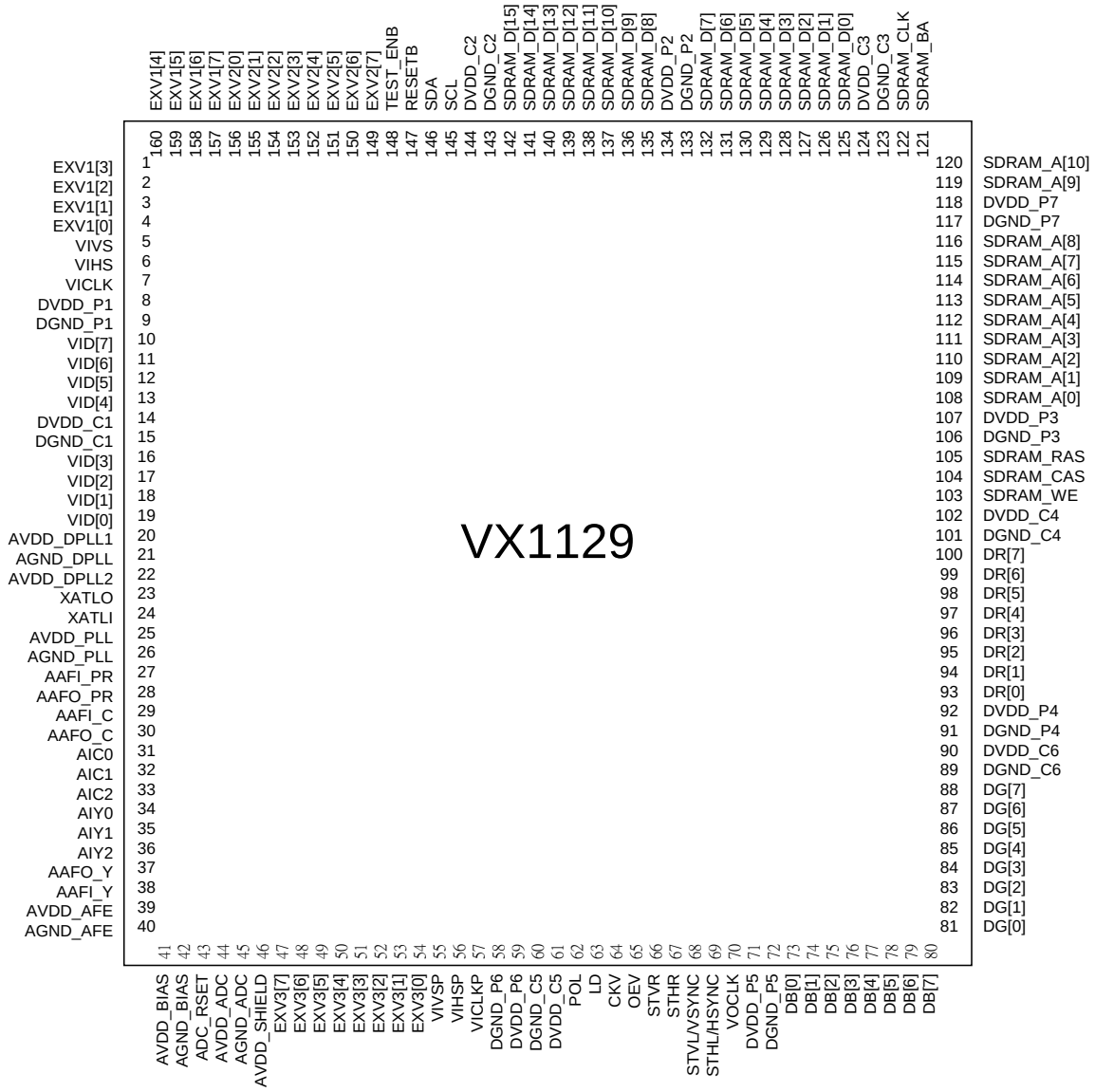
1.4 BLOCK DIAGRAM

1.4.1 BLOCK DIAGRAM OF VX1129

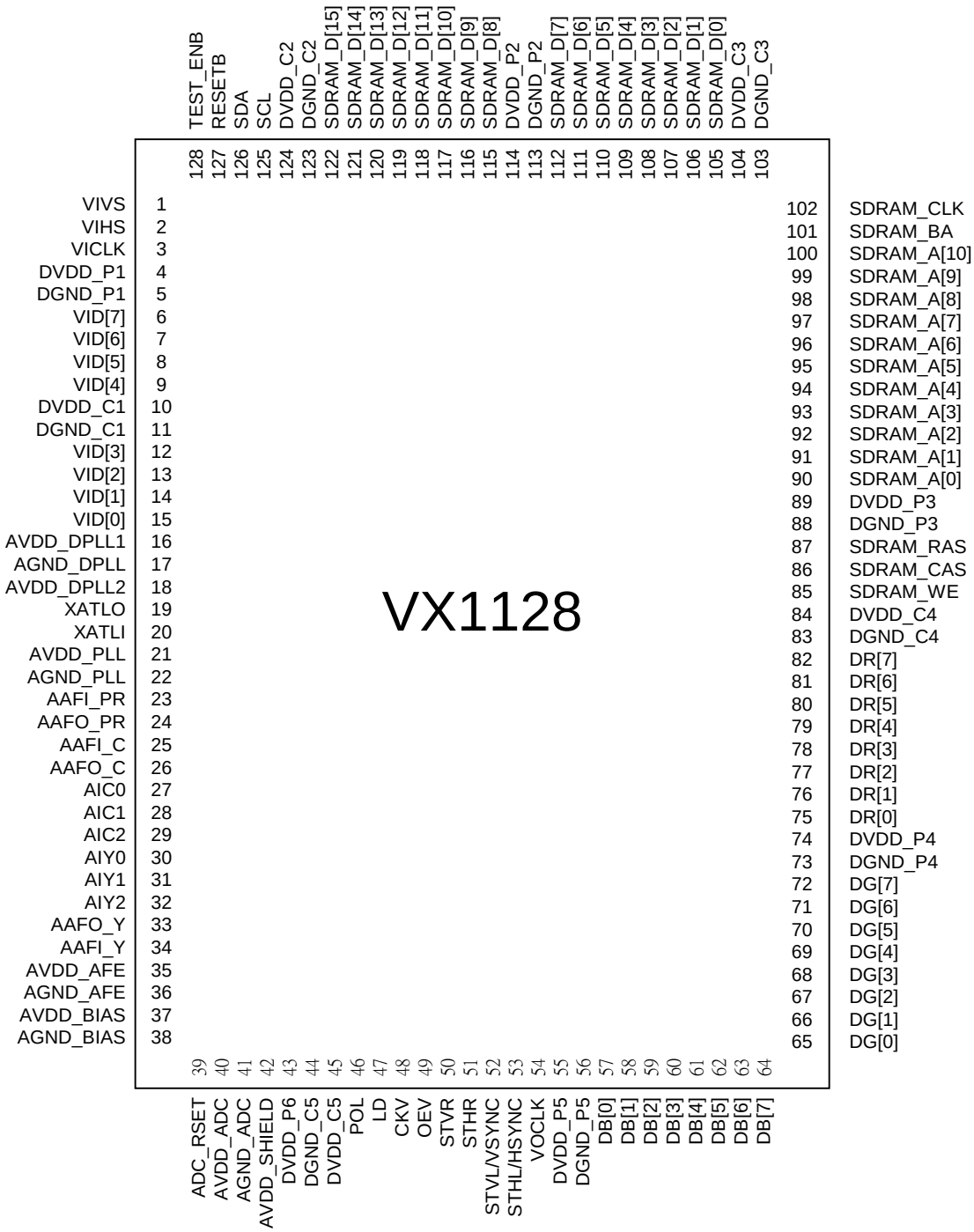


1.5 PINOUT DIAGRAM

1.5.1 PINOUT DIAGRAM OF VX1129



1.5.2 PINOUT DIAGRAM OF VX1128



1.6 PIN ASSIGNMENT

1.6.1 PIN ASSIGNMENT OF VX1129

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name_	Pin #	Pin Name
1	EXV1[3]	41	AVDD_BIAS	81	DG[0]	121	SDRAM_BA
2	EXV1[2]	42	AGND_BIAS	82	DG[1]	122	SDRAM_CLK
3	EXV1[1]	43	ADC_RSET	83	DG[2]	123	DGND_C3
4	EXV1[0]	44	AVDD_ADC	84	DG[3]	124	DVDD_C3
5	VIVS	45	AGND_ADC	85	DG[4]	125	SDRAM_D[0]
6	VIHS	46	AVDD_SHIELD	86	DG[5]	126	SDRAM_D[1]
7	VICLK	47	EXV3[7]	87	DG[6]	127	SDRAM_D[2]
8	DVDD_P1	48	EXV3[6]	88	DG[7]	128	SDRAM_D[3]
9	DGND_P1	49	EXV3[5]	89	DGND_C6	129	SDRAM_D[4]
10	VID[7]	50	EXV3[4]	90	DVDD_C6	130	SDRAM_D[5]
11	VID[6]	51	EXV3[3]	91	DGND_P4	131	SDRAM_D[6]
12	VID[5]	52	EXV3[2]	92	DVDD_P4	132	SDRAM_D[7]
13	VID[4]	53	EXV3[1]	93	DR[0]	133	DGND_P2
14	DVDD_C1	54	EXV3[0]	94	DR[1]	134	DVDD_P2
15	DGND_C1	55	VIVSP	95	DR[2]	135	SDRAM_D[8]
16	VID[3]	56	VIHSP	96	DR[3]	136	SDRAM_D[9]
17	VID[2]	57	VICLKP	97	DR[4]	137	SDRAM_D[10]
18	VID[1]	58	DGND_P6	98	DR[5]	138	SDRAM_D[11]
19	VID[0]	59	DVDD_P6	99	DR[6]	139	SDRAM_D[12]
20	AVDD_DPLL1	60	DGND_C5	100	DR[7]	140	SDRAM_D[13]
21	AGND_DPLL	61	DVDD_C5	101	DGND_C4	141	SDRAM_D[14]
22	AVDD_DPLL2	62	POL	102	DVDD_C4	142	SDRAM_D[15]
23	XATLO	63	LD	103	SDRAM_WE	143	DGND_C2
24	XATLI	64	CKV	104	SDRAM_CAS	144	DVDD_C2
25	AVDD_PLL	65	OEV	105	SDRAM_RAS	145	SCL
26	AGND_PLL	66	STVR	106	DGND_P3	146	SDA
27	AAFI_PR	67	STHR	107	DVDD_P3	147	RESET_B
28	AAFO_PR	68	STVL/VSYNC	108	SDRAM_A[0]	148	TEST_ENB
29	AAFI_C	69	STHL/HSYNC	109	SDRAM_A[1]	149	EXV2[7]
30	AAFO_C	70	VOCLK	110	SDRAM_A[2]	150	EXV2[6]
31	AIC0	71	DVDD_P5	111	SDRAM_A[3]	151	EXV2[5]
32	AIC1	72	DGND_P5	112	SDRAM_A[4]	152	EXV2[4]
33	AIC2	73	DB[0]	113	SDRAM_A[5]	153	EXV2[3]
34	AIY0	74	DB[1]	114	ADRAM_A[6]	154	EXV2[2]
35	AIY1	75	DB[2]	115	SDRAM_A[7]	155	EXV2[1]
36	AIY2	76	DB[3]	116	SDRAM_A[8]	156	EXV2[0]
37	AAFO_Y	77	DB[4]	117	DGND_P7	157	EXV1[7]
38	AAFI_Y	78	DB[5]	118	DVDD_P7	158	EXV1[6]
39	AVDD_AFE	79	DB[6]	119	SDRAM_A[9]	159	EXV1[5]
40	AGND_AFE	80	DB[7]	120	SDRAM_A[10]	160	EXV1[4]

1.6.2 PIN ASSIGNMENT OF VX1128

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name_	Pin #	Pin Name
1	VIVS	39	ADC_RSET	65	DG[0]	103	DGND_C3
2	VIHS	40	AVDD_ADC	66	DG[1]	104	DVDD_C3
3	VICLK	41	AGND_ADC	67	DG[2]	105	SDRAM_D[0]
4	DVDD_P1	42	AVDD_SHIELD	68	DG[3]	106	SDRAM_D[1]
5	DGND_P1	43	DVDD_P6	69	DG[4]	107	SDRAM_D[2]
6	VID[7]	44	DGND_C5	70	DG[5]	108	SDRAM_D[3]
7	VID[6]	45	DVDD_C5	71	DG[6]	109	SDRAM_D[4]
8	VID[5]	46	POL	72	DG[7]	110	SDRAM_D[5]
9	VID[4]	47	LD	73	DGND_P4	111	SDRAM_D[6]
10	DVDD_C1	48	CKV	74	DVDD_P4	112	SDRAM_D[7]
11	DGND_C1	49	OEV	75	DR[0]	113	DGND_P2
12	VID[3]	50	STVR	76	DR[1]	114	DVDD_P2
13	VID[2]	51	STHR	77	DR[2]	115	SDRAM_D[8]
14	VID[1]	52	STVL/VSYNC	78	DR[3]	116	SDRAM_D[9]
15	VID[0]	53	STHL/HSYNC	79	DR[4]	117	SDRAM_D[10]
16	AVDD_DPLL1	54	VOCLK	80	DR[5]	118	SDRAM_D[11]
17	AGND_DPLL	55	DVDD_P5	81	DR[6]	119	SDRAM_D[12]
18	AVDD_DPLL2	56	DGND_P5	82	DR[7]	120	SDRAM_D[13]
19	XATLO	57	DB[0]	83	DGND_C4	121	SDRAM_D[14]
20	XATLI	58	DB[1]	84	DVDD_C4	122	SDRAM_D[15]
21	AVDD_PLL	59	DB[2]	85	SDRAM_WE	123	DGND_C2
22	AGND_PLL	60	DB[3]	86	SDRAM_CAS	124	DVDD_C2
23	AAFI_PR	61	DB[4]	87	SDRAM_RAS	125	SCL
24	AAFO_PR	62	DB[5]	88	DGND_P3	126	SDA
25	AAFI_C	63	DB[6]	89	DVDD_P3	127	RESET_B
26	AAFO_C	64	DB[7]	90	SDRAM_A[0]	128	TEST_ENB
27	AIC0			91	SDRAM_A[1]		
28	AIC1			92	SDRAM_A[2]		
29	AIC2			93	SDRAM_A[3]		
30	AIY0			94	SDRAM_A[4]		
31	AIY1			95	SDRAM_A[5]		
32	AIY2			96	ADRAM_A[6]		
33	AAFO_Y			97	SDRAM_A[7]		
34	AAFI_Y			98	SDRAM_A[8]		
35	AVDD_AFE			99	SDRAM_A[9]		
36	AGND_AFE			100	SDRAM_A[10]		
37	AVDD_BIAS			101	SDRAM_BA		
38	AGND_BIAS			102	SDRAM_CLK		

1.7 PIN DESCRIPTION

Video Input Pins

Name	Type	Description	Notes
VID [7:0]	I	Digital Video Input Data(BT 656/601 / Y)	
VIHS	I	Digital Video Input Horizontal Synchronization	
VIVS	I	Digital Video Input Vertical Synchronization	
VICLK	I	Digital Video Input Clock	
EXV1[7:0]	I	Digital progressive video input data for PIP (R / Cb / CbCr)	Vx1129 only
EXV2[7:0]	I	Digital progressive video input data for PIP (G / Cr)	Vx1129 only
EXV3[7:0]	I	Digital progressive video input data for PIP (B)	Vx1129 only
VIHSP	I	Digital progressive video input Horizontal Synchronization	Vx1129 only
VIVSP	I	Digital progressive video input Vertical Synchronization	Vx1129 only
VICLKP	I	Digital progressive video input Clock	Vx1129 only

Video Output Pins

Name	Type	Description	Notes
DR [7:0]	O_{TS1}	R/V/Pr/BT656 Digital Video Output	
DG [7:0]	O_{TS1}	G/Y Digital Video Output	
DB [7:0]	O_{TS1}	B/U/Pb Digital Video Output	
HSYNC / STHL	O_1	Video Output Horizontal Synchronization / Composite Synchronization / STHL for TCON	
VSYNC / STVL	O_1	Video Output Vertical Synchronization / STVL for TCON	
VOCLK	O_2	Video Output Clock / BT656 Output Clock	
STHR	I/O_1	TCON Horizontal start address	
STVR	I/O_1	TCON Vertcal start address	
POL	I/O_1	TCON Polarity Selection	
LD	I/O_1	TCON Latch	
CKV	I/O_1	TCON Sample Clock	
OEV	I/O_1	TCON Output Enable	

External SDRAM I/O Pins

Name	Type	Description	Notes
SDRAM_D [15:0]	I/O_1	SDRAM Data Bus	
SDRAM_A [10:0]	O_{T1}	SDRAM Address Bus	
SDRAM_CLK	O_{T2}	SDRAM Clock	
SDRAM _RAS	O_{T1}	SDRAM Row Address Strobe (Active Low)	
SDRAM _CAS	O_{T1}	SDRAM Column Address Strobe (Active Low)	
SDRAM _WE	O_{T1}	SDRAM Write Enable (Active Low)	
SDRAM_BA	O_{T1}	SDRAM Bank	

Analog I/O Pins

Name	Type	Description	Notes
AIY0	AI	Analog Composite or Luminance Input	
AIY1	AI	Analog Composite or Luminance Input	
AIY2	AI	Analog Composite or Luminance Input	

AIC0	AI	Analog Composite or Chrominance Input	
AIC1	AI	Analog Composite or Chrominance Input or Pb Input	
AIC2	AI	Analog Composite or Chrominance Input or Pr Input	

Auxiliary Analog I/O Pins (8)

Name	Type	Description	Notes
AAFO_Y	AO	Analog Signal to Optional External Anti-Alias Filter of Y-channel	
AAFO_C	AO	Analog Signal to Optional External Anti-Alias Filter of C/Pb-channel	
AAFO_PR	AO	Analog Signal to Optional External Anti-Alias Filter of Pr-channel	
AAFIY	AI	Analog Signal from Optional External Anti-Alias Filter of Y-channel	
AAFIC	AI	Analog Signal from Optional External Anti-Alias Filter of C/Pb-channel	
AAFI_PR	AI	Analog Signal from Optional External Anti-Alias Filter of Pr-channel	
ADC_RSET	AI	Connect to an External Resister for Setting the Bias Current of ADC	

Miscellaneous I/O Pins

Name	Type	Description	Notes
/RESET	I_S	Chip Reset (Active Low)	
XTALO	XO	Crystal Output	
XTALI	XI	Crystal Input	
SDA	I/O_1	Host Interface Serial Data / Address	
SCL	I_S	Host Interface Serial Clock	
/TEST_EN	I_{PU}	Test Mode Enable (Active Low)	

Power Pins

Name	Type	Description	Notes
AVDD_PLL	P_{33}	Analog 3.3V Supply For PLL	Qty: 1
AVDD_AFE	P_{33}	Analog 3.3V Supply For AFE	Qty: 1
AVDD_BIAS	P_{33}	Analog 3.3V Supply For BIAS	Qty: 1
AVDD_ADC	P_{33}	Analog 3.3V Supply For ADC	Qty: 1
AVDD_SHIELD	P_{33}	Analog 3.3V Supply For Shielding	Qty: 1
AVDD_DPLL1	P_{25}	Digital 2.5V Supply For PLL	Qty: 1
AVDD_DPLL2	P_{25}	Digital 2.5V Supply For PLL	Qty: 1
DVDD_P1~7	P_{25}	Digital 3.3V Supply For I/O	Qty: 7

DVDD_C1~6	P_{25}	Digital 2.5V Supply For CORE	Qty: 6
AGND_PLL	G	Analog Ground For PLL	Qty: 1
AGND_AFE	G	Analog Ground For AFE	Qty: 1
AGND_BIAS	G	Analog Ground For BIAS	Qty: 1
AGND_ADC	G	Analog Ground For ADC	Qty: 1
AGND_DPLL	G	Digital Ground For PLL	Qty: 1
DGND_P1~7	G	Digital Ground For I/O	Qty: 7
DGND_C1~6	G	Digital Ground For CORE	Qty: 6

1.8 PACKAGE

- 1129 160-Pin HQFP
- 1128 128-Pin LQFP-EP