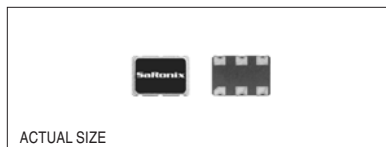


Technical Data

ST1317 / ST1517 Series



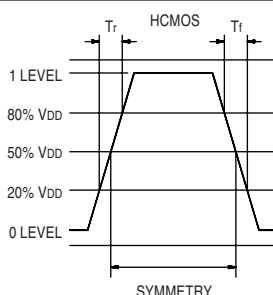
Description

The ST1317 / 1517 Series are voltage controlled crystal oscillators, with output logic levels compatible with HCMOS and TTL logic families. The device is contained in a sub-miniature, very low profile, leadless ceramic SMD package with 6 gold-plated contact pads. This miniature VCXO is ideal for today's automated assembly environments.

Applications

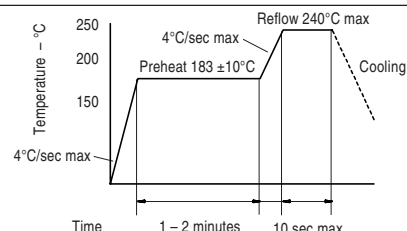
- For use in Phase-Locked Loop (PLL) Clock and Data Recovery, Frequency Translation, or Frequency Synthesis applications in Video, Video Compression, Telephony, and LAN/WAN Data Communication environments.
- High and wide frequency range from 32 to 125 MHz, see ST1307 / 1507 for frequencies from 1 to 31.999 MHz
- 3.3 or 5 Volt operation
- HCMOS and TTL compatible
- Tri-state output standard
- Miniature Ceramic SMD package
- Available on tape & reel; 16mm tape, 500pcs per reel

Output Waveform



Frequency Range:	32 MHz to 125 MHz
Frequency Stability:	±50 ppm over all conditions: operating temperature, rated input (supply) voltage changes, load change, calibration tolerance, shock and vibration (with control voltage held at center value)
Aging:	±12ppm max for 10 years @ +40°C average ambient op. temp.
Temperature Range:	Operating: 0 to +70°C or -40 to +85°C Storage: -55 to +125°C
Supply Voltage:	Recommended Operating: 3.3V ±10% or 5V ±5%
Supply Current:	35mA max (3.3V) 50mA max (32 to 70MHz), 65mA max (70+ to 125MHz) (5V)
Output Drive:	Symmetry: 5V: 45/55% @ 50% VDD, 40/60% @ 1.4V level 3.3V: 45/55% @ 50% VDD (0 to +70°C), 40/60% (-40 to +85°C) Rise & Fall Times: 4ns max, 20 to 80% VDD (3.3V CMOS and 5V AC MOS) 1.5ns max, 0.5V to 2.5V (5V TTL) Logic 0: 5V: 20% VDD max for AC MOS or 0.5V max for TTL 3.3V: 10% VDD max for capacitive load, 20% VDD max for 95Ω AC Logic 1: 5V: 80% VDD min for AC MOS or 2.5V min for TTL 3.3V: 90% VDD min for capacitive load, 80% VDD min for 95Ω AC Load: 5V: 5TTL or 50Ω AC or 50pF 32 to 50MHz, 30pF 50+ to 125MHz 3.3V: 30pF 32 to 80MHz, 95Ω AC 80+ to 125MHz Period Jitter RMS: 20ps max Phase Noise: -95dBc / Hz @100Hz, -110dBc / Hz @1kHz, -100dBc / Hz @10kHz
Pull Characteristics:	Input Impedance (pin 1): 50KΩ min Frequency Response (-3dB): 50 kHz min Pullability: ±32, ±50, ±80, ±100 ppm APR* (over rated control voltage) Rated Control Voltage: 0.5 to 4.5V (5V supply), 0.3 to 3.0V (3.3V supply) Operable Control Voltage: (-0.5V) to (VDD +0.5V) Transfer Function: Frequency increases when Control Voltage increases Monotonic Linearity: 10% max Center Control Voltage: 2.5V (5V supply), 1.65V (3.3V supply)
Mechanical:	Shock: MIL-STD-883, Method 2002, Condition B Solderability: MIL-STD-883, Method 2003 Terminal Strength: MIL-STD-883, Method 2004, Condition D Vibration: MIL-STD-883, Method 2007, Condition A Solvent Resistance: MIL-STD-202, Method 215 Resistance to Soldering Heat: MIL-STD-202, Method 210, Condition I or J
Environmental:	Thermal Shock: MIL-STD-883, Method 1011, Condition A Moisture Resistance: MIL-STD-883, Method 1004

Solder Reflow Guide



* APR = (VCXO Pull relative to specified Output Frequency) - (VCXO Frequency Stability)
Total VCXO Pull from specified nominal output frequency under all operating conditions for the life of the unit

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Technical Data

ST1317 / ST1517 Series

Tri-State Logic Table

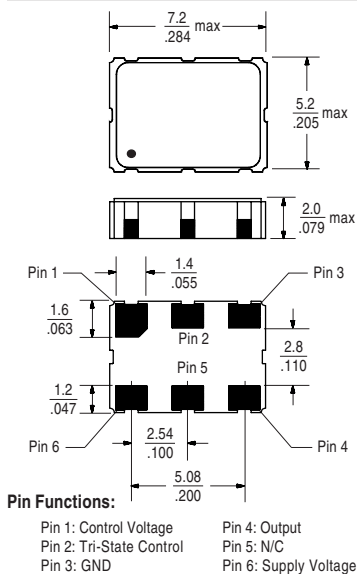
Pin 2 Input	Pin 4 Output
Logic 1 or N/C	Oscillation
Logic 0	High Impedance

Required Input Levels on Pin 2:

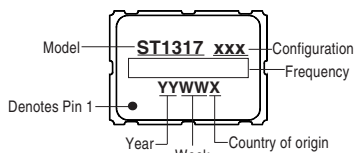
Logic 1 = 3.0V min

Logic 0 = 0.5V max(5V), 0.3V max (3.3V)

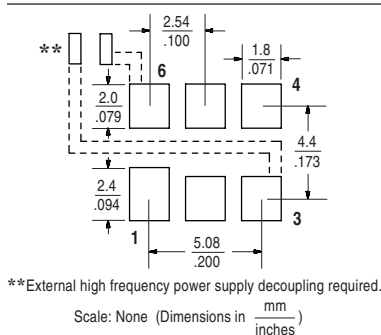
Package Details



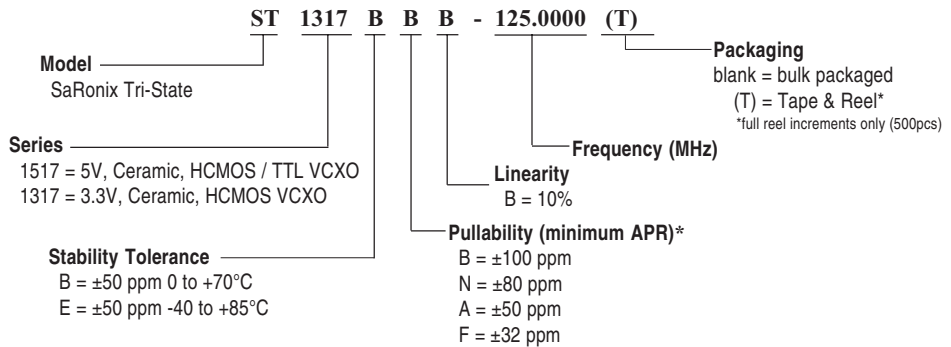
Marking Format (exact location of items may vary)



Recommended Land Pattern



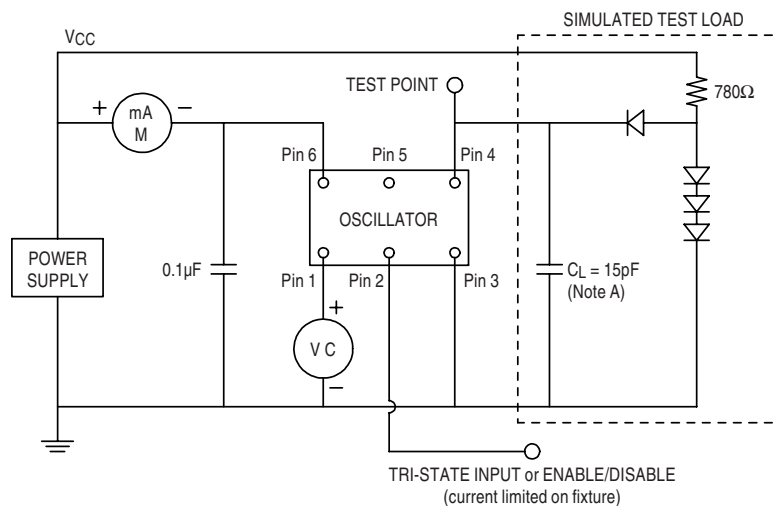
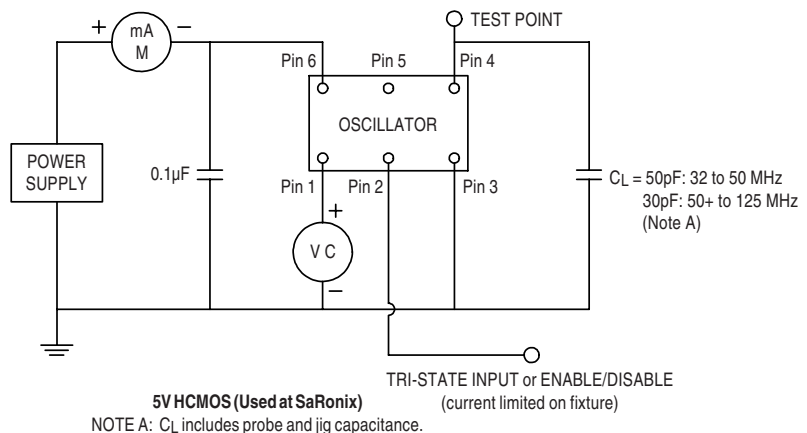
Part Numbering Guide



* APR = (VCXO Pull relative to specified Output Frequency) - (VCXO Frequency Stability)

Total VCXO Pull from specified nominal output frequency under all operating conditions for the life of the unit

Test Circuits:



All specifications are subject to change without notice.

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