

Dual P-Channel 1.8-V (G-S) MOSFET

CHARACTERISTICS

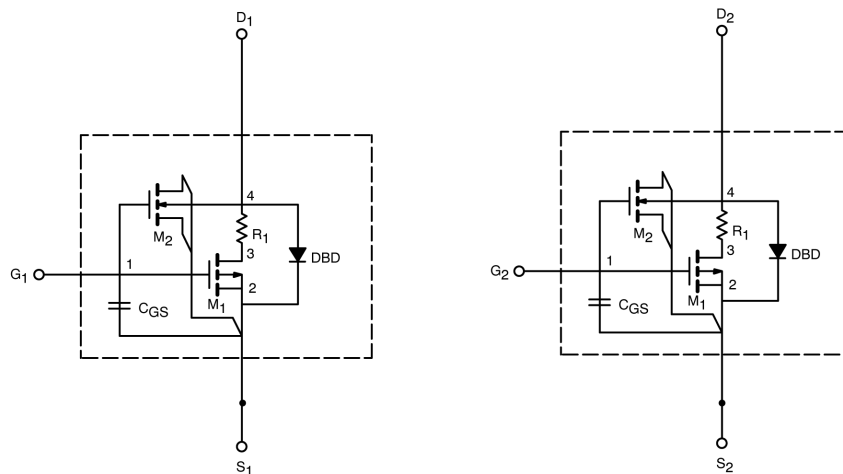
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model schematic is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device(s).

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model Si6969DQ

Vishay Siliconix



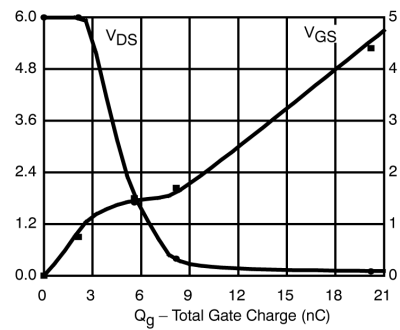
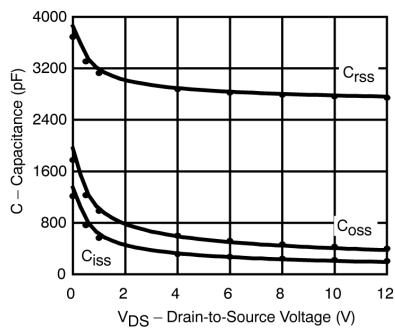
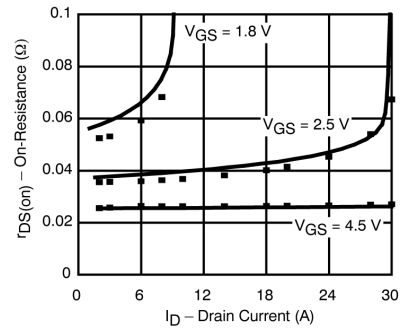
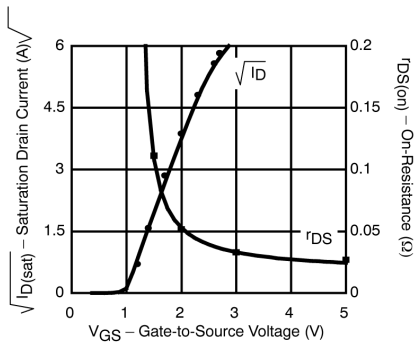
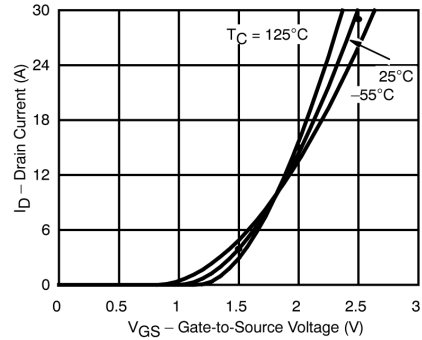
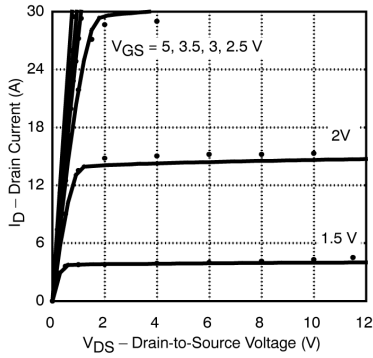
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Conditions	Typical	Unit
Static				
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	0.83	V
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -V, V _{GS} = -V		A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -V, I _D = -A		Ω
		V _{GS} = -V, I _D = -A		
		V _{GS} = -V, I _D = -A		
Forward Transconductance ^a	g _{fs}	V _{DS} = -V, I _D = -A		S
Diode Forward Voltage ^a	V _{SD}	I _S = -A, V _{GS} = 0 V		V
Dynamic^b				
Total Gate Charge	Q _g	V _{DS} = -V, V _{GS} = -V, I _D = -A		nC
Gate-Source Charge	Q _{gs}			
Gate-Drain Charge	Q _{gd}			
Turn-On Delay Time	t _{d(on)}	V _{DD} = -V, R _L = Ω I _D = -A, V _{GEN} = -V, R _G = Ω		ns
Rise Time	t _r			
Turn-Off Delay Time	t _{d(off)}			
Fall Time	t _f			
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -A, di/dt = 100 A/μs		

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.