

SCB68171 Very Little Serial Interface Chip (VLSIC)

Preliminary Specification

Microprocessor Products

DESCRIPTION

The Signetics Very Little Serial Interface Chip (VLSIC) is a bipolar interface device which connects one or more VMSbus controllers to the VMSbus itself. It provides bus driving and receiving in addition to latching data in both the transmit and receive directions.

SERCLK on the VMSbus has a waveform as shown in Figure 1, with four edges per cycle which are designated C1, S1, C2, S2. SYSCLK is used to discriminate (differentiate) the phases of SERCLK. The SYSCLK input should have a nominal 50% duty cycle and a cycle time which is 2/11 that of SERCLK, but SYSCLK and SERCLK need not be synchronous or have any fixed phase relationship. The 16MHz SYSCLK on the VMEbus meets these requirements for a back plane 2.9MHz SERCLK.

The VLSIC samples the XDATAN input on the SERCLK edge designated C1. XDATAN is clocked directly to SERDATN. The VLSIC then clocks the low-active OR (positive logic AND) of SERDATN and SERDATIN to RDATAN on the S1 edge. If XDATAN was high at C1, the VLSIC then samples the XSTARTN input on the C2 edge, and if it is low, the VLSIC makes SERDATN low, thus making a VMSbus start bit. If XDATAN was high at S1, then on the S2 edge it clocks the low active OR of SERDATN and SERDATIN to RSTARTN. If SERDATN was low at S1, it keeps (or makes) RSTARTN high at S2.

CHIPCLK is driven high from the C1 edge of SERCLK, and driven low from the C2 edge. Thus RDATAN and RSTARTN setup to CHIPCLK edges by approximately the low time of SERCLK. The VMSbus controller(s) must meet the specified setup and hold times to C1 for XDATAN and to C2 for XSTARTN.

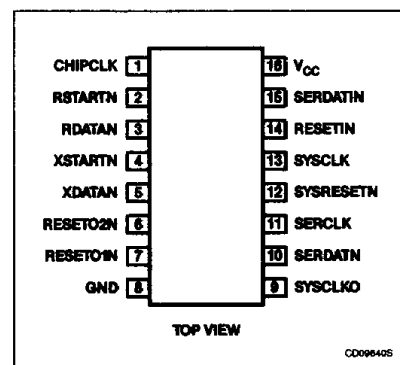
FEATURES

- 70mA open-collector drive for SERDATN
- Low capacitive loading
- Discriminates SERCLK into single-phase chip clock output
- Separates data and start bits for both receive and transmit
- Provides single bus load for multiple VMSbus controllers
- Simplifies controller design and allows use of slower technology
- VMEbus receiver for SYSCLK
- VMEbus driver/receiver for SYSRESETN
- 16-pin DIP

ORDERING INFORMATION

DESCRIPTION	PARAMETER	ORDERING CODE
16-Pin Plastic DIP	$V_{CC} 5V \pm 5\%$, $T_A = 0 \text{ to } 70^\circ\text{C}$	SCB68171C3N16

PIN CONFIGURATION



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DESCRIPTION (Continued)

A VMSbus controller is required to "jam" the bus by sending a string of "ones" (low) on SERDATN when a start bit is sensed while the controller is sending or tracking a frame. The first one bit should directly follow the misplaced start bit. Since the minimum S2-to-C1 time of SERCLK (25ns) is less than the sum of the maximum S2-to-RSTART-low time plus the minimum setup of XDATAN to C1, a controller cannot do this using XDATAN in the normal fashion.

The following feature is provided to solve this problem. The condition XDATAN low,

XSTARTN low, and CHIPCLK high directly sets the flipflop controlling SERDATN, and makes SERDATN low. (Note that a VMSbus controller would never assert both XDATAN and XSTARTN low in normal operation.) The assertion of both XDATAN and XSTARTN must occur soon enough to satisfy the SERDATN to S1 setup requirements of all the modules on the VMSbus.

The VLSIC is primarily intended for use in the P1 region of a VMEbus card. Space and functionality is at a premium in this area. Accordingly, the VLSIC includes an auto-

nous function of driving and receiving SYSRESETN on the VMEbus. A low on the RESETN input makes the VLSIC drive the SYSRESETN pin low. SYSRESETN is also received and driven onto two open-collector outputs RESETO1N and RESETO2N. RESETO1N has a high drive capability and is suitable for connection to the RESETN pin of a 680x0 processor, while RESETO2N has lower drive and capacitance and can be connected to the processor's HALTN pin. This function has no connection to the rest of the VLSIC, and could thus be used for some other purpose.

PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
SERCLK	11	I	Direct connect to VMSbus clock: Clocks SERDATN to RDATAN, RSTARTN. Clocks XDATAN, XSTARTN to SERDATN. Used to generate single-phase CHIPCLK.
SYSCLK	13	I	Direct connect to VMEbus clock or other signal meeting the specified frequency relationship to SERCLK: Used to discriminate the phases of SERCLK.
SYSCLKO	9	O	Repeater of SYSCLK for onboard use.
SERDATN	10	I/O	Direct connect to VMSbus data in bipolar open-collector links: Provides data output function for other types of links (e.g. optical). Requires pull-up resistor in either case.
SERDATIN	15	I	Tied to high logic level in bipolar open-collector links: Provides data input function for other types of links (e.g. optical).
CHIPCLK	1	O	Single phase clock for VMSbus controllers.
RDATAN	3	O	Conveys one/zero bits to VMSbus controller(s).
RSTARTN	2	O	Conveys start bits to VMSbus controller(s).
XDATAN	5	I	Input from VMSbus controller(s): In normal operation, a low on this line indicates a "one" bit should be sent. Simultaneous assertion of XDATAN and XSTARTN low, while CHIPCLK is high, drives SERDATN low directly in a "jam" condition.
XSTARTN	4	I	Input from VMSbus controller(s): In normal operation, a low on this line indicates a "start" bit should be sent. Simultaneous assertion of XDATAN and XSTARTN low, while CHIPCLK is high, drives SERDATN low directly in a "jam" condition.
RESETIN	14	I	Input from onboard logic: Low state forces SYSRESETN low.
SYSRESETN	12	I/O	Direct connect to VMEbus system reset: Open-collector output from RESETIN, received to drive RESETO1N and RESETO2N. Does not affect other VLSIC logic.
RESETO1N	7	O	High-drive open-collector output from SYSRESETN.
RESETO2N	6	O	Low-drive open-collector output from SYSRESETN.
V _{CC}	16		+5 Volts
GND	8		Ground

VMSBUS CONTROLLER DESIGN

Controllers using VLSIC should signal as follows on XDATAN and XSTARTN.

1. Controllers should present the next bit on XDATAN in response to the falling edge of CHIPCLK, and on XSTARTN in response to the rising edge of CHIPCLK. For a 2.9MHz SERCLK, they have at least 90nsec to do so, and approximately 120nsec from RDATAN valid.
2. Controllers may release XDATAN to high in response to the rising edge of

CHIPCLK, and may release XSTARTN to high in response to the falling edge. Since these are typically open-collector outputs of the controllers, there may be a timing advantage to do so.

3. A controller should present XDATAN and XSTARTN low in a "jam" situation, in a combinatorial fashion from RSTARTN. Thereafter the controller can release XSTARTN from the lowgoing edge of CHIPCLK, and may either signal 511 or 512 one bits in the usual fashion (1 and 2 above), or may just keep XDATAN low.

4. If two VMSbus controllers connected to the same VLSIC become "locally desynchronized", it is possible that one will present XDATAN low and the other XSTARTN low for the same bit cell. If this occurs, XDATAN predominates and SERDATN is driven low for a "one" bit. Thus a possible transient combination of XDATAN and XSTARTN low and CHIPCLK high actually has no effect. The controller presenting XSTARTN thereafter receives RDATAN low, and continues to try to send the start bit.

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ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATING	UNIT
V _S	Supply voltage range	-0.5 to +7	V
V _{IN}	Input voltage range	-0.5 to +5.5	V
T _A	Operating temperature range ²	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, T_A = 0°C to +70°C, R_L = 90, C_L = 15pF^{3, 4}

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I _{IL}	Low-level input current	V _{IN} = 0.4V			-0.4	mA
I _{IH}	High-level input current	* V _{IN} = 2.7V			20	μA
V _{IL}	Low-level input voltage		2		0.8	V
V _{IH}	High-level input voltage					V
V _{TH+} - V _{TH-}	Hysteresis — All inputs			300		mV
V _{OL}	Low level output voltage CHIPCLK, RDATAN, RSTARTN, RESETO2N SYSCLKO	I _{OL} = 8mA I _{OL} = 24mA I _{OL} = 70mA			0.5 0.5 0.5	V V V
V _{OH}	High level output voltage CHIPCLK, RDATAN, RSTARTN, SYSCLKO	I _{OH} = -3mA	2.7			V
I _{OH}	Output leakage current SERDATN, RESETO1N, SYSRESETN RESETO2N	V _{OH} = 5.5V			100	μA
I _{CC}	V _{CC} supply current	V _{CC} = Max			60	mA
C _I	Input capacitance SERCLK, SYSCLK			5		pF
C _{IO}	I/O capacitance SERDATN			10		pF

NOTES:

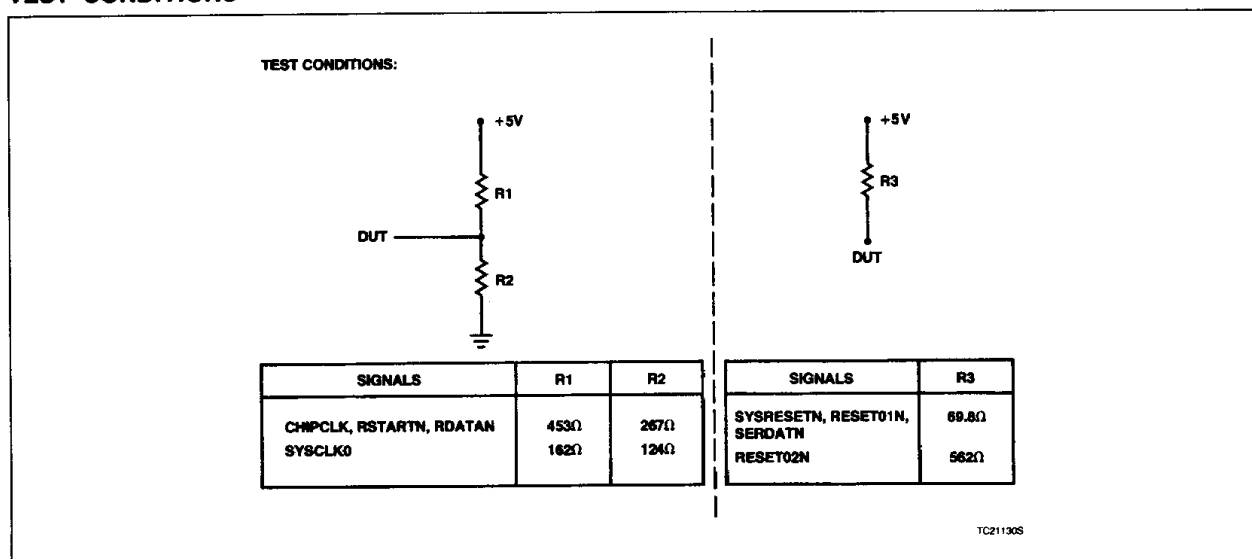
- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other conditions other than those indicated in the Electrical Characteristics section of this data sheet is not implied.
- For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
- Parameters are valid over specified temperature range.
- All voltage measurements are referenced to ground (GND). All time measurements are referenced at input voltages of 0.8V and 2V as appropriate.

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AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$, $R_L = 90$, $C_L = 50pF^{3, 4}$ (except as noted)

NO.	CHARACTERISTIC	TENTATIVE LIMITS		UNIT
		Min	Max	
1	Prop, C1 or C2 to SERDATN low	10	20	ns
2	Prop, C1 to SERDATN released	10	25	ns
3	Prop, S1 (S2) to RDATAN (RSTARTN) low		20	ns
4	Prop, S1 (S2) to RDATAN (RSTARTN) high		20	ns
5	Prop, C2 to CHIPCLK low		15	ns
6	Prop, C1 to CHIPCLK high		12	ns
7	Prop, XDATAN low and XSTARTN low (with CHIPCLK high) to SERDATN low ⁵		25	ns
8	RDATAN low to CHIPCLK low	t_{CL-10}		ns
9	RDATAN high to CHIPCLK low	t_{CL-12}		ns
10	RSTARTN low to CHIPCLK high	t_{CL-10}		ns
11	RSTARTN high to CHIPCLK high	t_{CL-12}		ns
12	Setup, SERDATN and/or SERDATIN low to S1 or S2	8		ns
13	Hold, SERDATN and/or SERDATIN low after S1 or S2	2		ns
14	Setup, SERDATN and SERDATIN high to S1 or S2	6		ns
15	Hold, SERDATN and SERDATIN high after S1 or S2	2		ns
16	Setup, XDATAN low to C1, XSTARTN low to C2	7		ns
17	Hold, XDATAN low after C1, XSTARTN low after C2	0		ns
18	Setup, XDATAN high to C1, XSTARTN high to C2	7		ns
19	Hold, XDATAN high after C1, XSTARTN high after C2	0		ns
20	Pulse Width, XDATAN and XSTARTN low with CHIPCLK high	10		ns
21	Prop, SYSCLK low to SYSCLKO low	8	15	ns
22	Prop, SYSCLK high to SYSCLKO high	5	12	ns
23	Pulse width, SERCLK low (t_{CL})	15		ns
23A	Pulse width, SYSCLK low (t_{SYCL})	10		ns
24	Pulse width, SYSCLK high (t_{SYCH})	10		ns
25	Cycle time, SYSCLK (t_{SYCY})	62		ns
25A	Cycle time, SERCLK (general case)	$5.49(t_{SYCY})$	$551(t_{SYCY})$	ns
26	Pulse width, SERCLK high, C1 to S1 ($t_{SYCY} = 62.5$) (general case)	174.25 $2.5t_{SYCY} + 18$		ns ns
27	Pulse width, SERCLK high, C2 to S2 ($t_{SYCY} = 62.5$) (general case)		120 $2(t_{SYCY}) - 5$	ns ns

TEST CONDITIONS

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