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Implementing NCP1207 in QR 24 W AC-DC Converter with Synchronous Rectifier

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APPLICATION NOTE

Introduction

The NCP1207 is a controller dedicated for driving the current−mode free running quasi−resonant Flyback offline converter.

This converter is designed for consumer products like notebooks, offline battery chargers, consumer electronics (DVD players, set−top boxes, TVs), etc.

The growing interest for EMI pollution reduction, efficiency improvement, and maximum safety has been taken into account while designing the NCP1207.

By implementing the NCP1207 one can build a power supply that can meet all those requirements. This can be achieved with help of the following NCP1207 main features:

- Current−Mode Control: Cycle−by−cycle primary current observation is helping to prevent any significant primary overcurrent which would cause transformer's core saturation and consequent serious power supply failure.
- Critical Mode Quasi−resonant Operation: Prevents the converter operation in Continuous Conduction Mode in any input and output condition. It is provided by the zero crossing detection of the auxiliary winding's voltage.
- By addition of the reasonable delay the switch turn−on instant can be shifted to the minimum (valley) of drain voltage. This improves EMI noise and efficiency.
- Dynamic Self−Supply: Ensures IC proper operation in applications where the output voltage varies during operation like battery chargers. The DSS also supplies the IC when the overvoltage event is being latched and converter operation is stopped.
- Overvoltage Protection: By sampling the plateau voltage on the auxiliary winding, the NCP1207 enters into latched fault condition whenever the overvoltage is detected. The controller stays fully latched until the V_{CC} decreases below 4.0 V, e.g. when the user unplugs the power supply from the mains outlet and re−plugs it. The OVP threshold can be adjusted externally.
- Over−Load Protection: by continuously monitoring the feedback loop activity, NCP1207 enters hiccup operation as soon as the power supply is overloaded. As soon as overload condition disappears, the NCP resumes operation.

The 24 W AC−DC Adaptor Board Specification

The adaptor has following maximum and performance ratings.

Output Power	24 W
Output Voltage	12 VDC
Output Current	2.0 A
Minimum Input Voltage	180 VAC
Maximum Input Voltage	240 VAC
Maximum Switching Frequency	70 kHz

The schematic diagram of the adaptor can be seen in Figure 1.

Transformer Design

The bulk capacitor voltage than can be calculated:

$$V_{bulk-min} = V_{AC-min}\sqrt{2} = 180 \cdot \sqrt{2} = 255\ VDC \quad \text{(eq. 1)}$$

$$V_{bulk-max} = V_{AC-max}\sqrt{2} = 240 \cdot \sqrt{2} = 339\ VDC \quad \text{(eq. 2)}$$

The requested output power is 24 W.

Assuming 87% efficiency the input power is equal to:

$$P_{IN} = \frac{P_{OUT}}{\eta} = \frac{24}{0.87} = 27.6\ W \quad \text{(eq. 3)}$$

The average value of input current at minimum input voltage is:

$$I_{IN-AVG} = \frac{P_{IN}}{V_{bulk-min}} = \frac{27.6}{255} = 108\ mA \quad \text{(eq. 4)}$$

Taking into account the absence of a clamping network the suitable reflected primary winding voltage for 800 V rated MOSFET switch is:

$$V_{flbk} = 800\ V - V_{bulk-max} - V_{spike} \quad \text{(eq. 5)}$$
$$= 800 - 339 - 330 = 131\ V$$

Using calculated Flyback voltage the maximum duty cycle can be calculated:

$$\delta_{max} = \frac{V_{flbk}}{V_{flbk} + V_{bulk-min}} = \frac{131}{131 + 255} \quad \text{(eq. 6)}$$
$$= 0.339 = 0.34$$

The following equation determines peak primary current:

$$I_{ppk} = \frac{2 \cdot I_{IN-AVG}}{\delta_{max}} = \frac{2 \cdot 108 \cdot 10^{-3}}{0.34} = 635\ mA \quad \text{(eq. 7)}$$

The maximum switching frequency at minimum input voltage is 70 kHz. Taking into account Quasi−Resonant (QR) and valley switching operation of the NCP1207 the QR time interval from the instant of the total core demagnetization to the valley of switch's drain voltage needs to be taken into account when calculating the switch max. ON−time interval.

Using QR time of 2 μs appropriate for 70 kHz switching frequency the ON−time can be calculated as follows:

$$t_{ON} = \left(\frac{1}{f_{sw}} - t_{QR}\right) \cdot \delta_{max} = \left(\frac{1}{70 \cdot 10^3} - 2 \cdot 10^{-6}\right) \quad \text{(eq. 8)}$$
$$\cdot\ 0.34 = 4.177\ \mu s = 4.18\ \mu s$$

The EF25 core for transformer was selected. It has cross−section area $A_e = 52.5\ mm^2$. The N67 ferrite material allows to use maximum operating flux density $B_{max} = 0.25$ T.

The number of turns for the primary winding is:

$$n_p = \frac{V_{bulk-min} \cdot t_{ON}}{B_{max} \cdot A_e} = \frac{255 \cdot 4.18 \cdot 10^{-6}}{0.25 \cdot 52.5 \cdot 10^{-6}} \quad \text{(eq. 9)}$$
$$= 80\ turns$$

The primary inductance can be calculated as follows:

$$L_p = \frac{V_{bulk-min}}{I_{ppk}} \cdot t_{ON} = \frac{255}{0.635} \cdot 4.18 \cdot 10^{-6} \quad \text{(eq. 10)}$$
$$= 1.68\ mH$$

The A_L factor of the transformer's core can be calculated as follows:

$$A_L = \frac{L_p}{(n_p)^2} = \frac{1.68 \cdot 10^{-3}}{(80)^2} = 263\ nH \quad \text{(eq. 11)}$$

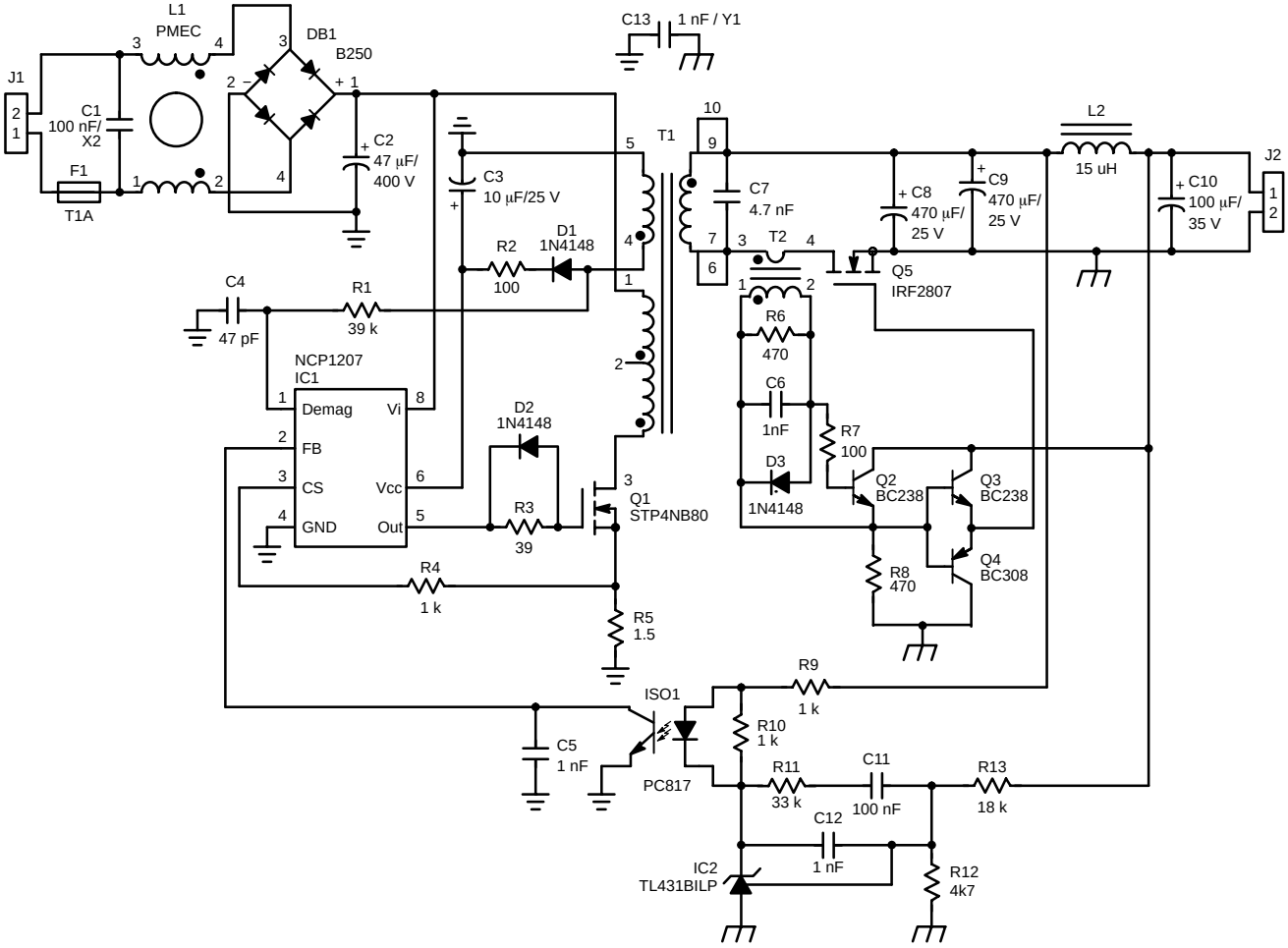


Figure 1. Schematic Diagram of the QR 24 W AC−DC Converter with NCP1207 and Synchronous Rectifier

Since skin effect and eddy currents play a significant role in the Flyback topology at given switching frequency the Litz wire is used. It consists of 4 wires each with diameter 0.12 mm.

To reduce the leakage inductance the primary winding is split to two windings each with half number of turns. The secondary winding is inserted between those halves primary windings. This is well known as a sandwich arrangement.

For an output voltage of 12 V, the number of turns of the secondary winding can be calculated (accounting for synchronous rectifier) as follows:

$$n_S = \frac{V_S(1 - \delta_{max})n_p}{\delta_{max} \cdot V_{bulk-min}} = \frac{12 \cdot (1 - 0.34) \cdot 80}{0.34 \cdot 255} \quad \text{(eq. 12)}$$
$$= 7.3 = 8 \text{ turns}$$

The secondary winding is again made with Litz wire. It consists in 24 wires featuring a diameter of 0.22 mm.

Using the above number of turns, the auxiliary winding derived:

$$n_{AUX} = \frac{(V_{AUX} + V_{fwd})}{V_S} \cdot n_S = \frac{(12 + 1)}{12} \cdot 8$$
$$= 8.67 = 9 \text{ turns} \quad \text{(eq. 13)}$$

A single wire of 0.15 mm diameter was used for the auxiliary winding.

The windings arrangement of the transformer is the following:

1. Auxiliary
2. 1st Half Primary
3. Secondary
4. 2nd Half Primary

Primary Current Control

Primary current control path consist in the sensing resistor R5, skipping resistor R4 and pin 3 of the IC named CS. The maximum voltage threshold on CS pin is about 1 V. The value of the current sense resistor R5 is therefore given by:

$$R_5 = \frac{V_{TH-max}}{I_{ppk}} = \frac{1}{0.635} = 1.57\ \Omega = 1.5\ \Omega \quad \text{(eq. 14)}$$

The skipping resistor R4 value together with the internal 200 μA current source gives the skipping voltage level. It is decided to set the skipping level to 20% of the maximum primary current. In this case the skipping voltage is 0.2 V.

The value of the skipping resistor R4 is then:

$$R_4 = \frac{V_{CS-skip}}{I_{int}} = \frac{0.2}{200 \cdot 10^{-6}} = 1\ \Omega \quad \text{(eq. 15)}$$

Demagnetization Detection and OVP

The transformer demagnetization sensing is based on the zero crossing detection of the auxiliary winding's voltage. For this purpose the zero crossing detector built−in the NCP1207 is connected to pin 1. Resistor R1 limits the current flowing through the pin 1 voltage clamps. Also this resistor together with capacitor C4 delays the zero voltage crossing event. It helps to tune the turn−on instant when the drain voltage is in the valley.

Resistor R1 has also another function. Together with the internal resistor divider, the comparator and its voltage reference, it forms an overvoltage protection circuit. Pin 1 includes a 30 k resistor internally connected to ground. If the voltage on that pin reaches roughly 7.2 V an overvoltage latch is triggered and converter operation is blocked until input supply plug is disconnected. The value of resistor R1 then can be calculated as follows:

$$R_1 = 30 \cdot 10^3 \cdot \left(\frac{V_{CC-max}}{7.2} - 1\right) \quad \text{(eq. 16)}$$
$$= 30 \cdot 10^3 \cdot \left(\frac{15.5}{7.2} - 1\right) - 34.6\ \text{k}\Omega = 39\ \text{k}\Omega$$

The value of the delaying capacitor C4 is a result of tuning process on the real board.

Synchronous Rectifier

The synchronous rectifier consists in the following basic blocks: the sensor of the secondary current, the gate driver and the MOSFET switch. A current transformer T2 senses the output rectifier current. The current transformer has its primary winding located in series with the secondary switch within the secondary current loop. Resistor R6 loads the secondary winding of the current transformer. The resistor R6 converts the current into a voltage. That voltage is filtered and limited by capacitor C6 and diode D3. It then goes to the gate driver, which consists in transistors Q2, Q3 and Q4 and pull−down resistor R8.

For the current transformer the ring core R10 was selected. It features a cross−section area $A_e = 7.83\ \text{mm}^2$. The N30 magnetic allows to use a maximum operating flux density of $B_{max} = 0.2$ T. The appropriate number of turns than can easily be wound on that core is around 20. The maximum demagnetization time of the converter's transformer can be calculated as follows:

$$t_{dem} = \frac{n_{cs-se} \cdot B_{max} \cdot A_e}{V_{clamp}} = \frac{20 \cdot 0.2 \cdot 7.82 \cdot 10^{-6}}{0.7}$$
$$= 45\ \mu\text{s} \quad \text{(eq. 17)}$$

This value is bigger than maximum operating demagnetization time. It means that the current transformer has enough freedom to work properly even if the converter is overloaded or during the start−up sequence when the demagnetization time is longer due to a lower output voltage.

Feedback Loop

The feedback loop is based on the secondary side to ensure good output voltage regulation. The control circuit is based on a TL431 that has an internal reference voltage of 2.5 V. The output voltage of the converter is divided by the resistors R12 and R13. The resistor divider output voltage is compared with the internal reference voltage of the TL431.

With regard to TL431 input leakage current, the resistor divider's current of 500 μA was selected. The resistor R12 then can be calculated as follows:

$$R_{12} = \frac{V_{TL431}}{I_{divider}} = \frac{2.5}{500 \cdot 10^{-6}} = 5\ k\Omega = 4.7\ k\Omega \quad \text{(eq. 18)}$$

The value of the upper resistor R13 of the divider is:

$$R_{13} = R_{12} \cdot \left(\frac{V_{OUT}}{V_{TL431}} - 1\right) = 4700 \cdot \left(\frac{12}{2.5} - 1\right) = 17860\ \Omega = 18\ k\Omega \quad \text{(eq. 19)}$$

The resistor R10 ensures the minimum current supply of 1.0 mA for TL431 in case of the converter operation near to the maximum output power when current flowing through the LED diode within the Optocoupler ISO1 is close to zero. The threshold voltage of the LED being around 1.0 V, the value of R10 is:

$$R_{10} = \frac{V_{LED}}{I_{TL431}} = \frac{1}{1 \cdot 10^{-3}} = 1\ k\Omega \quad \text{(eq. 20)}$$

The resistor R9 limits the current flowing through the LED in case the voltage across the output terminal of the TL431 is at its minimum, e.g. 2.5 V. Considering the nominal output voltage 12 V and a maximum LED current of 10 mA, the value of R9 is:

$$R9 = \frac{V_{OUT} - V_{LED} - V_{TL431}}{I_{LED-max}} = \frac{12 - 1 - 2.5}{10 \cdot 10^{-3}} = 850\ \Omega = 1\ k\Omega \quad \text{(eq. 21)}$$

Resistor R11 together with capacitors C11.C12 creates a "Pole−Zero" compensation circuit of the feedback loop. Their values are result of feedback loop response measurements and adjustments on the board.

Since NCP1207 allows a direct Optocoupler connection, the ISO1 is connected without any pull−up resistor to Pin 2. Capacitor C5 bypasses any high frequency current pick−up.

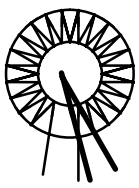
Primary Switch Snubber Network

Since any standard snubber will generate losses, a different approach has been used in this design. To cope with voltage spikes, the primary switch has been rated for a 800 V BV_{dss}. The snubber capacitor C7 is located on the secondary side. This capacitor has two functions. The first purpose is to create together with secondary leakage inductance the resonant tank. Similarly the primary resonant circuit consists of the primary leakage inductance and associated parasitic capacitances. The resonant frequency of the secondary resonant circuit is approximately two times higher than resonant frequency of the primary resonant circuit. This frequency difference efficiently decreases the voltage spike on the primary. The second function of C7 is to protect the secondary switch from voltage spikes.

Bill of Materials

C1	100 nF / X2
C2	47 μF / 400 V
C3	10 μF / 25 V
C4	47 pF, Ceramic
C5	1.0 nF, Ceramic
C6, C12	1.0 nF, Ceramic
C7	4.7 nF, Ceramic
C8, C9	470 μF / 25 V
C10	100 μF / 35 V
C11	100 nF, Ceramic
C13	1.0 nF / Y1
DB1	B250
D1, D2, D3	1N4148
F1	1.0 A, Time−lag
IC1	NCP1207
IC2	TL431
ISO1	PC817
L1	2*10 mH, Common Mode
L2	10 μH
Q1	STP4NB80
Q2, Q3	BC238
Q4	BC308
Q5	IRF2807
R1	39 k
R2, R7	100
R3	39
R4, R9, R10	1.0 k
R5	1.5
R6, R8	470
R11	33 k
R12	4k7
R13	18 k
T1	Transformer, See text
T2	Transformer, See below

T2 Transformer Specifications



Ferrite Core	Epcos (Siemens) R10, Material N30
Primary Winding	1 turn (See Picture), Heat resisting plastic insulated wire, copper 0.5 mm diameter.
Secondary Winding	22 turns, enameled wire, copper 0.3 mm diameter. For winding beginnings see the application schematic.

PCB Layout

Proper printed circuit board layout is essential for good operation of the whole converter. It also influences the EMI signature in both conducted and radiated measurements.

It is important to ensure good grounding technique and keep all high frequency current loop and high voltage areas as small as possible to avoid both magnetic and electric radiation.

An example of the layout can be seen in Figure 2.

The component arrangement can be seen in Figure 3. The board size is 97.5 * 44 mm.

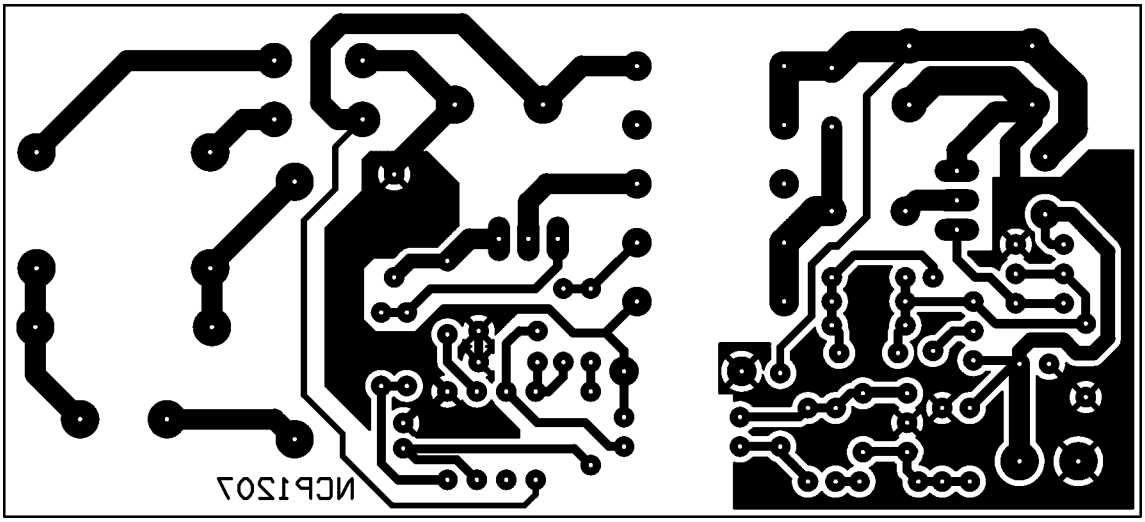


Figure 2. Printed Circuit Board Layout − Bottom Side

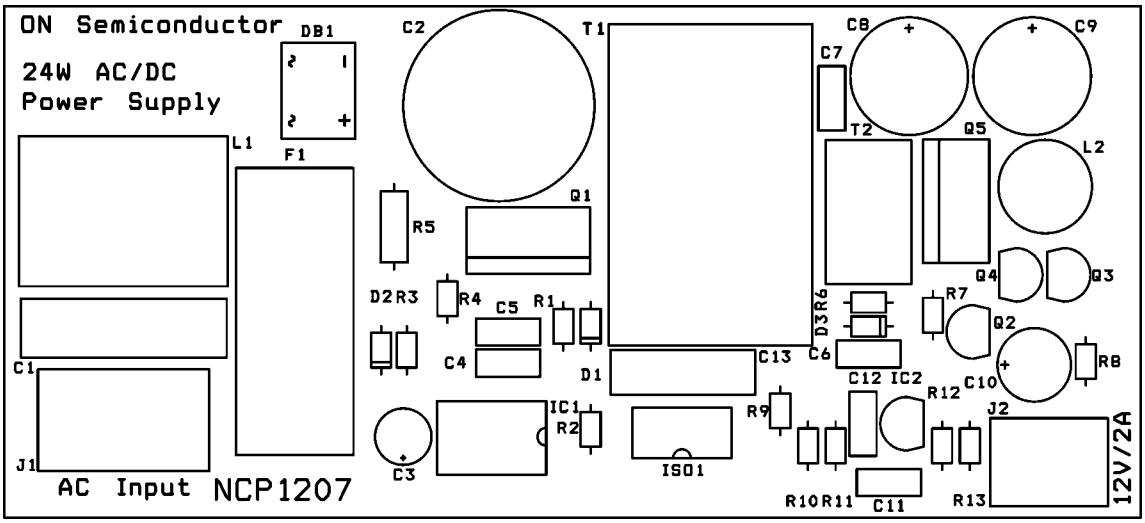


Figure 3. Printed Circuit Board Layout − Silkscreen Component Side

Practical Results

One of the most important parameters considered during the converter design is the overall power conversion efficiency. For this reason the synchronized output rectifier was utilized. Table 1 lists the measured results for converter working at minimum specified input voltage 255 VDC. The corresponding graphical representation of the Table 1 can be seen in Figure 4. Table 2 lists similar results for the maximum specified input voltage of 339 VDC. Figure 5 again helps to see the results belonging to Table 2. The no−load power consumption measured at 255 VDC input voltage is about 275 mW and at 339 VDC is about 385 mW.

Table 1. Power Conversion Efficiency at 255 VDC Input Voltage

P_{OUT} (W)	Efficiency (%)
24	91.68
22	91.69
20	91.63
18	91.49
16	91.33
14	90.83
12	90.08
10	89.16
8	87.87
6	85.59
4	81.85
2	77.31

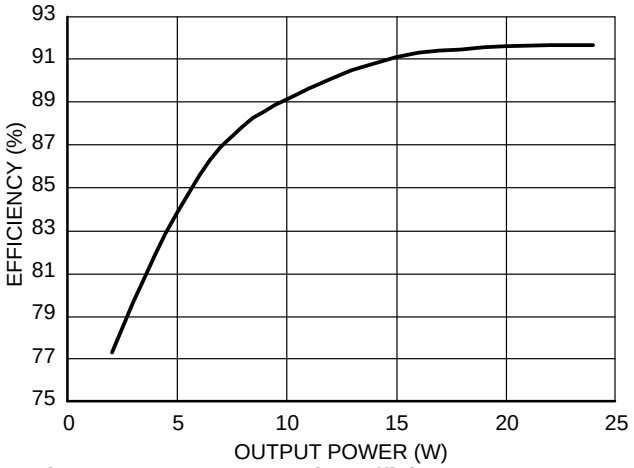


Figure 4. Power Conversion Efficiency at 255 VDC Input Voltage

Table 2. Power Conversion Efficiency at 339 VDC Input Voltage

P_{OUT} (W)	Efficiency (%)
24	90.70
22	90.56
20	90.42
18	90.28
16	89.76
14	88.97
12	87.85
10	86.39
8	84.75
6	82.16
4	78.20
2	73.62

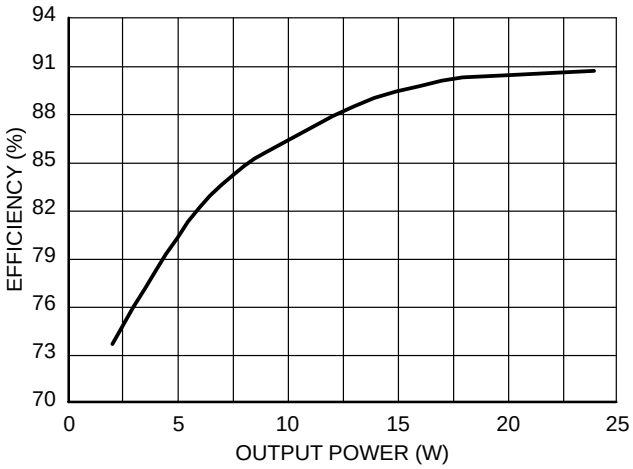


Figure 5. Power Conversion Efficiency at 339 VDC Input Voltage

The following pictures of the basic voltage waveforms demonstrate the operation of the converter at specific conditions.

Figure 6 shows in top trace the gate driver voltage and in bottom trace primary switch's drain voltage at full load.

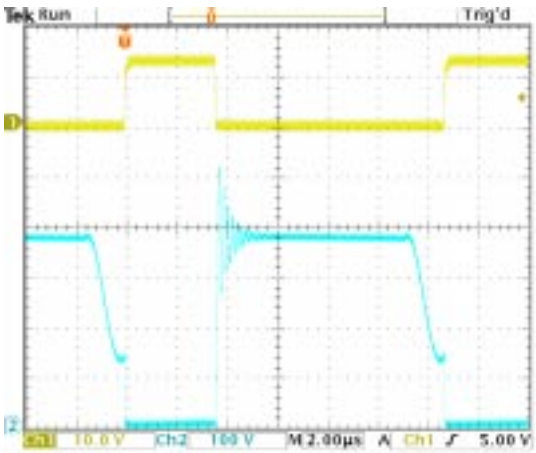


Figure 6. Gate Driver and Drain Voltage at Full Load

Figure 7 shows the same measurement points as in Figure 6 but at medium load condition when the first valley of the drain voltage is being skipped.

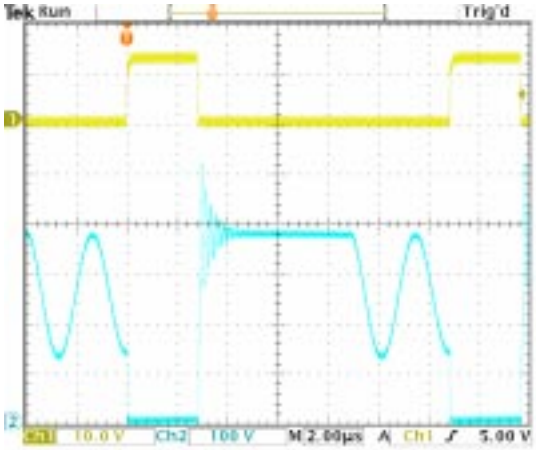


Figure 7. Gate Driver and Drain Voltage at Medium Load

Figure 8 is the same as previous measurements but for light load condition when two valleys are skipped.

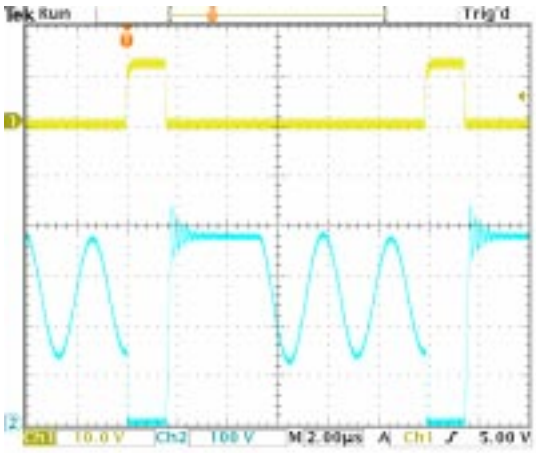


Figure 8. Gate Driver and Drain Voltage at Light Load

The cycle skipping operation when the output load is very light is depicted in Figure 9.

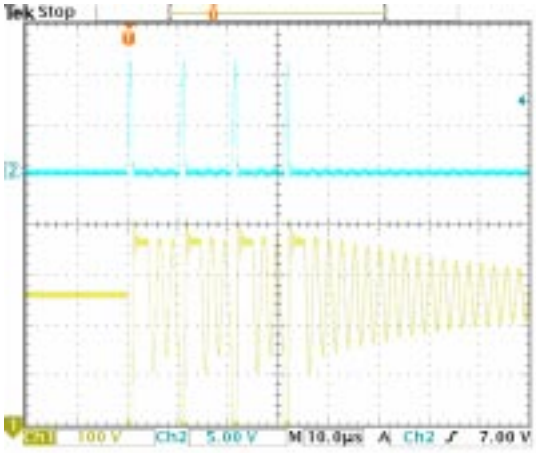


Figure 9. Gate Driver and Drain Voltage during the Cycle Skipping at Very Light Load

The waveforms during overload condition is depicted in Figure 10.

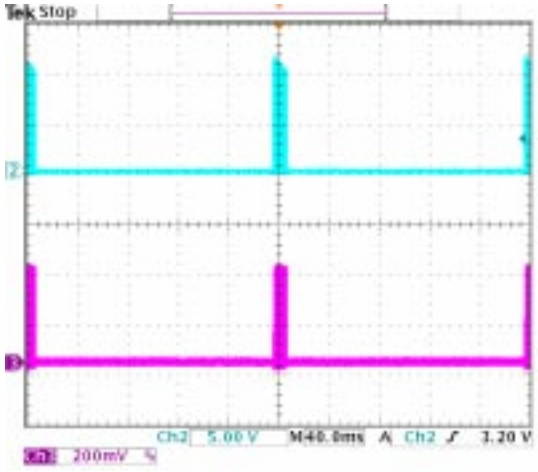


Figure 10. Gate Driver and Drain Voltage during the Over−Load

The load regulation of the output voltage for load step change from 100% to 10% and vise versa can be seen in Figure 12.

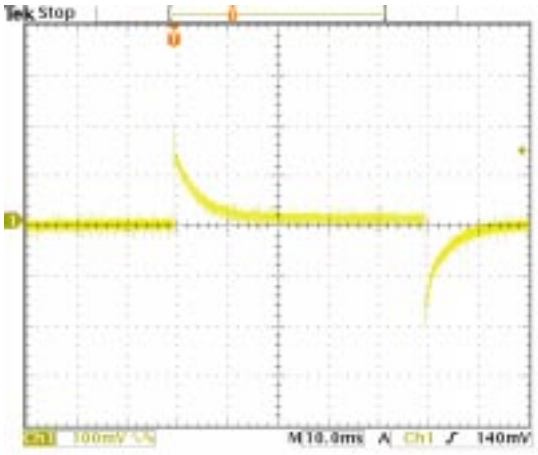


Figure 12. Load Regulation

Detailed view of the burst pulse during overload can be seen in Figure 11. This figure clearly demonstrates the operation of the internal soft−start block.

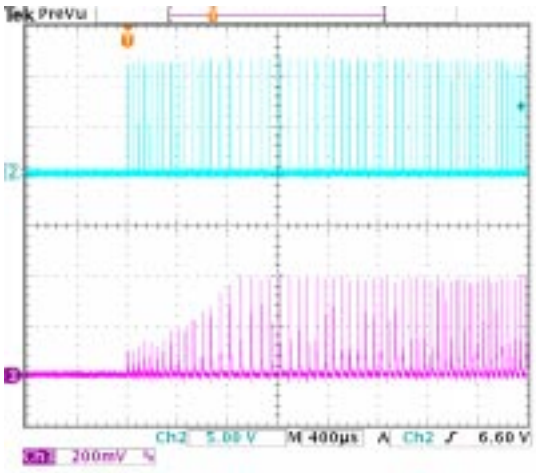


Figure 11. Detailed View of the Burst Pulse

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