Ordering number: EN 2844B

SANYO No.2844B

LC36256P,PL,PM,PML-10/12/15

Asynchronous Silicon Gate CMOS LSI

32768 Words × 8 Bits Static RAMs

General Description

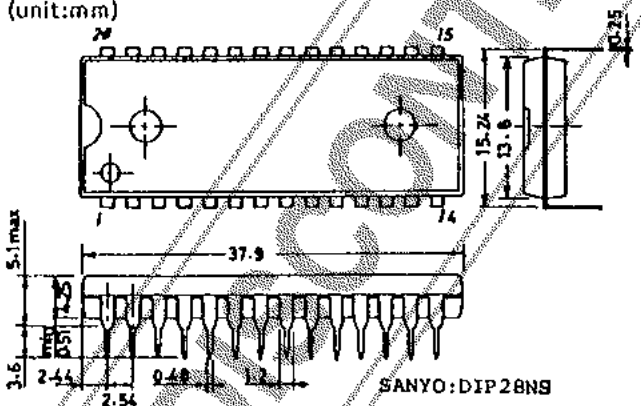
The LC36256P,PL,PM,PML are fully asynchronous silicon gate CMOS static RAMs organized as 32768 words x 8bits. The CMOS-used peripheral permits less current dissipation.

The LC36256P,PL,PM,PML have two control signal inputs: $\overline{OE}$ for high-speed memory access and chip enable input $\overline{CE}$ for power-down and device select. Therefore, the LC36256P,PL,PM,PML are especially suited for use in systems which require high speed, low power, battery backup and it is easy to expand the memory capacity.

Features

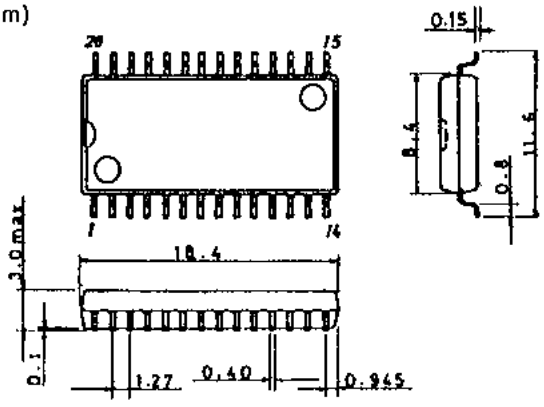
- Access time
  - LC36256P,PL,PM,PML-10:100ns(max)
  - LC36256P,PL,PM,PML-12:120ns(max)
  - LC36256P,PL,PM,PML-15:150ns(max)
- Low standby current
  - LC36256PL,PML-10/12/15 :100uA(max)
  - LC36256P,PM-10/12/15 : 1mA(max)
- Single 5V supply:5V±10%
- Data retention supply voltage:2.0 to 5.5V
- No clock required (Fully static memory)
- Directly TTL compatible:All inputs and outputs
- Common data input and output using 3-state outputs
- 28-pin DIP plastic package
- 28-pin SOP (450mil) plastic package

Case Outline 3081-D28NS
(unit:mm)



SANYO:DIP28NS

Case Outline 3156-SOP28VL
(unit:mm)



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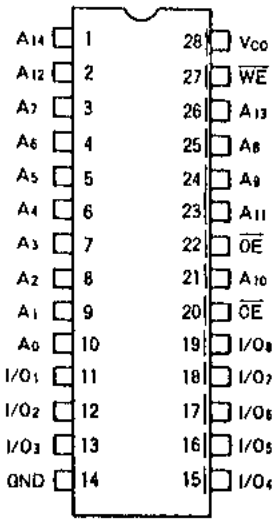
Specifications and information herein are subject to change without notice.

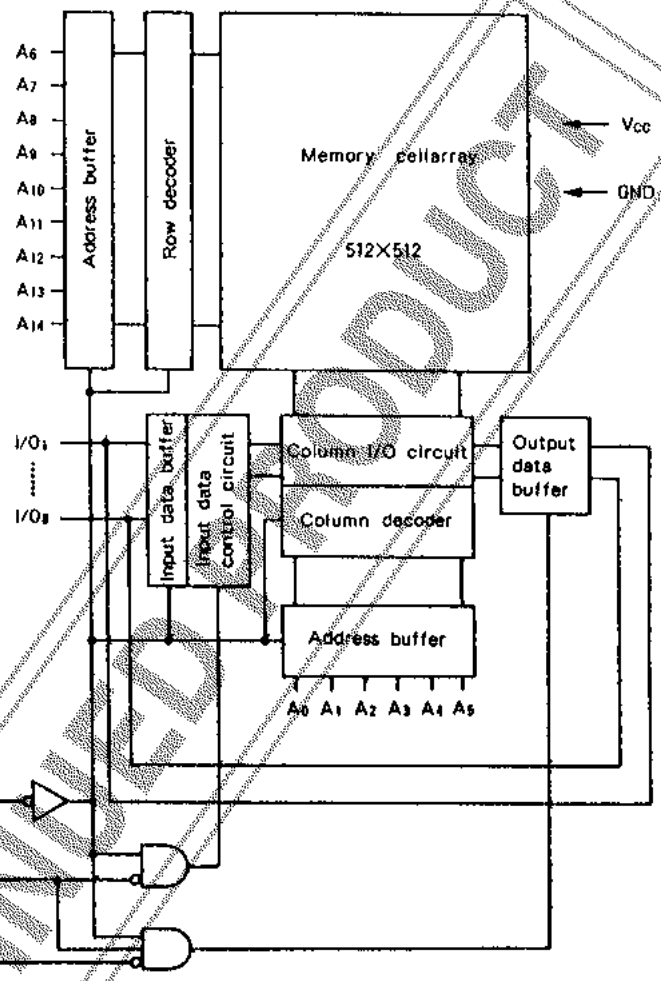
SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

■ Pin Assignment

TOP VIEW



■ Block Diagram



A_0 to A_{14} :Address input
$\overline{WE}$:Read/write control input
$\overline{OE}$:Output enable input
$\overline{CE}$:Chip enable input
I/O_1 to I/O_8 :Data input/output
Vcc,GND :Power supply pin

■ Functional Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read Cycle	L	L	H	Data output	I_{CCA}
Write Cycle	L	X	L	Data input	I_{CCA}
Output Disable	L	H	H	High impedance	I_{CCA}
Nonselect	H	X	X	High impedance	I_{CCS}

X : H or L

■ Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits		unit
Maximum Supply Voltage	Vcc max			+7.0	V
Input Pin Voltage	VIN			−0.5~Vcc+0.5	V
I/O Pin Voltage	VI/O			−0.5~Vcc+0.5	V
Allowable Power Dissipation	Pd max	Ta=+70℃	DIP	1.0	W
			SOP	0.7	
Operating Temperature	Topg			0~+70	℃
Storage Temperature	Tstg			−55~+125	℃

■ DC Allowable Operating Conditions at Ta=0 to +70℃

Parameter	Symbol	min	typ	max	unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Input 'H'-Level Voltage	VIH	2.2		Vcc+0.3	V
Input 'L'-Level Voltage	VIL	−0.3		0.8	V

■ DC Electrical Characteristics at Ta=0 to +70℃, Vcc=5V±10%

Parameter	Symbol	Condition		min	typ*	max	unit
Input Leak Current	ILI	VIN=0~Vcc		−1.0		1.0	μA
I/O Leak Current	ILO	$\overline{CE}$=VIH or $\overline{OE}$=VIH or $\overline{WE}$=VIL, VI/O=0~Vcc		−1.0		1.0	μA
Output 'H'-Level Voltage	VOH	IOH=−1.0mA		2.4			V
Output 'L'-Level Voltage	VOL	IOL=2.1mA				0.4	V
Operating Supply Current (DC)	ICCA1	$\overline{CE}$≤0.2V, II/O=0mA, VIN≤0.2V or VIN≥Vcc−0.2V				15	mA
	ICCA2	$\overline{CE}$=VIL, II/O=0mA, VIN=VIH or VIL				15	mA
Average Operating Supply Current	ICCA3	$\overline{CE}$=VIL, II/O=0mA, min cycle				70	mA
Standby Supply Current	ICCS1	$\overline{CE}$≥Vcc−0.2V, VIN=0~Vcc	LC36256PL,PML-10/12/15		2	100	μA
			LC36256P,PM-10/12/15			1	mA
	ICCS2	$\overline{CE}$=VIH, VIN=0~Vcc				3	mA

*:Reference value at Vcc=5V, Ta=+25℃

■ Input/Output Capacitance at Ta=+25℃, f=1MHz

Parameter	Symbol	Condition	min	typ	max	unit
Input/Output Capacitance	CI/O	VI/O=0V			10	pF
Input Capacitance	CIN	VIN=0V			5	pF

Note)The values shown above are based on sampling inspection.

■ AC Electrical Characteristics at Ta=0 to +70℃, Vcc=5V±10%

AC Test Conditions

Input pulse voltage level	:0.6V, 2.4V
Input rise/fall time	:5ns
Input/output timing level	:1.5V
Output load	:1TTL gate + C_L = 100pF (Including jig capacitance)

Read Cycle

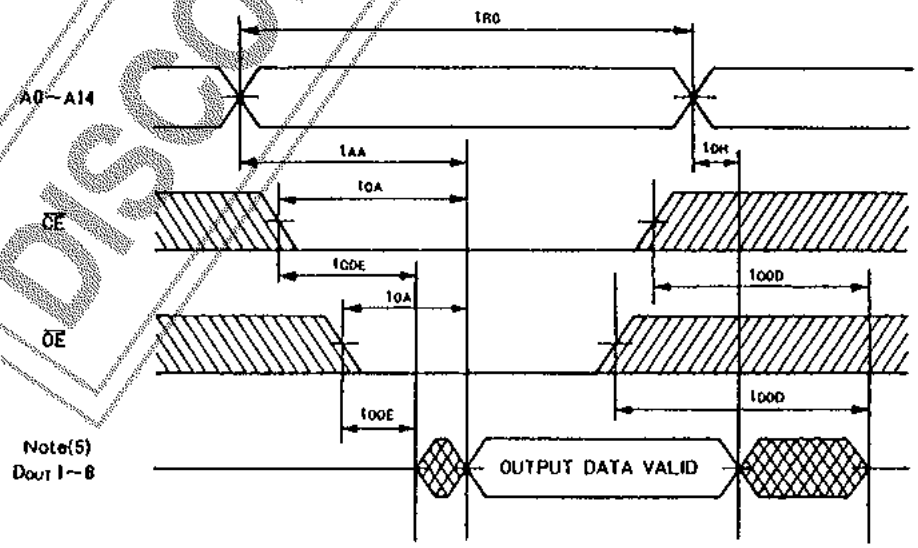
Parameter	Symbol	LC36256P, PL, PM, PML-10		LC36256P, PL, PM, PML-12		LC36256P, PL, PM, PML-15		unit
		min	max	min	max	min	max	
Read Cycle Time	tRC	100		120		150		ns
Address Access time	tAA		100		120		150	ns
$\overline{CE}$ Access Time	tCA		100		120		150	ns
$\overline{OE}$ Access Time	tOA		50		60		70	ns
Output Hold Time	tOH	10		10		10		ns
$\overline{CE}$-Output Enable Time	tCOE	10		10		10		ns
$\overline{OE}$-Output Enable Time	tOOE	5		5		5		ns
$\overline{CE}$-Output Disable Time	tCOD		35		40		50	ns
$\overline{OE}$-Output Disable Time	tOOD		35		40		50	ns

Write Cycle

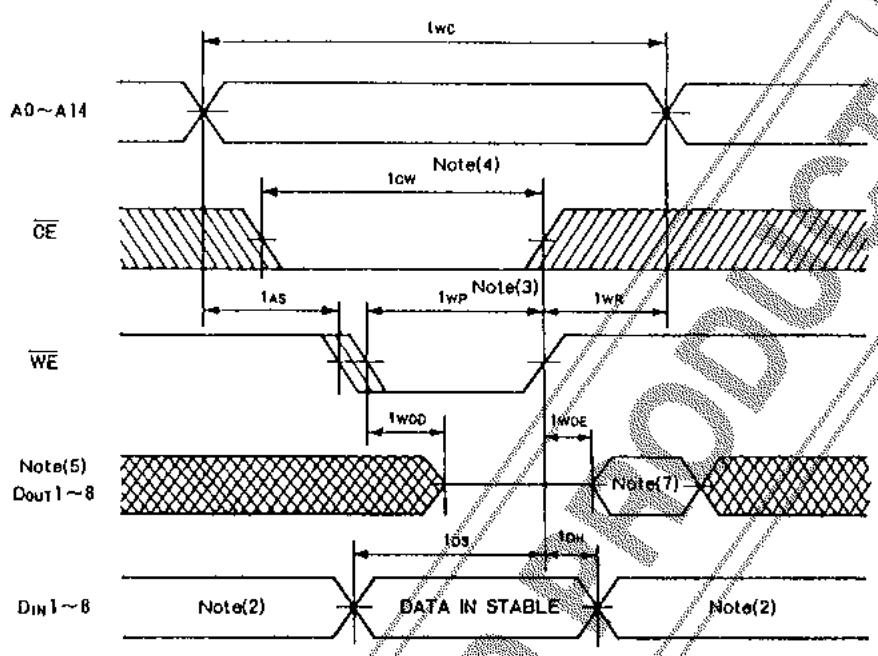
Parameter	Symbol	LC36256P, PL, PM, PML-10		LC36256P, PL, PM, PML-12		LC36256P, PL, PM, PML-15		unit
		min	max	min	max	min	max	
Write Cycle TIme	tWC	100		120		150		ns
Address Setup Time	tAS	0		0		0		ns
Write Pulse Width	tWP	70		80		90		ns
$\overline{CE}$ Setup Time	tCW	80		90		100		ns
Write Recovery Time	tWR	0		0		0		ns
Data Setup Time	tDS	40		50		60		ns
Data Hold Time	tDH	0		0		0		ns
$\overline{WE}$-Output Enable Time	tWOE	10		10		10		ns
$\overline{WE}$-Output Disable time	tWOD		35		40		50	ns

Timing Chart

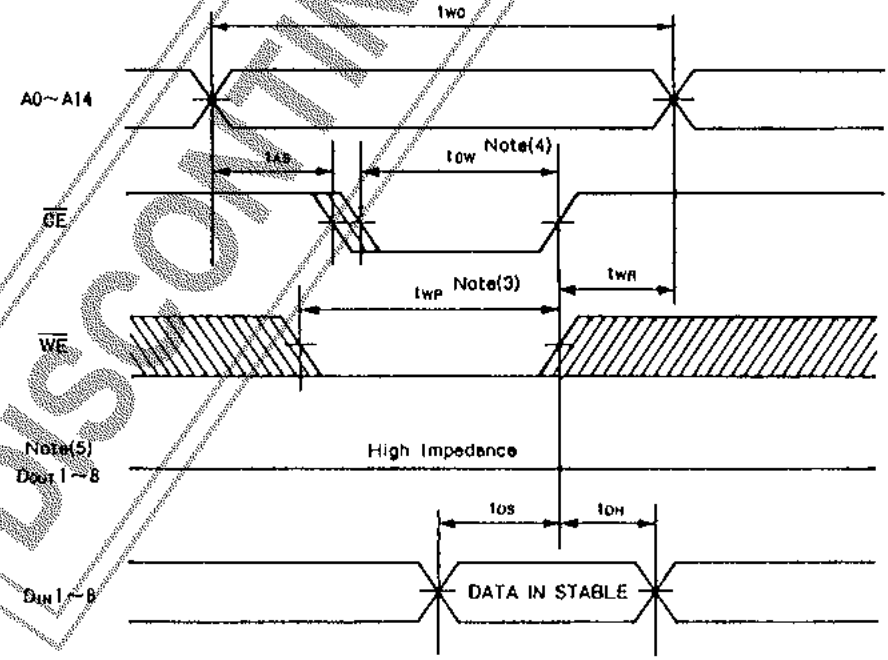
[Read Cycle] Note(1)



[Write Cycle 1] ($\overline{WE}$ Write) Note(6)



[Write Cycle 2] ($\overline{CE}$ Write) Note(6)



Note) (1) $\overline{WE}$ must be high during read cycle.
(2) When D_{OUT} is in the output state, no opposite polarity signal must be applied externally.
(3) t_{WP} occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. t_{WP} is measured from $\overline{WE}$ going low to the earlier of $\overline{CE}$ going high.
(4) t_{CW} occurs during the overlap of a low $\overline{CE}$ and A low $\overline{WE}$. t_{CW} is measured form $\overline{CE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
(5) D_{OUT} is in a high impedance state when $\overline{OE}$ is high or $\overline{CE}$ is high or $\overline{WE}$ is low.
(6) When $\overline{OE}$ is high during write cycle, D_{OUT} is in a high impedance state.
(7) D_{OUT} has the same polarity as write data of this write cycle.

■ Data Retention Characteristics at Ta=0 to +70°C

Parameter	Symbol	Condition		min	typ*	max	unit
Data Retention Supply Voltage	V_{DR}	$V_{\overline{CE}} \geq V_{CC}-0.2V$		2.0		5.5	V
Data Retention Supply Current	I_{CCDR}	$V_{CC}=3.0V$	LC36256PL,PML-10/12/15		1.0	50	μA
		$V_{\overline{CE}} \geq V_{CC}-0.2V$	LC36256P, PM-10/12/15			500	μA
Chip Enable Setup Time	t_{CDR}			0			ns
Chip Enable Hold Time	t_R			t_{RC}**			ns

*Reference value at Ta=+25°C **t_{RC}=Read Cycle Time

Data Retention Waveform