L64010
L64011
L64012
16-Bit HCMOS Multiplier-Accumulators

LSI LOGIC

Description

The L64010 replicates industry standard functionality and pinout for a 64-pin DIP package. It includes a full product register preload feature.

The L64011 replicates industry standard functionality in a 64-pin DIP package without product register preload. In addition, it contains a feedthrough (FT) pin which controls an optional output (pipeline) register which greatly reduces output delay time.

The L64012 replicates industry standard functionality and pinout for a 68-pin chip carrier package. Three pins normally reserved for VDD and GND are used as optional signal pins. These pins allow the device to operate in pipelined mode as in the L64011, as well as allow serial scan operation of all input and output registers. Serial scan is useful for board and system level testing.

Features

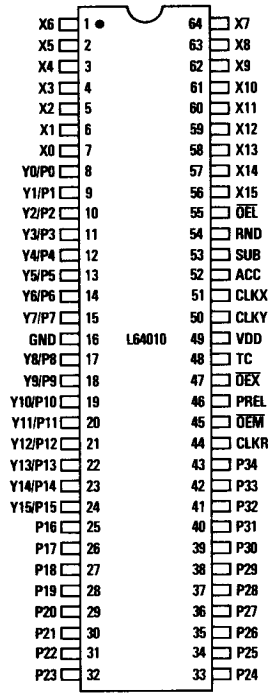
- 16 × 16-bit parallel multiplication and product accumulation
- 1.5-micron drawn (1.0-effective) gate length HCMOS process for high speed and low power
- Pin-for-pin replacement for AMD29510, TRW TDC1010, WTL2010, (L64010, L64012)
- Optional pipeline register to decrease output delay (L64011, L64012)
- Multiply-accumulate time

L64010/11/12	45 ns commercial
	60 ns military
L64010A/11A/12A	30 ns commercial
	40 ns military

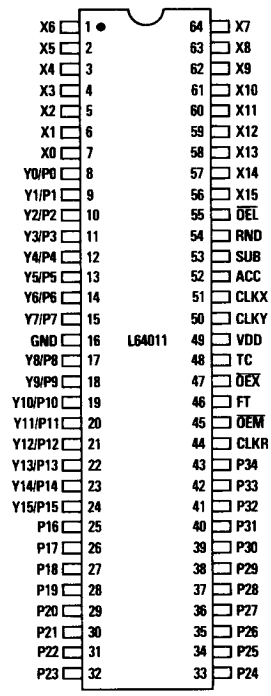
- Full serial scan capability supported by X, Y, instruction and output registers (L64012)
- Full 35-bit product register may be directly preloaded in one clock cycle (L64010, L64012)
- 2000 V ESD protection
- All three circuits designed using MACGEN™ Megacell Compiler™

Pin Diagrams (Top View)

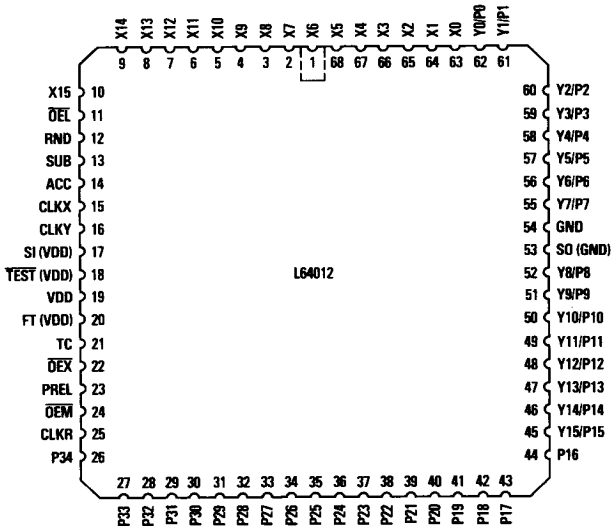
L64010
64-Pin CDIP



L64011
64-Pin CDIP



L64012
68-Pin LCC



Note:
Pin assignments in parentheses indicate pinout for industry standard functionality (no pipeline, no scan).

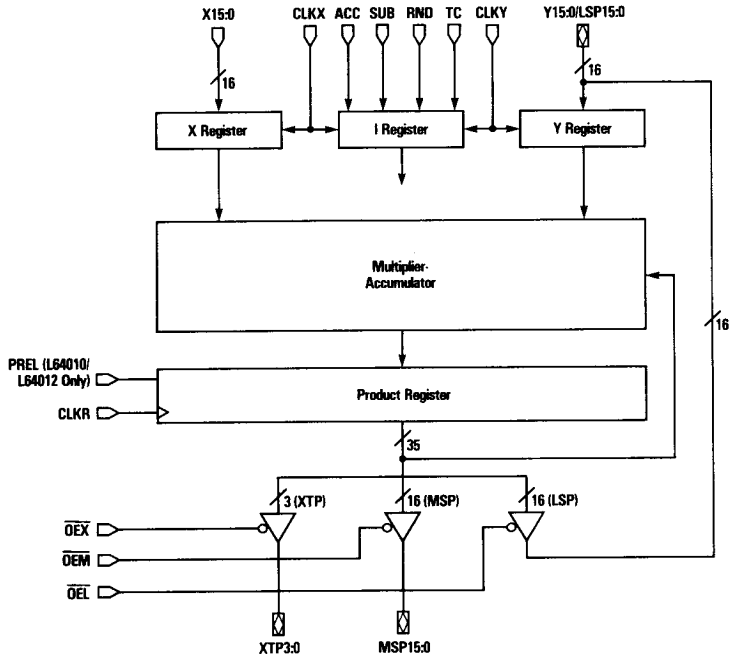
October 1987

Order Number L64010

Logic Block Diagrams

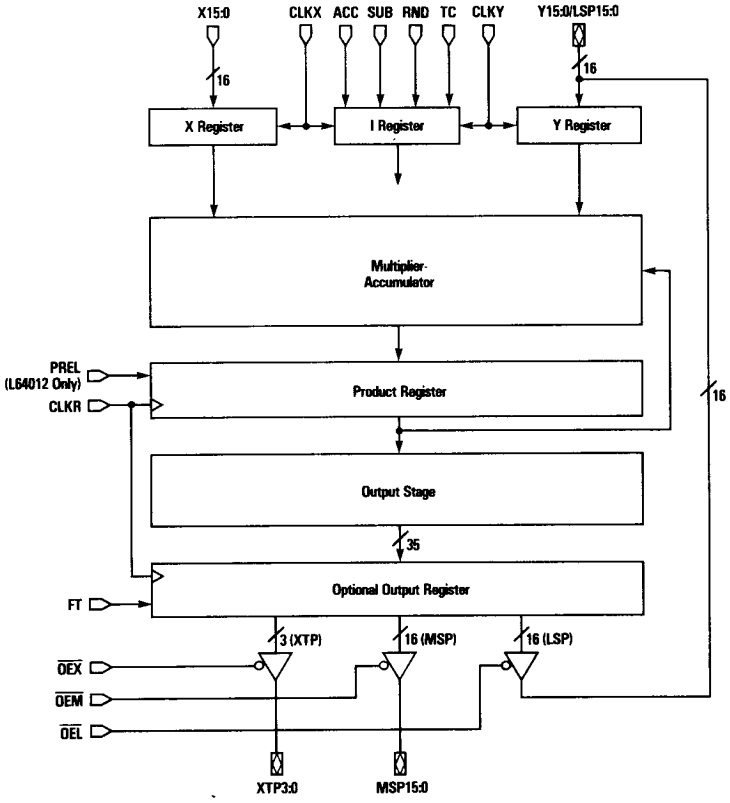
Industry Standard Operation

L64010 (All Modes)
L64011 (FT = HIGH)
L64012 (FT = HIGH, $\overline{TEST}$ = HIGH)



Pipelined Operation

L64011 (FT = LOW)
L64012 (FT = LOW, $\overline{TEST}$ = HIGH)



L64010/11/12 Product Matrix

Device	Package	Industry Standard Pinout	Preload	Pipeline Register	Scan Test
L64010	64CDIP	X	X		
L64011	64CDIP	X		X	
L64012	68LCC or 68PGA	X	X	X	X

Description

The L64010, L64011 and L64012 are three high speed 16 × 16-bit parallel multiplier-accumulators. They are fabricated with a 1.5-micron drawn gate length HCMOS process. Multiplier-accumulators have been designed using modified Booth encoding, Wallace tree adders and a high-speed carry-select adder.

These devices are useful in Digital Signal Processing (DSP) applications such as Fast Fourier Transforms (FFTs), digital filtering, power expansion and correlations. They are also useful for general computational tasks such as matrix manipulations, graphics and image processing as well as arithmetic acceleration.

Two 16-bit input registers are provided for the X and Y operands. A third register stores four instruction inputs, TC, RND, ACC and SUB. The instruction register is clocked when either the X or the Y input register is clocked. TC selects either a two's complement or an unsigned magnitude format for both data inputs. If RND is HIGH, a "1" is added to the MSB of the LSP (position P15). The 32-bit multiplier product is zero-filled or sign-extended as appropriate and passed as a 35-bit number to the accumulator.

The operation of the accumulator is controlled by the signals ACC, SUB and PREL. ACC and SUB are registered whenever the X or Y registers are clocked. ACC in conjunction with SUB selects one of the first three accumulator functions (see Pipeline/Accumulation Function Table). For preloading purposes the accumulator is considered in three sections: Extended Product (XTP, P34–P32) controlled by $\overline{OEX}$, Most Significant Product (MSP, P31–P16) controlled by $\overline{OEM}$, and Least Significant Product (LSP, P15–P0) controlled by $\overline{OEL}$. When PREL is LOW these controls are active-LOW Output Enables for 3-state output buffers. When PREL is HIGH the output buffers go to high impedance and $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ select a portion of the product register for preloading. Preloading of data applied to the bidirectional P port occurs at the rising edge of CLKR.

The L64012 contains full single phase scan test circuitry. Scan test is a system level test technique which allows the internal state of a device to be observed through a minimum of I/O pins. Scan test is invoked by holding the $\overline{TEST}$ input LOW. The output register, X register, instruction register and Y register all operate as linked serial shift registers. Data can be placed into any of these registers through the Scan Input (SI) pin. Similarly, data can be clocked through these registers and observed through the Scan Output (SO) pin.

This scan test technique is identical to the one available for LSI Logic cell-based megacells and memories. When combined on a board or in a system, this single phase scan system provides a fully integrated system level test scheme allowing full chip level diagnostics and fault isolation.

Pin Listing and Description

X15:0
16-bit data input. Data are loaded into the X register on the rising edge of CLKX.

Y15:0/P15:0
16-bit data input/output. Data are loaded into the Y register on the rising edge of CLKY. These pins also serve as the product output for the Least Significant Product (LSP) as well as an input to preload the LSP register. The LSP is preloaded on the rising edge of CLKR.

P31:16
16-bit data input/output. Product output for the Most Significant Product (MSP) as well as an input to preload the MSP section of the product register (the MSP is preloaded on the rising edge of CLKR) with PREL = HIGH and $\overline{OEM}$ = HIGH.

P34:32
Three-bit data input/output. Product output for the extended product (XTP) as well as an input to preload the XTP section of the product register (the XTP is preloaded on the rising edge of CLKR) with PREL = HIGH and OEX = HIGH.

CLKX, CLKY
Clocks for the X and Y registers respectively. Both load data on the rising edge of the clock. The instruction register (for TC, RND, ACC and SUB) is loaded on the rising edge of either CLKX or CLKY.

CLKR
Clock for the product register and optional output register. Data are loaded into both registers on the rising edge of the clock.

TC (Two's Complement)
When TC is HIGH, both the X and Y data inputs are interpreted as two's complement numbers, otherwise both data inputs are interpreted as unsigned. The TC control input is loaded on the rising edge of either CLKX or CLKY.

RND (Round)
When RND is HIGH a "1" is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP) to round MSP and XTP data upwards. The RND control input is loaded on the rising edge of either CLKX or CLKY.

SUB (Subtract)
When both ACC and SUB are HIGH, the contents of the product register are subtracted from the current multiplier product and the difference is stored back into the product register at the next rising edge of CLKR. When ACC is HIGH and SUB is LOW, addition instead of subtraction is performed. When ACC is LOW, the device will act as a simple multiplier, regardless of SUB. SUB is loaded on the rising edge of either CLKX or CLKY.

ACC (Accumulate)
When ACC is HIGH, the multiplier product is added to or accumulated with the results in the product register. The sign of this operation is affected by the SUB input control. ACC is loaded on the rising edge of either CLKX or CLKY.

PREL (Preload)—L64010, L64011 Only
The PREL input works in conjunction with any corresponding output enable ($\overline{OEL}$, $\overline{OEM}$, $\overline{OEX}$) input. When PREL is HIGH, all output buffers are at high impedance (High-Z). When $\overline{OEL}$, $\overline{OEM}$ or $\overline{OEX}$ are also HIGH, the preload data present at the corresponding set of output pins is loaded into the product register at the rising edge of CLKR.

$\overline{OEL}$, $\overline{OEM}$ and $\overline{OEX}$ (Output Enables)
$\overline{OEL}$, $\overline{OEM}$ and $\overline{OEX}$ are the 3-state output enables for the LSP, MSP and XTP respectively. Device outputs are enabled when PREL is LOW and the appropriate output enable is also LOW. $\overline{OEL}$, $\overline{OEM}$ and $\overline{OEX}$ are non-registered control signals.

FT (Feedthrough)—L64011, L64012
When FT is LOW, a pipeline register is inserted into the output section, reducing output delay time. When HIGH, FT allows the output register to be bypassed, disabling the final pipeline stage and allowing the device to operate exactly as an industry standard (non-pipelined) architecture.

$\overline{TEST}$—L64012
When LOW, the X, Y, instruction and output registers operate in a scan test mode to form a scan chain. Scan registers are clocked via the normal input clocks for each set of registers.

SI, SO (Scan Input, Scan Ouput)—L64012
Scan input and scan output respectively for the scan chain during test mode.

X and Y Data Input Formats

	15	14	13	•••	2	1	0
Unsigned Integer (TC = 0)	2^{15}	2^{14}	2^{13}	•••	2^{2}	2^{1}	2^{0}
Two's Complement Integer (TC = 1)	-2^{15} (Sign)	2^{14}	2^{13}	•••	2^{2}	2^{1}	2^{0}
Unsigned Fractional (TC = 0)	2^{-1}	2^{-2}	2^{-3}	•••	2^{-14}	2^{-15}	2^{-16}
Two's Complement Fractional (TC = 1)	-2^{0} (Sign)	2^{-1}	2^{-2}	•••	2^{-13}	2^{-14}	2^{-15}

Numerical Output Formats

Unsigned Integer Output

XTP			MSP														LSP															
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Two's Complement Integer Output

XTP			MSP														LSP															
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{34} (Sign)	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Output

XTP			MSP														LSP															
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Two's Complement Fractional Output

XTP			MSP														LSP															
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{4} (Sign)	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

Pipeline/Accumulation Function Table

Control Inputs				Product Register	Optional Output Register	Comments	
FT	PREL	ACC	SUB				
H	L	L	X	Q	Transparent	Load Product Register	Industry Standard Operation Product Register feeds directly to outputs of device
H	L	H	L	Q	Transparent	Positive Accumulation in Product Register	
H	L	H	H	Q	Transparent	Negative Accumulation in Product Register	
H	H	X	X	PL	Transparent	Preload Product Register	
L	L	L	X	Q	Q+1	Load Product Register	Pipelined Operation Insertion of Output Register into output path decreases output delay. Output Register contains Product Register data which has been delayed by one clock cycle.
L	L	H	L	Q	Q+1	Positive Accumulation in Product Register	
L	L	H	H	Q	Q+1	Negative Accumulation in Product Register	
L	H	X	X	PL	Q+1	Preload Product Register	

Q = Product Register loaded with current data on rising edge of CLKR.
Q+1 = Output Register loaded with data delayed by one clock cycle on rising edge of CLKR (Pipeline Mode).
PL = Product Register loaded with Preload data on rising edge of CLKR.

Preload Function Truth Table

Control Inputs				Product Register			Comments
PREL	OEX	OEM	OEL	XTP P35:32	MSP P31:16	LSP P15:0	
L	L	L	L	Q	Q	Q	Standard Operation
L	L	L	H	Q	Q	Z	
L	L	H	L	Q	Z	Q	
L	L	H	H	Q	Z	Z	
L	H	L	L	Z	Q	Q	
L	H	L	H	Z	Q	Z	
L	H	H	L	Z	Z	Q	
L	H	H	H	Z	Z	Z	
H	L	L	L	Z	Z	Z	Preload Operation
H	L	L	H	Z	Z	PL	
H	L	H	L	Z	PL	Z	
H	L	H	H	Z	PL	PL	
H	H	L	L	PL	Z	Z	
H	H	L	H	PL	Z	PL	
H	H	H	L	PL	PL	Z	
H	H	H	H	PL	PL	PL	

Z = Output buffers disabled (High-Z).
Q = Output buffers enabled. Contents of output register (pipelined operation) or product register (non-pipelined operation) available at outputs.
PL = Outputs disabled (High-Z). Preload data present at the output pins will be loaded into the product register at the rising edge of CLKR.

Note:
The L64010 and L64012 do not support partial preloading of the product register. It is recommended that all 35 bits of the product register should be preloaded simultaneously. If the preload operation must occur in stages, then the LSP must be preloaded before the MSP and the MSP preloaded before the XTP. This ensures proper carry operation.

Operating Characteristics

Absolute Maximum Ratings (Referenced to GND)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	−0.3 to +7	V
Input Voltage	VIN	−0.3 to VDD +0.3	V
DC Input Current	IIN	±10	mA
Storage Temperature Range	TSTG	−65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+3 to +6	V
Operating Ambient Temperature Range Military	TA	−55 to +125	°C
Industrial Range	TA	−40 to +85	°C
Commercial Range	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges[1]

Symbol	Parameter	Condition			Min	Typ	Max	Units
VIL	Low Level Input Voltage						0.8	V
VIH	High Level Input Voltage							
	Commercial Temperature Range				2.2			V
	Military and Industrial Temperature Range				2.3			V
IIN	Input Current	VIN = VSS			−350		−35	μA
VOH	High Level Output Voltage		Comm	Mil				
		IOH =	−4 mA	−3.2 mA	2.4	4.5		V
VOL	Low Level Output Voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOZ	3-State Output Leakage Current	VOH = VSS or VDD			−10	±1	10	μA
IOS	Output Short Circuit Current[2]	VDD = Max, VO = VDD			25		140	mA
		VDD = Max, VO = 0V			−15		−100	mA
IDDQ	Quiescent Supply Current	VIN = VDD or VSS					10	mA
IDD	Operating Supply Current	tMA = tCYCLE = 50 ns				160		mA
CIN	Input Capacitance	Any Input				5		pF
COUT	Output Capacitance	Any Output				10		pF

Notes:
1. Military temperature range is −55°C to +125°C, ±10% power supply; industrial temperature range is −40°C to +85°C, ±5% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. All inputs contain pull-up resistors.

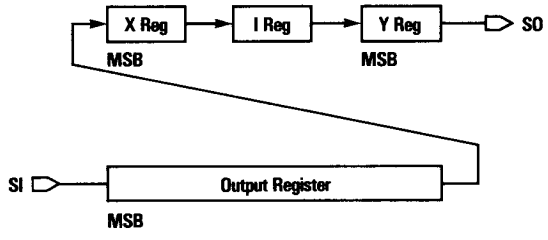
AC Switching Characteristics: Commercial Temperature Range (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V) $\overline{\text{TEST}}$ = HIGH for L64012

Symbol	Parameter	L64010/11/12		L64010A/11A/12A		Units	Notes
		Min	Max	Min	Max		
tMA	Multiply-Accumulate Cycle Time		45		30	ns	
tIS	Input Data Setup Time	10		7		ns	
tIH	Input Data Hold Time	6		3		ns	
tIPW	Input Register Minimum Pulse Width	15		10		ns	
tODP	Output Delay from CLKR (Pipelined)		30		20	ns	CL = 50pF
tOD	Output Delay from CLKR		50		45	ns	
tOPW	Output Register Minimum Pulse Width (CLKR)	15		15		ns	
tOE	Output Enable Time		40		35	ns	
tOZ	Output Disable Time		35		30	ns	
tSPREL	Setup Time During Preload	10		10		ns	
tHPREL	Hold Time During Preload	6		3		ns	

AC Switching Characteristics: Military Temperature Range (TC = 55°C to +125°C, VDD = 4.5 V to 5.5 V) $\overline{\text{TEST}}$ = HIGH for L64012

Symbol	Parameter	L64010/11/12		L64010A/11A/12A		Units	Notes
		Min	Max	Min	Max		
tMA	Multiply-Accumulate Cycle Time		60		40	ns	
tIS	Input Data Setup Time	15		10		ns	
tIH	Input Data Hold Time	8		5		ns	
tIPW	Input Register Minimum Pulse Width	15		15		ns	
tODP	Output Delay from CLKR (Pipelined) L64011/L64012 Only		35		25	ns	CL = 50pF
tOD	Output Delay from CLKR		60		55	ns	
tOPW	Output Register Minimum Pulse Width (CLKR)	20		20		ns	
tOE	Output Enable Time		45		40	ns	
tOZ	Output Disable Time		40		35	ns	
tSPREL	Setup Time During Preload	15		15		ns	
tHPREL	Hold Time During Preload	5		5		ns	

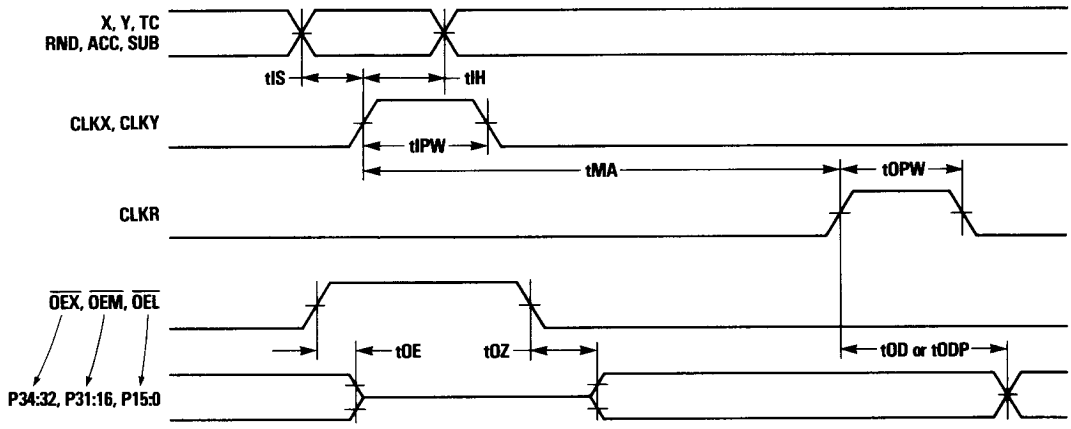
Logic Diagram—Scan Chain
L64012 Only ($\overline{\text{TEST}}$ = LOW)



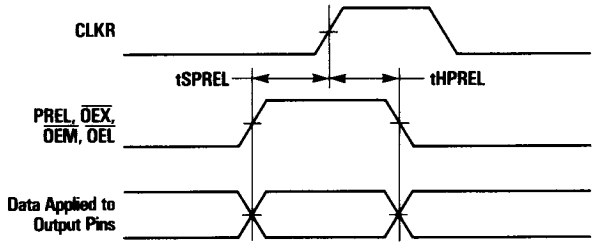
Notes:
1. I Register scan order is: TC, ACC, SUB, RND.
2. Register control clocks act as scan clocks.
3. Apply CLKY at or before CLKX. Apply CLKX at or before CLKR.

AC Timing Waveforms

Normal Operation ($\overline{TEST}$ = HIGH)

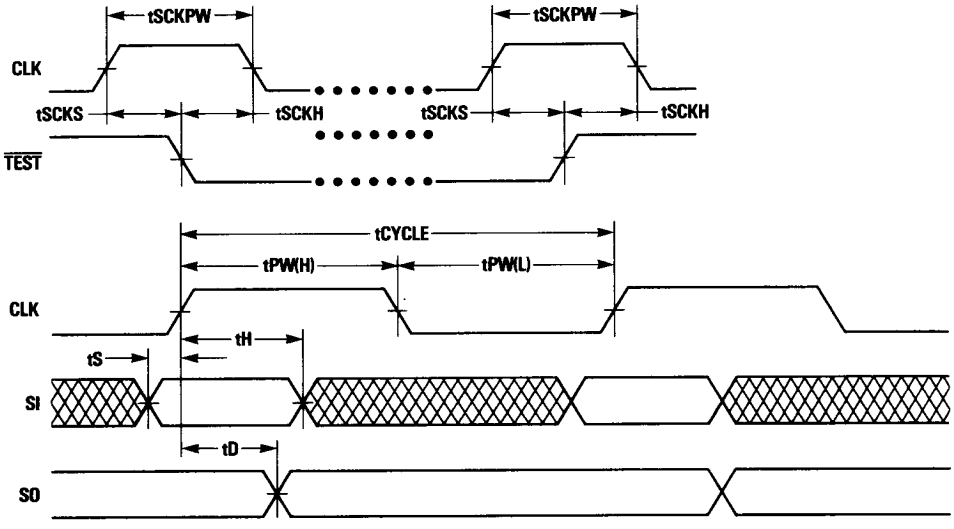


PRELOAD Operation–L64010, L64012 Only ($\overline{TEST}$ = HIGH)



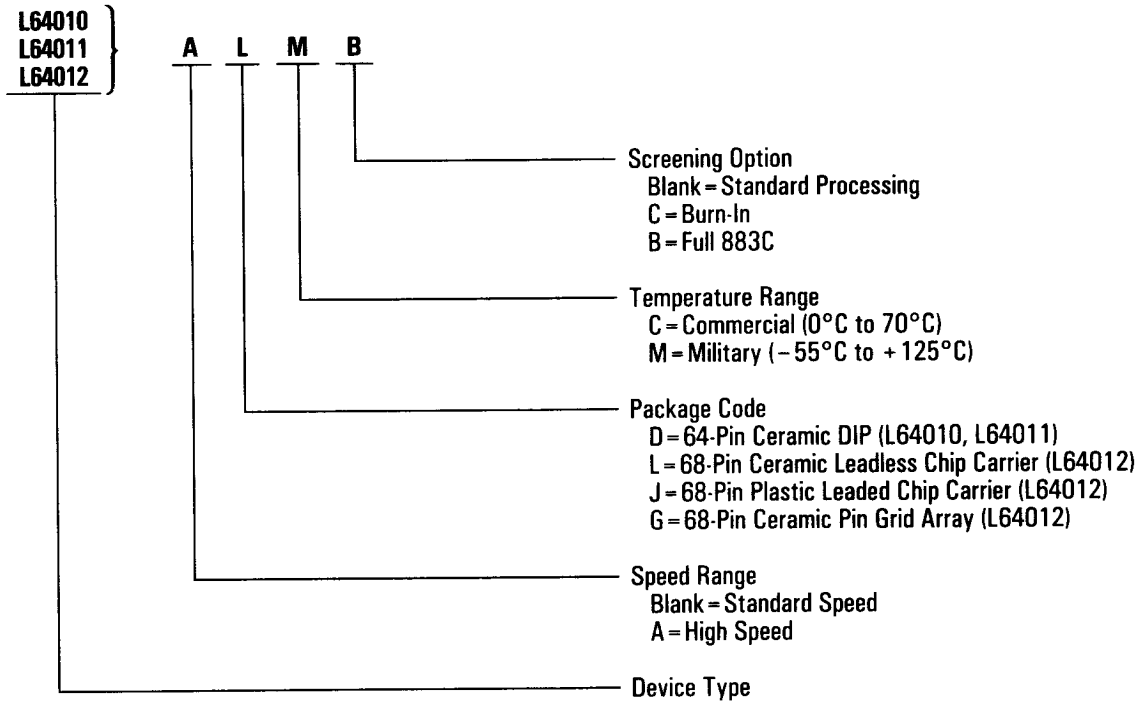
Scan Test Timing Waveforms

L64012 Only ($\overline{TEST}$ = LOW)



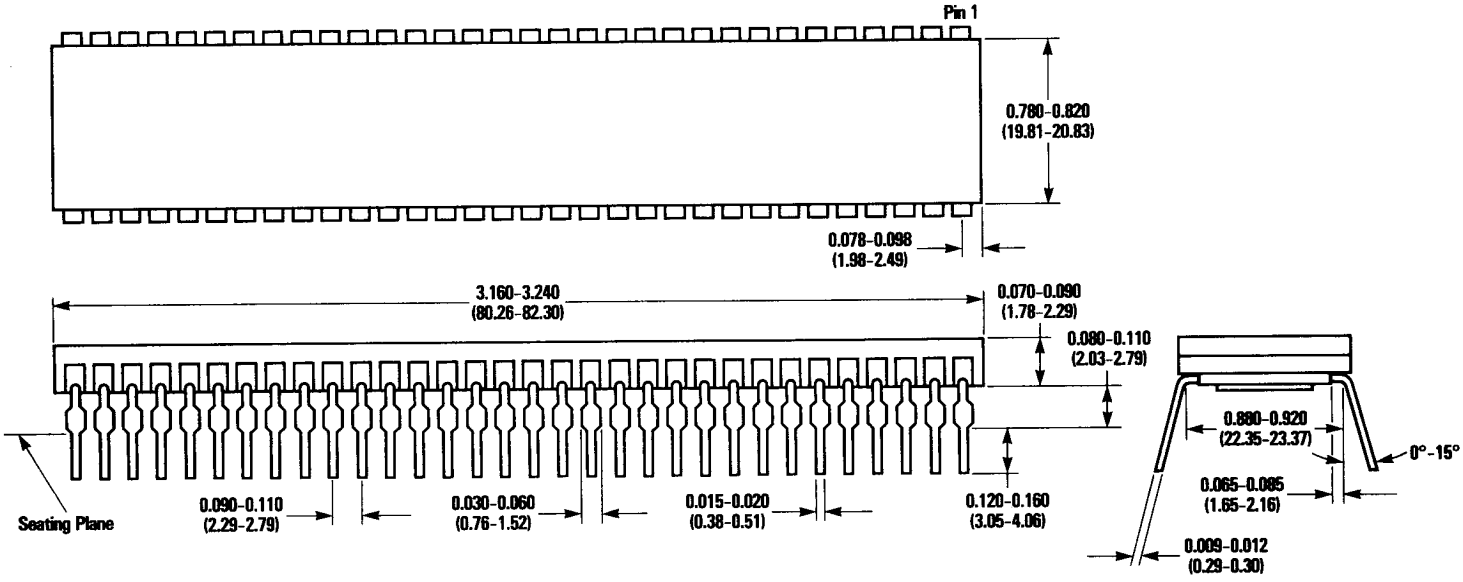
Notes:
1. During scan, all clocks must be tied together.
2. All clocks should be HIGH while entering and leaving TEST mode.
3. tCYCLE is 75 ns commercial, 100 ns military.

Ordering Information



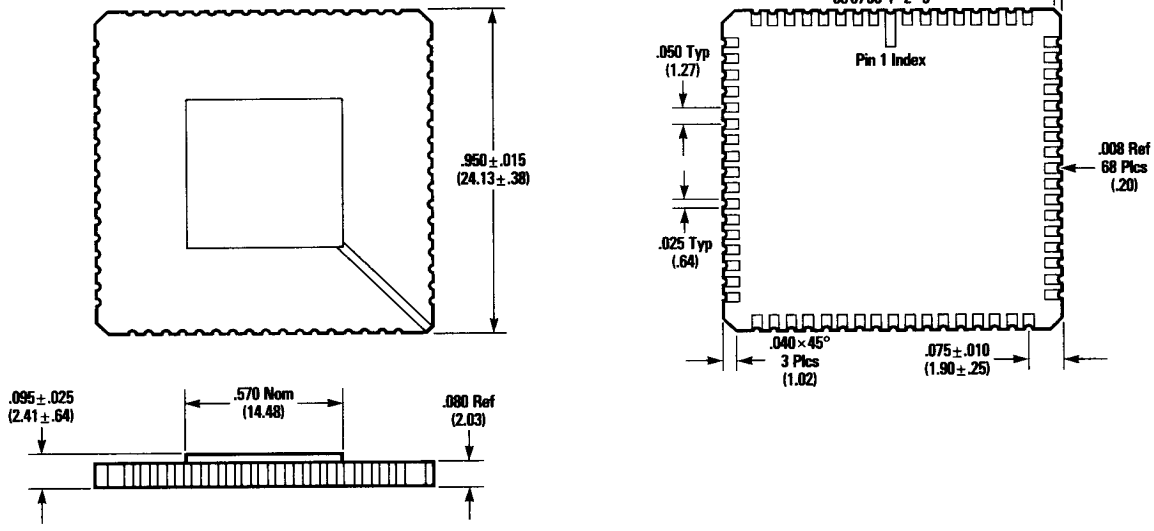
Package Drawings

64-Lead (900 MIL) CerDIP



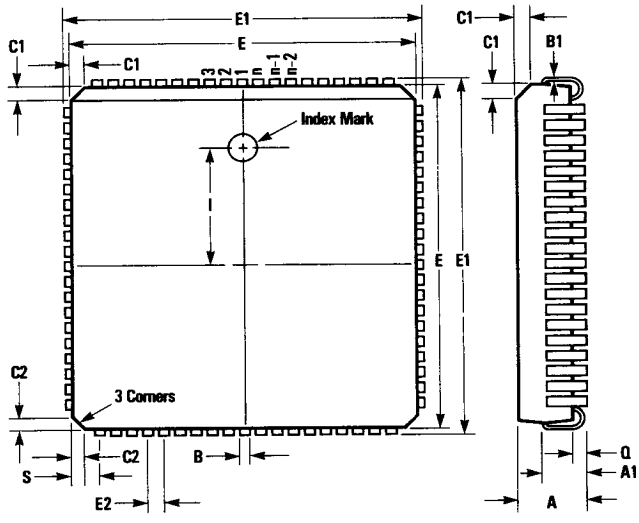
Package Drawings

Ceramic Leadless Chip Carrier 68-Pin (MOS type C)



Notes:
1. All exposed metallized area shall be gold plated 60 microinches Min. thickness over 50 microinches Min-350 microinches Max Nickel over refractory metallization.
2. Cap is gold plated kovar or ceramic.
3. Base is Al203.
4. Package dimensions fit within JEDEC outline for 50 mil center line pkgs.

68-Pin Plastic Leaded Chip Carrier



A	Min	.165 (4.19)
	Max	.185 (4.70)
A1	Min	.100 (2.54)
	Max	–
B	Min	.026 (.66)
	Max	.032 (.81)
B1	Ref	.020 (.51)
E	Min	.950 (24.13)
	Max	.958 (24.33)
E1	Min	.985 (25.02)
	Max	.995 (25.27)

E2	Ref	.050 (1.27)
Q	Min	.020 (.51)
	Max	–
S	Ref	.075 (1.90)
C1	Min	.042 (1.07)
	Max	.048 (1.22)
C2	Min	–
	Max	.010 (.25)
I	Ref	.350 (8.89)
Notes		1,2,3,4

Notes:
1. Pins are tin plated or hot solder dipped (increase B1 MAX by .003" (.08)) copper or Alloy 42.
2. Pin foot print matches that of ceramic chip carrier JEDEC Type A.
3. Package can be surface mounted or socketed.
4. Package dimensions fit within the JEDEC outline.

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008361 KLR

Printed in USA
097.83.DS036.20K.IM.CC