HUGHES
HUGHES AIRCRAFT COMPANY
SOLID STATE PRODUCTS

AUTO-REFRESH CMOS LCD DRIVER

HLCD 0515

DESCRIPTION

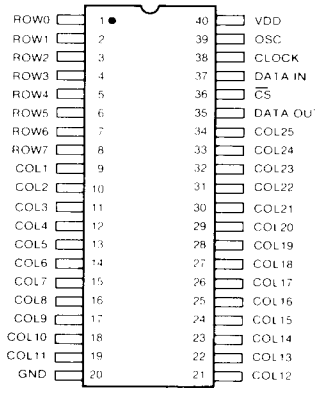
The HLCD 0515 is a CMOS driver for multiplexed Liquid Crystal Displays. Each unit is capable of driving an LCD matrix of up to 8 rows × 25 columns. This display could be a graphic array, custom array, or 5 characters in a 5 × 7 format. Multiple units may be cascaded for displays with more rows and/or more columns. The input is in a serial format (data is loaded in one row at a time) and requires the user to specify the on/off state of each pixel. Therefore, the user has great flexibility in displaying the shapes and figures he needs. The HLCD 0515 provides all the multi-level AC waveforms necessary for the LCD driver, automatically refreshes the display, and interfaces directly with most microprocessors and microcomputers.

The HLCD 0515 operates over ~~5-10~~ 5-10 volt range. The Driver is available in a 40 pin dual-in-line ceramic package (D suffix) or plastic package (P suffix). Unpackaged dice (H suffix) are available upon request.

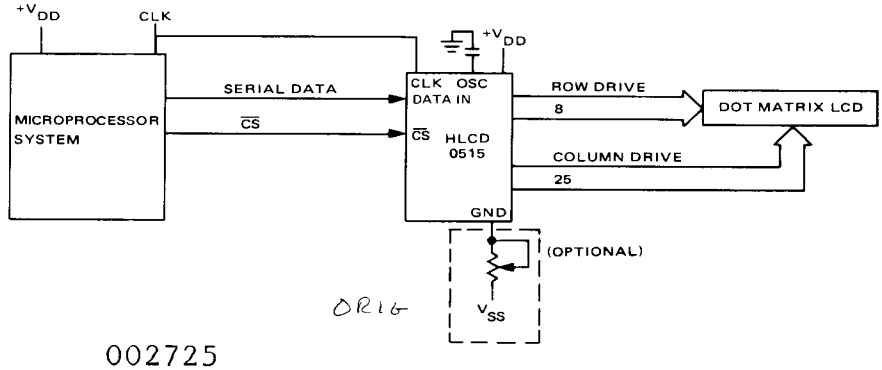
FEATURES

- CMOS circuitry
  - Low power dissipation
  - Wide temperature range
  - Wide supply variation
- Microprocessor compatible
- CMOS and NMOS compatible
- Drives an 8 × 25 multiplexed LCD
- Automatic display refresh
- On-Chip oscillator
- Power down/blank display mode
- Number of rows is selectable from 2 through 8

PIN CONFIGURATION



TYPICAL SYSTEM INTERCONNECT



S-42

ORIG

002725

T-2725

HJG

MAXIMUM RATINGS, *Absolute-Maximum Values*

V_{DD} Supply ..... −.03 to +12V
Input to Voltages ..... V_{DD} −12 to V_{DD} +.3
Storage Temperature ..... −65 to +125°C
Operating Temperature
Plastic Package ..... −40 to +85°C
Ceramic Package ..... −55 to +125°C

STATIC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{DD} = +5V, unless otherwise specified

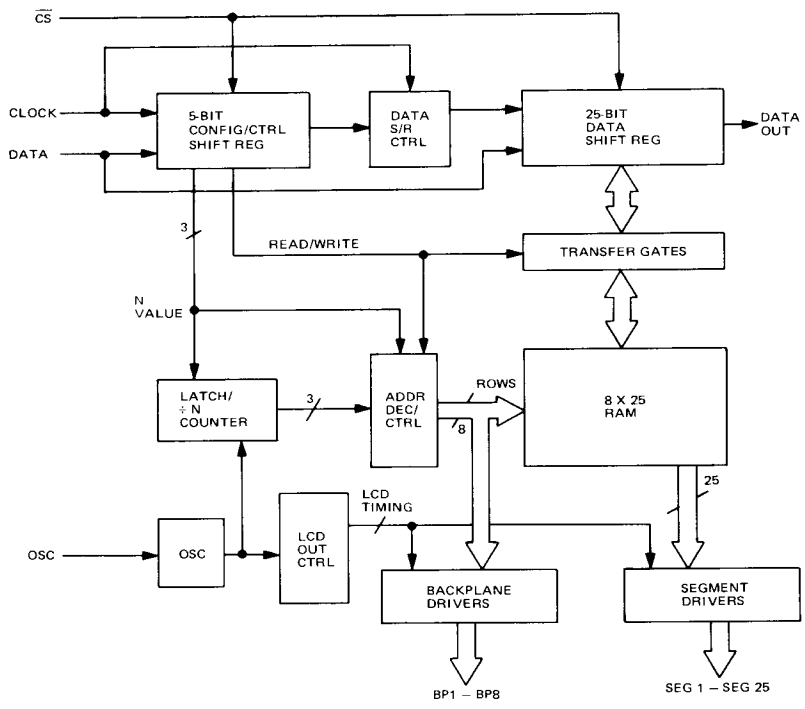
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		4.5		10	V
Supply Current	I_{DD}				900	μA
Input High Level	V_{IH}	entire V_{DD} range	.75 V_{DD}		V_{DD}	V
Input Low Level	V_{IL}		V_{DD}-12		.25V_{DD}	V
Input Leakage	I_L				5	μA
Input Capacitance	C_I				5	pf
Row Output High (Sel)	V_{OH}			V_{DD}		V
Row Output Low (Sel)	V_{OL}			0		V
Row Output High (Unsel)	V_{OUH}			.75 V_{DD}		
Row Output Low (Unsel)[1]				.25 V_{DD}		V
Column Output High	V_{OH}			V_{DD}		V
Column Output Low	V_{OL}			0		V
Column Output (Unsel)	V_{OM}			.5 V_{DD}		V
Data Out High Level	V_{OH}	40 μA	2.4			V
Data Out Low Level	V_{OL}	I_L = 1.6μA			.4	V
Row Output Impedance	R_{OUTR}	I_L = 10μA			10	KΩ
Column Output Impedance	R_{OUTC}	I_L = 10μA			40	KΩ
Offset Voltage	V_{OFF}				50	mV

NOTE 1: See Output Waveforms

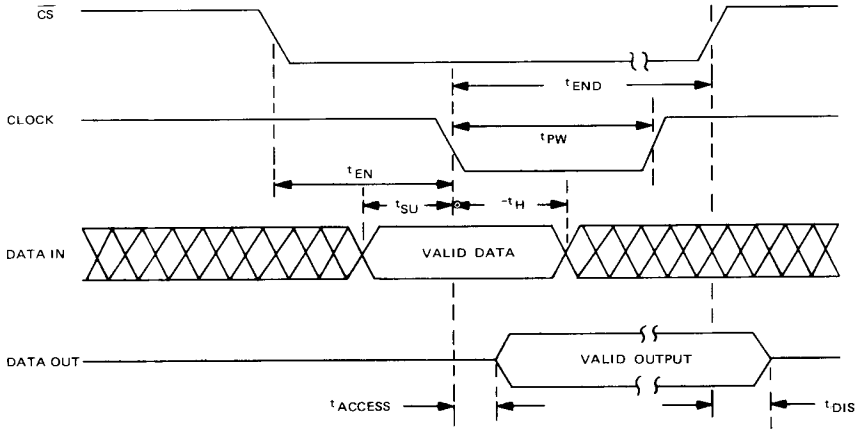
DYNAMIC ELECTRICAL CHARACTERISITICS at T_A = 25°C; V_{DD} = +5V unless otherwise specified

PARAMETER	SYMBOL	MIN	MAX	UNITS
Select enable time, chip select falling edge to clock falling edge	t_{EN}	500		nsec
Data Setup time, data valid prior to clock falling edge	t_{SU}	100		nsec
Data hold time, data valid after clock falling edge	t_H	10		nsec
Output Prop. delay, clock-falling edge to data out valid	t_{ACCESS}		200	nsec
Disable time, chip select rising edge to data out hi-impedance	t_{DIS}		200	nsec
Deselect time delay from clock falling edge to chip select rising edge	t_{END}	250		nsec

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



SELECT AND MODE CONTROL

There are four modes of operation in the HLCD 0515:

1. Write buffer mode
2. Read buffer mode
3. Initialization mode — blank display
4. Initialization mode — visible display

A serial data string is presented to the Data In terminal for any operation. The data format is shown below:

FIRST ◄ SERIAL DATA BITS TO THE DATA IN TERMINAL ► LAST																												
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Row Control (8 rows)			Mode Control		Column Select (25 columns)																							

ROW CONTROL

Data bits 1, 2, and 3 represent the address of the row to be selected or the total number of rows to be selected minus 1 depending on the mode controls. The row control information is in binary and controls 8 rows from 0 through 7. Data bit 1 is the MSB and data bit 3 is the LSB.

MODE CONTROL

Data bits 4 and 5 represent the operational mode to be selected. Each mode is described separately in the Operational Mode Section.

Data bit 4	5	
0	0	Write into RAM storage buffer
0	1	Read from RAM storage buffer
1	0	Initialization with blank display
1	1	Initialization with visible display

COLUMN SELECT

Data bits 6 through 30 represent the 25 individual column bits in the addressed row (bits 1-3) while in the write mode. Data bit 6 corresponds to column ~~25~~, data bit 7 corresponds to column ~~24~~..., data bit 30 corresponds to column ~~1~~ 25 1 2

OPERATIONAL MODES

1. Initialization Mode:

There are two modes available for initialization of the HLCD 0515. The main purpose for initialization is to define the total number of rows to be used in the display, and to make the display visible or blank.

a. Initialization with Blank Display (Bit 4 = 1, Bit 5 = 0)

When this mode is selected, the display is blanked out and the total number of rows are selected via data bits 1, 2 and 3. Column information may or may not be provided. If the column information is provided via data bits 6 through 30, this mode also acts as a write into RAM storage mode writing a row of data into the RAM at the row selected by data bits 1, 2 and 3. (i.e. the last row of the display).

b. Initialization with Visible Display (Bit 4 = 1, Bit 5 = 1)

In this mode, the first three data bits represent (N-1) where N is the total number of rows used in the display. Also it enables the display information to become visible. This mode can be terminated after five data bits, otherwise, it will read the column information of the row that is selected via the data-out line on successive clock inputs (i.e. the last row of the display).

2. Write Mode: (Bit 4 = 0, Bit 5 = 0)

This mode is used to write or update the data into the 8 x 25 RAM storage. Row address is provided by row control data bits 1, 2, and 3, while 25 bit data for each column is provided via data bit 6 through bit 30. The display can be made visible or blank depending upon the initialization mode previously selected.

3. Read Mode: (Bit 4 = 0, Bit 5 = 1)

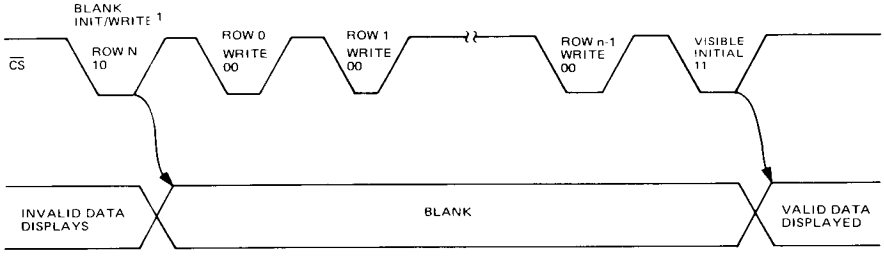
This mode is used to read the data from the 8 × 25 RAM storage and sequentially display it on the Data Out terminal. Row address is provided by row control data bits 1, 2 & 3.

For each row address, column data is shifted serially on Data Out terminal from column 25 to column 1 on each successive clock.

4. Typical Mode Sequence:

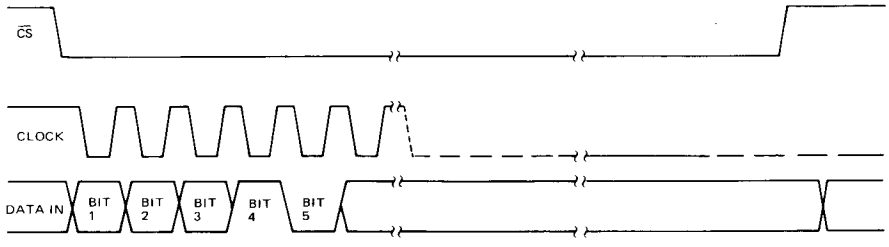
With power on, the display shows random data on the display. The initialization with blank display mode can be selected and the first write can be made on the last row during the same cycle by providing column data on bit 6 through bit 30. Additional write modes will be selected to write into all the rows in the same manner. Once the final row is written, an initialization mode with visible display must be selected.

TYPICAL MODE SEQUENCE & TIMING



NOTE 1: SEE EXPANDED TIMING BELOW

EXPANDED INITIALIZATION/WRITE WITH BLANK DISPLAY (30 BITS)



SYNCHRONIZATION AND CASCADING

To cascade a number of HLCD 0515's, which share rows, all units must be synchronized. This can be done by driving each Osc pin of the HLCD 0515 with the same external signal and initializing all units at the same time.

In Figure A, the HLCD 0515 is used to drive 8 rows × 25N columns. Rows from one unit are tied to the display and rows on the other units are not used. The chip select signal also controls all the HLCD 0515 at the same time on Data In pins the different data (column data) is presented by data bus to control different columns. In the initialization mode all HLCD 0515 must be presented the same data on Data In pins by software. Alternatively, a common data line and individual chip selects could be used.

Theoretically any number of HLCD 0515 can be cascaded together as shown. In reality, it depends on the characteristics of the display and the application. In a similiar manner, one can utilize a number of HLCD 0515 to drive 16 rows x m column displays. For each 8 x 25 block, one HLCD 0515 is required as shown in Figure B

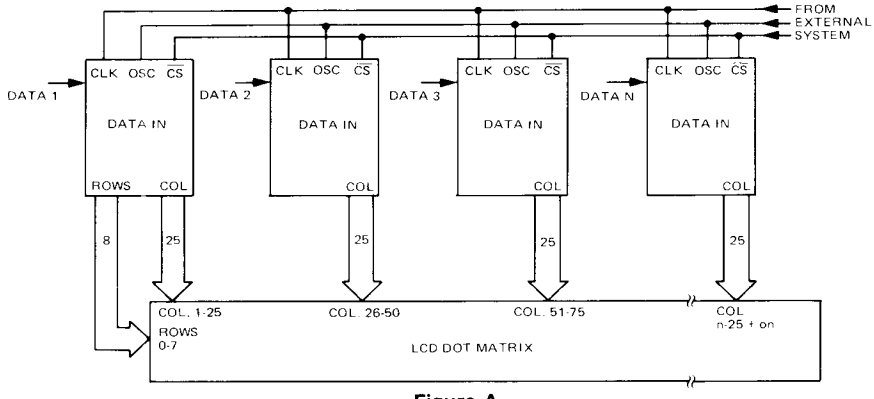


Figure A

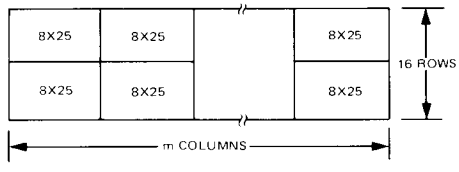


Figure B

SIGNAL DESCRIPTION

Row 0 — Row 7; Pin 1 — Pin 8 (Outputs): These eight outputs can be connected directly to the row pins (backplanes) of the display.

Col 1 — Col 25; Pin 9 — Pin 19, Pin 21 — Pin 34 (Outputs): These twenty five outputs can be connected directly to the column pins of the display.

GND Pin 20: Ground for display and display driver.

VDD; Pin 40: Most positive supply for the display and display driver.

Data Out; Pin 35 (Output): The Data Output pin produces data serially from the RAM buffer during the read buffer mode.

$\overline{CS}$; Pin 36 (Input): The chip select input enables all operating modes of HLCD 0515 when $\overline{CS}$ is low.

Data In; Pin 37: The data input pin is used for loading the RAM buffer data serially from an external system. Positive logic is used and a logic 1 makes a pixel visible.

Clock; Pin 38 (Input): Negative going edge on this pin clocks the data in or out, depending on the mode.

OSC; Pin 39 (Input): The timing for refresh waveforms for the LCD is determined by a capacitor connected to this pin. An external signal should be used to synchronize the oscillators while cascaded.

OSCILLATOR FREQUENCY

To determine the proper frequency of operation, one must consider:

1) the external frequency is divided by two on-board.
2) number of backplanes selected (rows), and
3) 30 Hz minimum no-flicker frequency.

The f is derived as:

$$f = \frac{1}{1\ XN\ X\ 30}$$

The external capacitor which will produce f is:

$$f = \frac{1}{50K \times C}$$

where the value of C is in microfarads

Example: 8 backplanes, $\frac{1}{2\ X\ 8\ X\ 30} = \frac{1}{50K\ X\ C}$, yields C = .01 microfarads

LCD DRIVER NOTES

1. RMS Drive Voltages — The On and Off RMS drive voltages supplied to each pixel by the HLCD 0515 depend on the number of backplanes, N, as follows:

$$V_{RMS}\ ON = \frac{V_{DD}}{4}\sqrt{\frac{N+15}{N}}$$

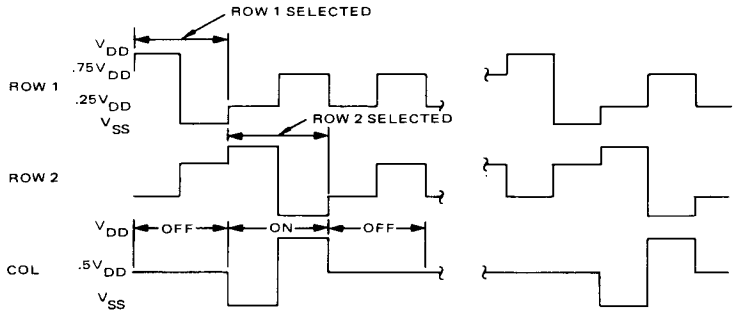
$$V_{RMS}\ OFF = \frac{V_{DD}}{4}\sqrt{\frac{N+3}{N}}$$

The HLCD 0515 generates on-chip all required voltages to drive a multiplexed LCD with the V/4 drive scheme. The V/4 scheme requires the following voltages be derived (when V_{DD} is the supply voltage):

V_{DD}
.75 V_{DD}
.5 V_{DD}
.25 V_{DD}
0

Note if the display requires a swing more negative than system ground, the V_{DD} is tied in common with system V_{DD} and the GND is taken sufficiently lower than system GND to provide the required swing. (The user must insure that the HLCD 0515's VIL spec is not violated and that VOL's can be read by the system.) Waveforms for the V/4 display drive scheme are shown below:

TYPICAL OUTPUT WAVEFORMS



2. Temperature Compensation — The HLCD 0515 can be used with displays requiring temperature compensation. The technique is to select a PTC (Positive Temp Compensation) thermistor with a temperature response which complements that of the display. The thermistor is inserted between the HLCD 0515's V_{SS} and the negative reference source.

HUGHES SOLID STATE PRODUCTS
HUGHES AIRCRAFT COMPANY
500 Superior Avenue Newport Beach CA 92663
Telephone (714) 759-2942 TWX 910-596-1374
In Europe: Hughes Solid State Products
Hughes Aircraft International Service Co
Schmaedel Str 22 8000 Munich West Germany
Telephone 49 89-834 7088 Telex 5213856 HSPD

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