

# E0C621A

## 4-bit Single Chip Microcomputer



- Core CPU Architecture
- 32kHz/455kHz Twin Clock Operation
- SVD Circuit/Analog Comparator
- Watchdog Timer

### ■ DESCRIPTION

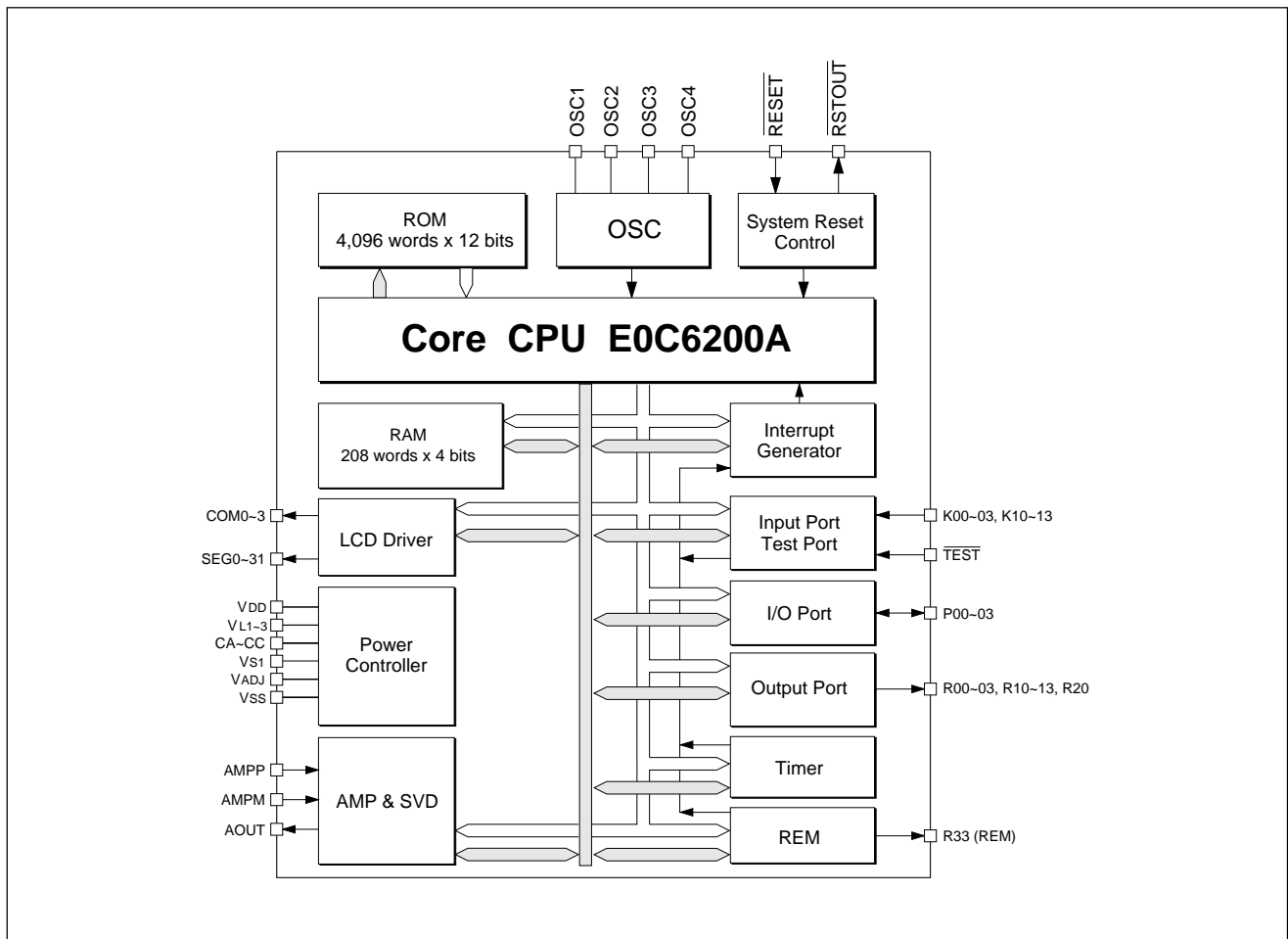
The E0C621A is a CMOS 4-bit microcomputer using an E0C6200A as its core processor. It contains ROM, RAM, LCD driver circuit, remote-control carrier output circuit, time base counter, analog comparator, watchdog timer and other functions on a single chip. The E0C621A provides an excellent solution for low-power system applications such as an infrared remote controller with clock function. One time PROM version is available.

### ■ FEATURES

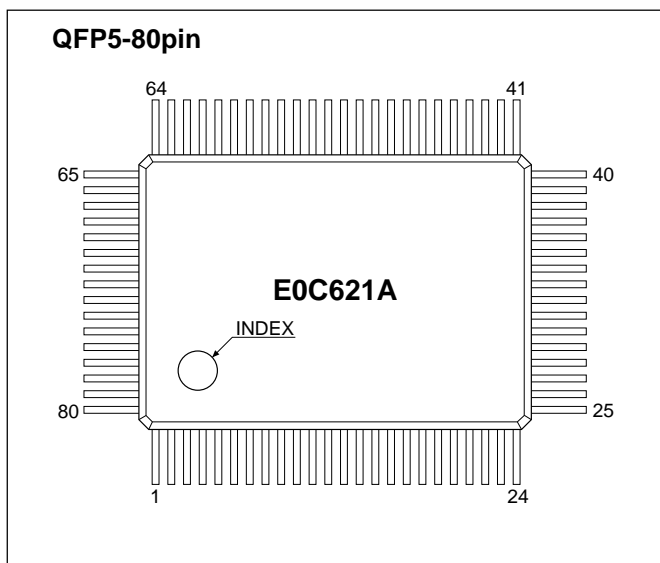
- CMOS LSI 4-bit parallel processing
- Twin clock ..... 32.768kHz (Typ.) Crystal  
455kHz (Typ.) CR or Ceramic oscillation circuit  
(selectable by mask option)
- Instruction set ..... 100 instructions
- Instruction cycle time ..... 32kHz clock mode : 153μsec, 214μsec or 366μsec  
455kHz clock mode : 11μsec, 15μsec or 26μsec
- ROM capacity ..... 4,096 × 12 bits
- RAM capacity ..... 208 × 4 bits
- Input port ..... 8 bits (pull-up resistors are available by mask option)
- Output port ..... 9 bits (clock, buzzer output is available by mask option)
- I/O port ..... 4 bits
- Remote control carrier (REM) ..... 1 bit (hardware timer or software timer is selectable by software)
- LCD driver ..... 32 segments × 3 commons or 32 segments × 4 commons  
(1/3 or 1/4 duty is selectable by mask option)
- Built-in LCD power supplies ..... Voltage regulator, voltage doubler and voltage tripler
- Built-in SVD circuit ..... 2.3V ± 0.1V (supply voltage detector) Criteria voltage
- Built-in amplifier ..... Operational amplifier for MOS input analog comparator
- Built-in watchdog timer (Mask option)
- Interrupts ..... External : Input interrupt 2 lines  
Internal : Timer interrupt (32Hz, 8Hz, 2Hz) 1 line (3ch.)  
REM interrupt 1 line
- Supply voltage ..... 3.0V (2.2V to 3.5V)
- Current consumption ..... HALT mode (32.768kHz) : 2μA (Typ.)  
OPERATING mode (455kHz) : 130μA (Typ.)
- Package ..... QFP5-80pin (plastic), QFP14-80pin (plastic)  
Die form

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## ■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG16	21	COM0	41	OSC4	61	K11
2	SEG15	22	CC	42	Vs1	62	K12
3	SEG14	23	CB	43	R00	63	K13
4	SEG13	24	CA	44	R01	64	TEST
5	SEG12	25	VL3	45	R02	65	N.C.
6	SEG11	26	VL2	46	R03	66	SEG31
7	SEG10	27	RESET	47	R10	67	SEG30
8	SEG9	28	VADJ	48	R11	68	SEG29
9	SEG8	29	VL1	49	R12	69	SEG28
10	SEG7	30	R33 (REM)	50	R13	70	SEG27
11	SEG6	31	RSTOUT	51	R20	71	SEG26
12	SEG5	32	AMPP	52	P00	72	SEG25
13	SEG4	33	AMPM	53	P01	73	SEG24
14	SEG3	34	AOUT	54	P02	74	SEG23
15	SEG2	35	VDD	55	P03	75	SEG22
16	SEG1	36	N.C.	56	K00	76	SEG21
17	SEG0	37	OSC1	57	K01	77	SEG20
18	COM3	38	OSC2	58	K02	78	SEG19
19	COM2	39	VSS	59	K03	79	SEG18
20	COM1	40	OSC3	60	K10	80	SEG17

N.C. = No Connection

## PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
VDD	35	I	Power source (+) terminal
VSS	39	I	Power source (-) terminal
VS1	42	-	Oscillation and internal logic system regulated voltage output terminal (approx. VDD-2.0 V)
VL1	29	-	LCD system regulated voltage output terminal (approx. VDD-VL)
VL2	26	-	LCD system booster output terminal (VDD-2VL)
VL3	25	-	LCD system booster output terminal (VDD-3VL)
VADJ	28	I	VL input adjustment terminal
CA-CC	22-24	-	Booster capacitor connecting terminal
OSC1	37	I	Crystal oscillation input terminal
OSC2	38	O	Crystal oscillation output terminal
OSC3	40	I	Ceramic or CR oscillation input terminal
OSC4	41	O	Ceramic or CR oscillation output terminal
K00-03, K10-13	56-63	I	Input terminal
P00-03	52-55	I/O	I/O terminal
R00-03, R10, R11	43-48	O	Output terminal
R12	49	O	Output terminal (DC, FOUT or BZ output may be selected by mask option)
R13	50	O	Output terminal (DC or BZ output may be selected by mask option)
R20	51	O	Output terminal
R33(REM)	30	O	Remote control carrier output terminal
AMPP	32	I	Analog comparator non-inverted input terminal
AMPM	33	I	Analog comparator inverted input terminal
AOUT	34	O	Analog comparator output terminal
SEG0-31	1-17, 66-80	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0-3	18-21	O	LCD common output terminal
RESET	27	I	Initial reset input terminal
TEST	64	I	Test input terminal
RSTOUT	31	O	Initial reset output terminal

## ABSOLUTE MAXIMUM RATINGS

(VDD=0V)

Rating	Symbol	Value	Unit
Supply voltage	VSS	-5.2 to 0.5	V
Input voltage	VI	VSS -0.3 to 0.3	V
	VIosc	VS1 -0.3 to 0.3	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature and time	Tsol	260°C, 10sec (at lead)	-
Power dissipation	Pd	250	mW

## RECOMMENDED OPERATING CONDITIONS

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	VSS	VDD = 0 V	-3.5	-3.0	-2.2	V
Oscillation frequency	fosc1		-	32.768	-	kHz
	fosc3	duty : 50 ± 5%	50	455	600	kHz
Power supply voltage for LCD driver	VL1		-1.6	-1.03	-	V
CR oscillation external resistor	RCR		100	140	500	kΩ

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## ■ ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub>=0V, V<sub>SS</sub>=-2.2 to -3.5V, V<sub>L3</sub>=-3.0V, T<sub>a</sub>=-20 to 70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V <sub>IH1</sub>		K00–K03, K10–K13, P00–P03	0.2V <sub>SS</sub>		0	V
Low level input voltage (1)	V <sub>IL1</sub>		K00–K03, K10–K13, P00–P03	V <sub>SS</sub>		0.8V <sub>SS</sub>	V
High level input voltage (2)	V <sub>IH2</sub>		RESET	0.1V <sub>SS</sub>		0	V
Low level input voltage (2)	V <sub>IL2</sub>		RESET	V <sub>SS</sub>		0.9V <sub>SS</sub>	V
High level input current	I <sub>IH</sub>	V <sub>IH</sub> = V <sub>DD</sub>				1	μA
Low level input current	I <sub>IL1</sub>	V <sub>IL1</sub> = V <sub>SS</sub>	No pull up, K00–K03, K10–K13	-1			μA
	I <sub>IL2</sub>	V <sub>IL2</sub> = V <sub>SS</sub>	Pull up, K00–K03, K10–K13	-5		-0.35	μA
	I <sub>IL3</sub>	V <sub>IL3</sub> = V <sub>SS</sub>	RESET pin	-5		-0.35	μA
	I <sub>IL4</sub>	V <sub>IL4</sub> = 0.2V <sub>SS</sub>	Pull up, K00–K03, K10–K13	-30			μA
	I <sub>IL5</sub>	V <sub>IL5</sub> = 0.2V <sub>SS</sub>	RESET pin	-40			μA
	I <sub>IL6</sub>	V <sub>IL6</sub> = V <sub>SS</sub>	P00–P03 *	-15		-2	μA
High level output current (1)	I <sub>OH1</sub>	V <sub>OH1</sub> = 0.1V <sub>SS</sub>	R00–R03, R10–R13, RSTOUT			-250	μA
Low level output current (1)	I <sub>OL1</sub>	V <sub>OL1</sub> = 0.9V <sub>SS</sub>	R00–R03, R10–R13, RSTOUT	1.0			mA
High level output current (2)	I <sub>OH2</sub>	V <sub>OH2</sub> = 0.1V <sub>SS</sub>	R20			-1.8	mA
Low level output current (2)	I <sub>OL2</sub>	V <sub>OL2</sub> = 0.9V <sub>SS</sub>	R20	1.0			mA
High level output current (3)	I <sub>OH3</sub>	V <sub>OH3</sub> = 0.1V <sub>SS</sub>	P00–P03			-250	μA
Low level output current (3)	I <sub>OL3</sub>	V <sub>OL3</sub> = 0.9V <sub>SS</sub>	P00–P03	1.0			mA
High level output current (4)	I <sub>OH4</sub>	V <sub>OH4</sub> = 0.1V <sub>SS</sub>	R33 (REM)			-1.8	mA
Low level output current (4)	I <sub>OL4</sub>	V <sub>OL4</sub> = 0.9V <sub>SS</sub>	R33 (REM)	1.0			mA
Common output current	I <sub>OH5</sub>	V <sub>OH5</sub> = -0.05V	COM0–COM3			-3.0	μA
	I <sub>OL5</sub>	V <sub>OL5</sub> = V <sub>L3</sub> + 0.05V		3.0			μA
Segment output current (in LCD output mode)	I <sub>OH6</sub>	V <sub>OH6</sub> = -0.05V	SEG0–SEG31			-3.0	μA
	I <sub>OL6</sub>	V <sub>OL6</sub> = V <sub>L3</sub> + 0.05V		3.0			μA
Segment output current (in DC output mode)	I <sub>OH7</sub>	V <sub>OH7</sub> = 0.1V <sub>SS</sub>	SEG0–SEG31			-50	μA
	I <sub>OL7</sub>	V <sub>OL7</sub> = 0.9V <sub>SS</sub>		70			μA
Internal voltage	V <sub>L1</sub>	V <sub>ADJ</sub> = V <sub>L1</sub> , I <sub>L1</sub> = 5 μA		-1.11	-1.03	-0.95	V
	V <sub>L2</sub>	1 MΩ load connected between V <sub>DD</sub> and V <sub>L2</sub>		2V <sub>L1</sub>		2V <sub>L1</sub> + 0.1	V
	V <sub>L3</sub>	1 MΩ load connected between V <sub>DD</sub> and V <sub>L3</sub>		3V <sub>L1</sub>		3V <sub>L1</sub> + 0.3	V
SVD voltage	V <sub>SVD</sub>			-2.4	-2.3	-2.2	V
Current consumption	I <sub>OP</sub>	HALT mode	OSCC = 0, V <sub>ADJ</sub> = V <sub>L1</sub> , No panel load		2	5	μA
		OSC1 mode *1	OSCC = 0, V <sub>ADJ</sub> = V <sub>L1</sub> , No panel load		9	18	μA
		OSC3 mode *1, *2	V <sub>ADJ</sub> = V <sub>L1</sub> , No panel load		130	250	μA

\* Only at read cycle using internal program.

\*1 The SVD circuit and analog comparator are in the OFF status.

\*2 OSC3 mode: Ceramic oscillation (455 kHz) or CR oscillation (R = 140 kΩ)

## ■ OSCILLATION CHARACTERISTICS

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

### ● OSC1 (Crystal)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ , Crystal: C-002R ( $C_I=35k\Omega$ ),  $C_G=25pF$ ,  $C_D$ =built-in,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	$t_{sta}$	$V_{SS}=-2.2$ to $-3.5V$	–	–	5	Sec
Built-in capacitance (drain)	$C_D$	Package as assembled	–	25	–	pF
		Bare chip	–	24	–	pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-3.5V$	–	–	5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10	–	10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	40	–	–	ppm
Harmonic oscillation start voltage	$V_{hho}$	$C_G=5pF$	–	–	-3.5	V
Permitted leak resistance	$R_{leak}$	Between OSC1 and other pins	200	–	–	M $\Omega$

### ● OSC3 (CR oscillation)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ ,  $R_{CR}=140k\Omega$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	$f_{osc3}$		–	280	–	kHz
Oscillation start voltage	$V_{sta}$	( $V_{SS}$ )	-2.2	–	–	V
Oscillation start time	$t_{sta}$	$V_{SS}=-2.2$ to $-3.5V$	–	3	–	mS
Oscillation stop voltage	$V_{stp}$	( $V_{SS}$ )	-2.2	–	–	V

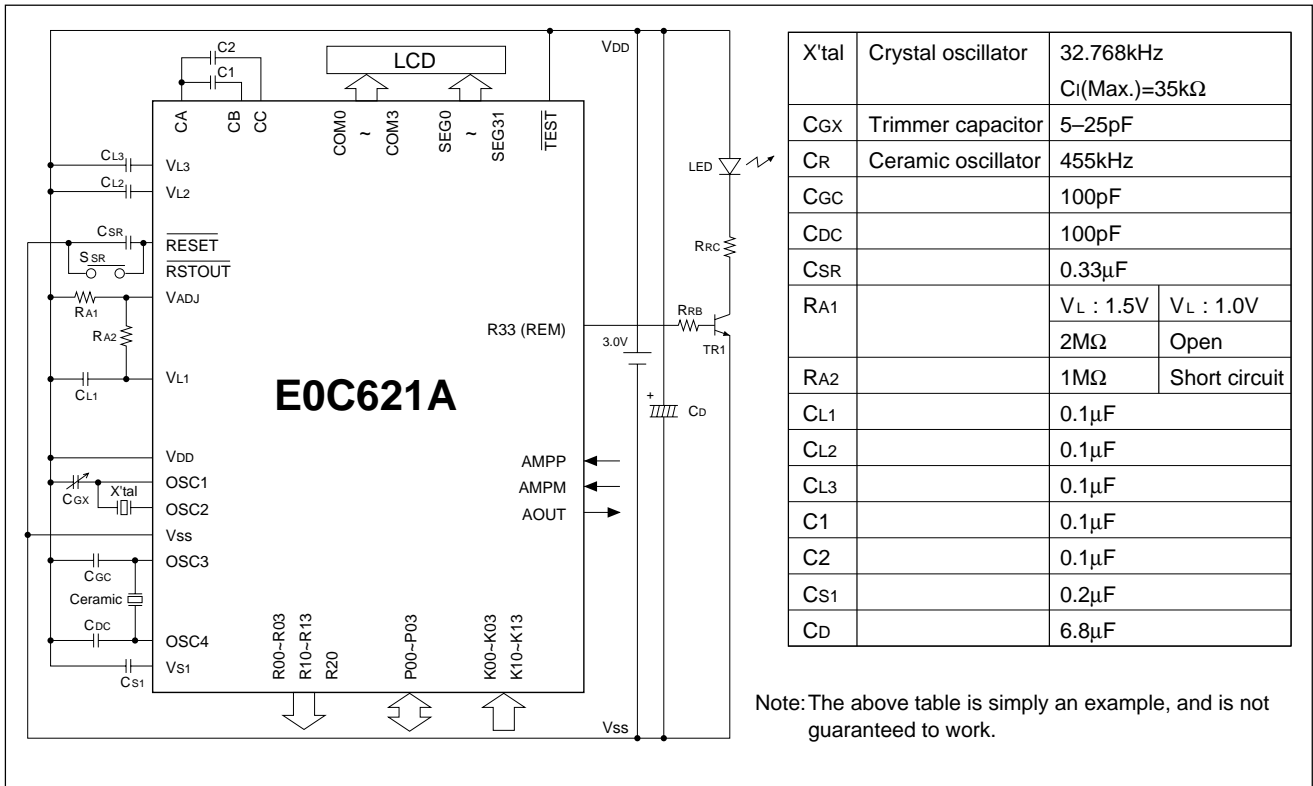
### ● OSC3 (Ceramic)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ , Ceramic: CSB455E (Murata Mfg. Co.),  $C_{GC}=C_{DC}=100pF$ ,  $T_a=25^\circ C$ )

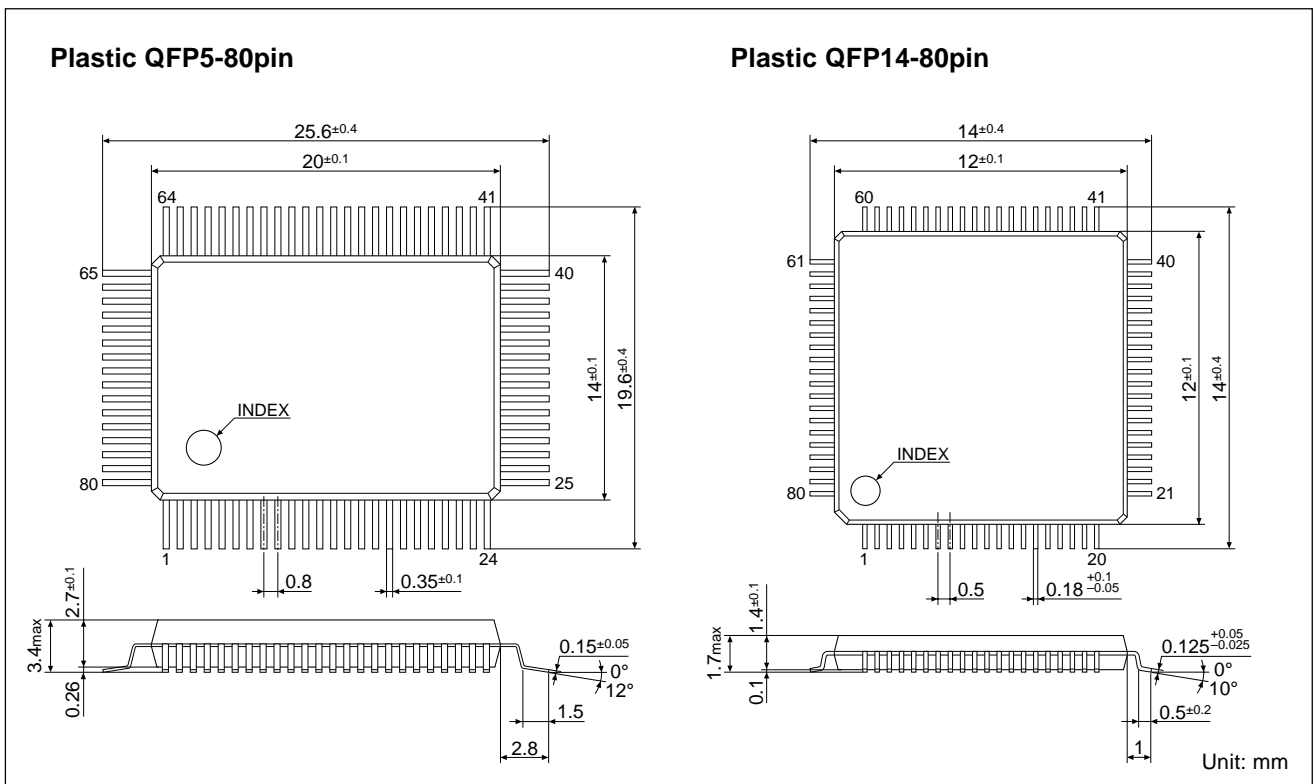
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	$V_{sta}$	( $V_{SS}$ )	-2.2	–	–	V
Oscillation start time	$t_{sta}$	$V_{SS}=-2.2$ to $-3.5V$	–	3	–	mS
Oscillation stop voltage	$V_{stp}$	( $V_{SS}$ )	-2.2	–	–	V

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## ■ BASIC EXTERNAL CONNECTION DIAGRAM



## ■ PACKAGE DIMENSIONS



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