CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7B153
CY7B154

Expandable 65,536 x 4 Static R/W RAM

Features

- **High speed**
  - **— 12 ns t_{AA}**
- **Easy memory expansion with: $\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ (7B154 only), CE_4, CE_5 (7B153 only), and $\overline{OE}$**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **— 743 mW**
- **Low standby power**
  - **— 275 mW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7B153 and CY7B154 are high-performance BiCMOS static RAMs organized as 65,536 words by 4 bits. Easy memory expansion is provided by an active LOW output enable ($\overline{OE}$) and four chip enables for each part: $\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ (CY7B154 only), CE_4, and CE_5 (CY7B153 only). The active HIGH and active LOW chip enables provide on-chip address decoding, eliminating the need for external decoder logic. Both devices have an automatic power-down feature, reducing the power consumption by more than 70% when deselected.

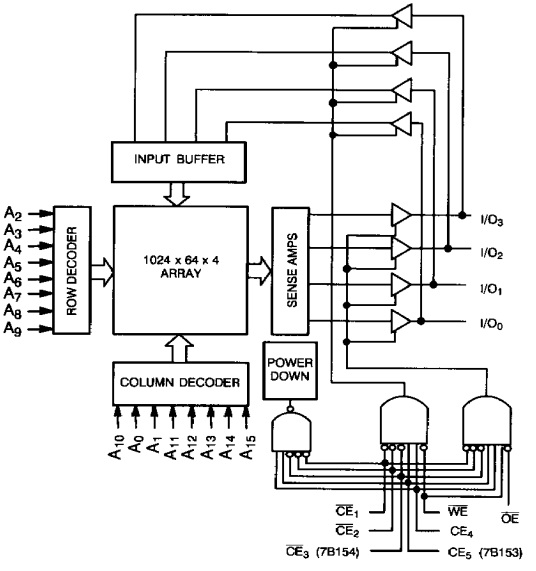
An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_{1,2,3}$ and $\overline{WE}$ inputs are both LOW and $CE_{4,5}$ are HIGH, data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip enable ($\overline{CE}_{1,2,3}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) and chip enable ($CE_{4,5}$) are HIGH. Under these conditions, the contents of the location specified on the address pins is present on the four data input/output pins.

The four input output pins are in a high-impedance state when the device is deselected (any of: $\overline{CE}_{1\ 2,3}$ HIGH or $CE_{4,5}$ LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{WE}$ and $\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH).

The CY7B153 and CY7B154 are available in leadless chip carriers and space-saving 300-mil-wide DIPs and SOJs.

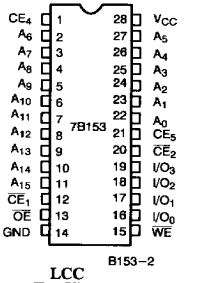
Logic Block Diagram



B153-1

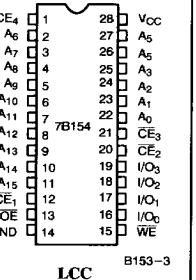
Pin Configurations

DIP/SOJ Top View



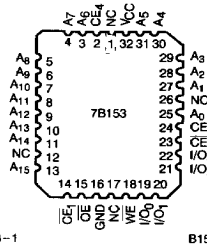
B153-2

DIP/SOJ Top View



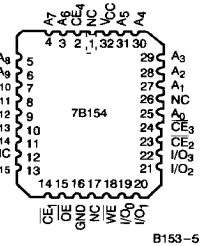
B153-3

LCC Top View



B153-4

LCC Top View



B153-5

Selection Guide

		7B153–12 7B154–12	7B153–15 7B154–15	7B153–20 7B154–20
Maximum Access Time (ns)		12	15	20
Maximum Operating Current (mA)	Commercial	135	135	135
	Military		145	145
Maximum Standby Current (mA)	Commercial	50	50	50
	Military		60	60

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage on V_{CC} Relative to GND[1] . – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to + 7.0V

DC Input Voltage[1] ..... – 0.5V to + 7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics[3] Over the Operating Range

Parameters	Description	Test Conditions		7B153–12 7B154–12 Min.	7B153–12 7B154–12 Max.	7B153–15, 20 7B154–15, 20 Min.	7B153–15, 20 7B154–15, 20 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		135		135	mA
			Mil				145	
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $CE_{1,2,3}$ ≥ V_{IH}, $CE_{4,5}$ ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		50	mA
			Mil				60	
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $CE_{1,2,3}$ ≥ V_{CC} – 0.3V, $CE_{4,5}$ ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		30		30	mA
			Mil				40	

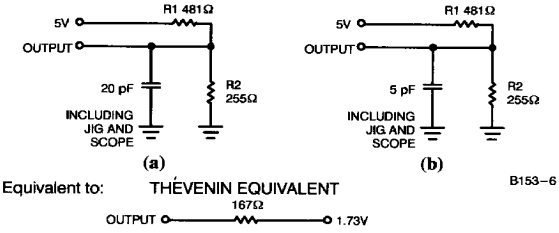
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

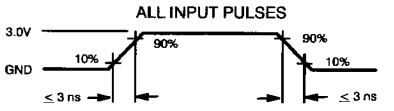
Notes:

1. $V_{IL\,(min.)}$ = – 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



B153–6



B153–7

Switching Characteristics[3,6] Over the Operating Range

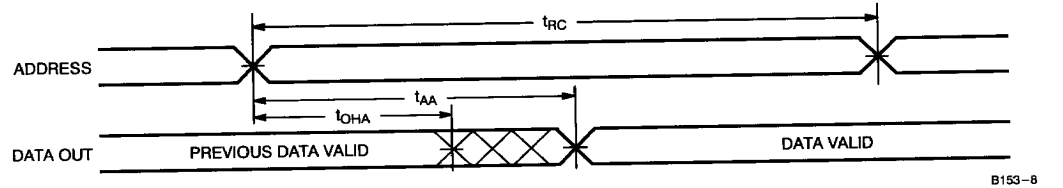
Parameters	Description	7B153–12 7B154–12		7B153–15 7B154–15		7B153–20 7B153–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		10		12	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	2		2		2		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		7		8		10	ns
t_{LZCE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Low Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE}_{1,2,3}$, HIGH or $CE_{4,5}$ LOW to High Z[7,8]		7		8		10	ns
t_{PU}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Power-Up		0		0		0	ns
t_{PD}	$\overline{CE}_{1,2,3}$, HIGH or $CE_{4,5}$ LOW to Power-Down		12		15		20	ns
WRITE CYCLE[9,10]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Write End	9		10		15		ns
t_{AW}	Address Set-Up to Write End	9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	9		10		15		ns
t_{SD}	Data Set-Up to Write End	7		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7,8]		7		7		10	ns

Notes:

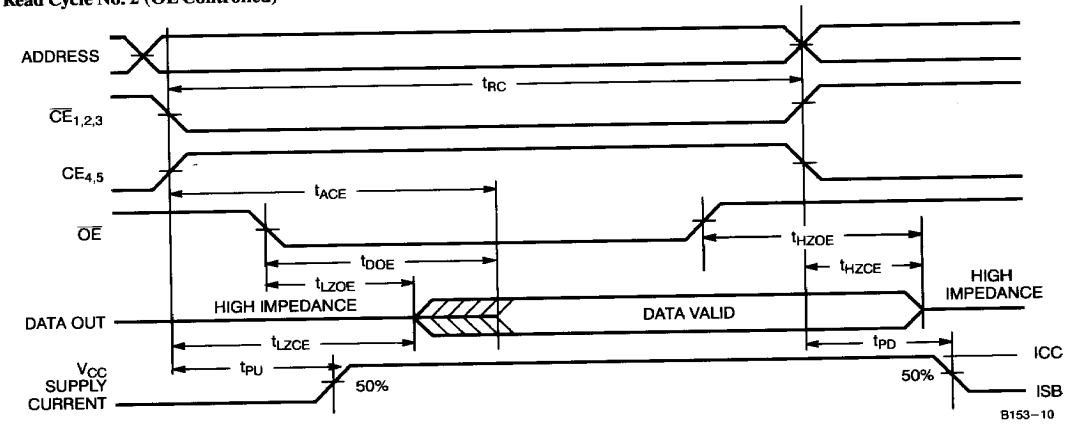
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 20-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_{1,2,3}$ LOW, $CE_{4,5}$ HIGH, and $\overline{WE}$ LOW. All signals must be appropriately set to initiate a write and any of these signals can terminate a write. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

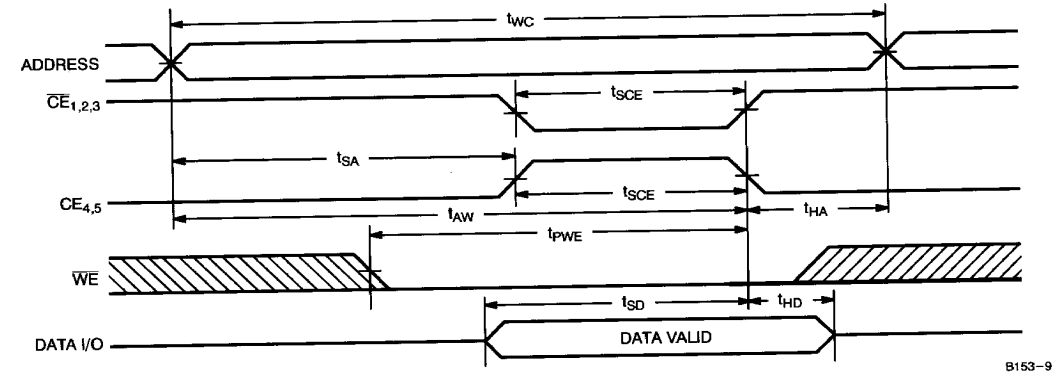
Read Cycle No. 1[11,12]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[12,13]



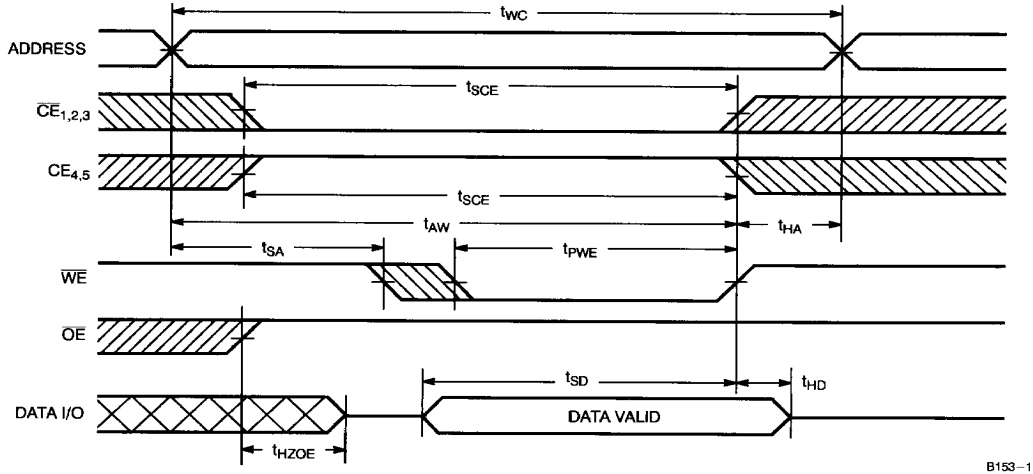
Write Cycle No. 1 ($\overline{CE_1}$, $\overline{CE_2}$, $\overline{CE_3}$, CE_4, or CE_5 Controlled)[14,15]



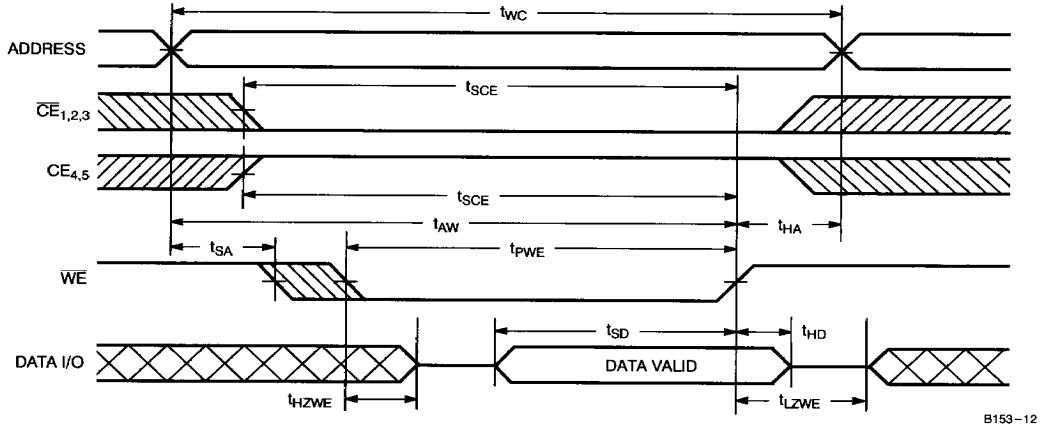
Notes:
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}_{1,2,3} = V_{IL}$, $CE_{4,5} = V_{IH}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}_{1,2,3}$ transition LOW and $CE_{4,5}$ transition HIGH.
14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If any of $\overline{CE}_{1,2,3}$ go HIGH or $CE_{4,5}$ goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[14,15]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10,15]



CY7B153 Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	CE_4	CE_5	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_3$	Mode	Power
H	X	X	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	H	X	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	L	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	H	L	H	Data Out	Read	Active (I_{CC})
L	L	H	H	X	L	Data In	Write	Active (I_{CC})
L	L	H	H	H	H	High Z	Selected	Active (I_{CC})

CY7B154 Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$	CE_4	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_3$	Mode	Power
H	X	X	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	H	X	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	L	H	L	H	Data Out	Read	Active (I_{CC})
L	L	L	H	X	L	Data In	Write	Active (I_{CC})
L	L	L	H	H	H	High Z	Selected	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B153–12PC	P21	Commercial
	CY7B153–12DC	D22	
	CY7B153–12LC	L55	
	CY7B153–12VC	V21	
15	CY7B153–15PC	P21	Commercial
	CY7B153–15DC	D22	
	CY7B153–15LC	L55	
	CY7B153–15VC	V21	
	CY7B153–15DMB	D22	Military
	CY7B153–15LMB	L55	
20	CY7B153–20PC	P21	Commercial
	CY7B153–20DC	D22	
	CY7B153–20LC	L55	
	CY7B153–20VC	V21	
	CY7B153–20DMB	D22	Military
	CY7B153–20LMB	L55	

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B154–12PC	P21	Commercial
	CY7B154–12DC	D22	
	CY7B154–12LC	L55	
	CY7B154–12VC	V21	
15	CY7B154–15PC	P21	Commercial
	CY7B154–15DC	D22	
	CY7B154–15LC	L55	
	CY7B154–15VC	V21	
	CY7B154–15DMB	D22	Military
	CY7B154–15LMB	L55	
20	CY7B154–20PC	P21	Commercial
	CY7B154–20DC	D22	
	CY7B154–20LC	L55	
	CY7B154–20VC	V21	
	CY7B154–20DMB	D22	Military
	CY7B154–20LMB	L55	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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