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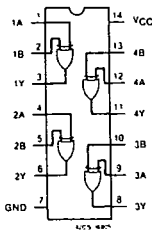
CD54/74HC86 CD54/74HCT86

T-43-21-00

High-Speed CMOS Logic

HARRIS SEMICONDUCTOR

27E D ■ 4302271 0017532 2 ■ HAS



FUNCTIONAL DIAGRAM AND
TERMINAL ASSIGNMENT

Quad 2 - Input EXCLUSIVE - OR Gate

Type Features:

- Four independent EXCLUSIVE - OR gates
- Buffered inputs and outputs

Applications:

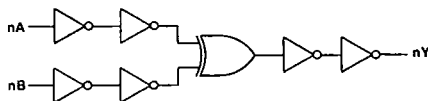
- Logical comparators
- Parity generators and checkers
- Adders/Subtractors

The RCA CD54/74HC86 and CD54/74HCT86 contain four independent EXCLUSIVE-OR gates in one package. They provide the system designer with a means for implementation of the EXCLUSIVE-OR function.

The CD54HC/HCT86 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT86 are supplied in 14-lead plastic dual-in-line packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Sigetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}
@ $V_{CC} = 5$ V
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.
CMOS Input Compatibility
 $I_1 \leq 1 \mu A$ @ V_{OL} , V_{OH}



92CS-38429

Fig. 1 - Logic diagram each gate.

TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level.
L = LOW voltage level.

CD54/74HC86 CD54/74HCT86

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}):	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg}):	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm)	
with solder contacting lead tips only	$+300^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_i , V_o	0	V_{CC}	V
Operating Temperature T_A :			
CD74 Types	-40	+85	$^\circ\text{C}$
CD54 Types	-55	+125	$^\circ\text{C}$
Input Rise and Fall Times, t_r , t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC86 CD54/74HCT86

STATIC ELECTRICAL CHARACTERISTICS

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CHARACTERISTICS	CD74HC86/CD54HC86										CD74HCT86/CD54HCT86										UNITS	
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE				
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C				
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max			
High-Level Input Voltage	V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5		2	—	—	2	—	2	—	V
				4.5	3.15	—	—	3.15	—	3.15	—	—	to									
				6	4.2	—	—	4.2	—	4.2	—	—	5.5									
Low-Level Input Voltage	V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5				0.8	—	0.8	—	0.8	V
				4.5	—	—	1.35	—	1.35	—	1.35	—	to									
				6	—	—	1.8	—	1.8	—	1.8	—	5.5									
High-Level Output Voltage	V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
CMOS Loads				4.5	4.4	—	—	4.4	—	4.4	—											
				6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V _{IL} or V _{IH}											V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
				-4	4.5	3.98	—	—	3.84	—	3.7	—										
				-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage	V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V	
CMOS Loads				4.5	—	—	0.1	—	0.1	—	0.1											
				6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V _{IL} or V _{IH}											V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V	
				4	4.5	—	—	0.26	—	0.33	—	0.4										
				5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current	I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current	I _{CC}	V _{CC} or Gnd	0	6	—	—	2	—	20	—	40	V _{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA	
Additional Quiescent Device Current per Input Pin: 1 Unit Load	ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA	

*For dual-supply systems theoretical worst case ($V_i = 2.4$ V, $V_{cc} = 5.5$ V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
All Inputs	1

* Unit load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC86

CD54/74HCT86

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES		UNITS
			54/74HC	54/74HCT	
Propagation Delay, Any Input	15	t_{PLH} t_{PHL}	9	13	ns
Power Dissipation Capacitance*	—	C_{PD}	22	27	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:

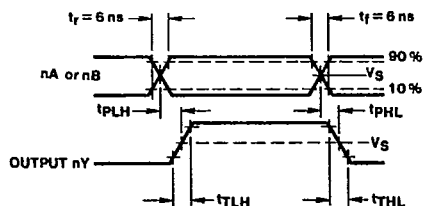
f_i = input frequency.

C_L = output load capacitance.

V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, nA, nB to nY	t _{PLH}	2		120		—		150		—		180		—	ns
	t _{PHL}	4.5		24		32		30		40		36		48	
		6		20		—		26		—		31		—	
Output Transition Time	t _{TLH}	2		75		—		95		—		110		—	ns
	t _{THL}	4.5		15		15		19		19		22		22	
		6		13		—		16		—		19		—	
Input Capacitance	C _i		—	10	—	10	—	10	—	10	—	10	—	10	pF



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	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.