
Main Features

- High Sensitivity and High SNR Performance 2/3" CMOS Sensor
- Total Resolution of 2.5M (with 5 μ m Square Pixels)
- High Data Rate: 150 Mpixels/s Provides 60 Frame/s at 2M Resolution (for 2M60)
- Camera Link[®] Data Format (Base Configuration - 2 Channels)
- Flexible and Easy to Operate via Serial Communication Control
 - Gain: 0 dB to 18 dB in 3 dB Steps
 - Bit Depth: 8, 10 or 12-bit Data
 - Contrast Expansion
 - Shutter Time Programmable
 - Trigger Mode: Free-run or External Trigger Mode
 - Programmable ROI
 - Test Pattern
- Column FPN Correction
- Programmable Look-up Table
- Single Power Supply: DC 12V to 24V Provided on Hirose-6 Connector
- Input TTL Trigger Signal and Output TTL Shutter Signal on Hirose-5 Connector
- Compact Design: 44 x 44 x 45 mm (w, h, l)
- C-mount Adapter
- High Reliability - CE and FCC Compliant

Product Description

This camera features an outstanding sensitivity and dynamic range even at maximal speeds. The ROI allows to increase the frame rate (for instance, 157 fps in VGA format 2M60). ATMOS[™] cameras are based on a rolling shutter CMOS sensor.

The configuration interface provides access to advanced functions (contrast expansion, image calibration, LUT). The versatile and compact mechanical housing enables you to implement various configurations.

These features combined with a compelling price, make ATMOS an attractive alternative for demanding users of megapixel cameras.

Applications

High-speed, dynamic range performance and reliability of this camera make it suitable for machine vision, especially:

- Material Inspection (e.g. glass, IC, PCB)
- Robot Guidance
- Metrology

and various applications like:

- Microscopy
- Surveillance Demanding Tasks



Camera Link[®] Areascan Cameras

ATMOS[™] 2M60
ATMOS[™] 2M30

Preliminary





1. Typical Performances

Table 1-1. Camera Typical Performances

Sensor Characteristics at Maximum Pixel Rate			
	2M60	2M30	Unit
Resolution H × V	2096 × 1184	2096 × 1184	Pixels
Pixel size (square)	5 × 5	5 × 5	μm
Maximum frame rate	48	24	Hz
Pixel rate	150	75	MHz
Camera Performances			
Bit depth	8, 10 or 12		Bits
Spectral range	350–1000		nm
Linearity	±2% in 5% and 95% of FSR		
PRNU	1.5% rms		
FPN	0.1% rms		
Peak Response @ G = 0	33 ⁽¹⁾		LSB/nJ/cm ²
Output RMS Noise	< 3 LSB rms		dB
Dynamic range	> 62.5		
Conversion factor	11		e ⁻ /LSB
Dark Current	1500		e ⁻ /s
Over Illumination Behavior	75 Esat		
Mechanical and Electrical Interface			
Size (w × h × l)	44 × 44 × 45		mm
Weight	115		g
Lens Mount	C-mount		
Sensor Alignment	$\Delta x, y = \pm 250$ $\Delta z = \pm 150$ $\Delta \theta_{xy} = \pm 0.7$ $\Delta \text{tilt}_z = 0\text{-}200$		μm μm degree μm
Power supply	single 12 to 24		VDC
Power consumption	< 3		W
Operating temperature	0 to 55 (non-condensing)		°C
Storage temperature	-40 to 70		°C

Note: 1. Measured with light source 3200°K and BG38 IR cut-off filter 2 mm thickness.

Figure 1-1. Responsivity Diagram

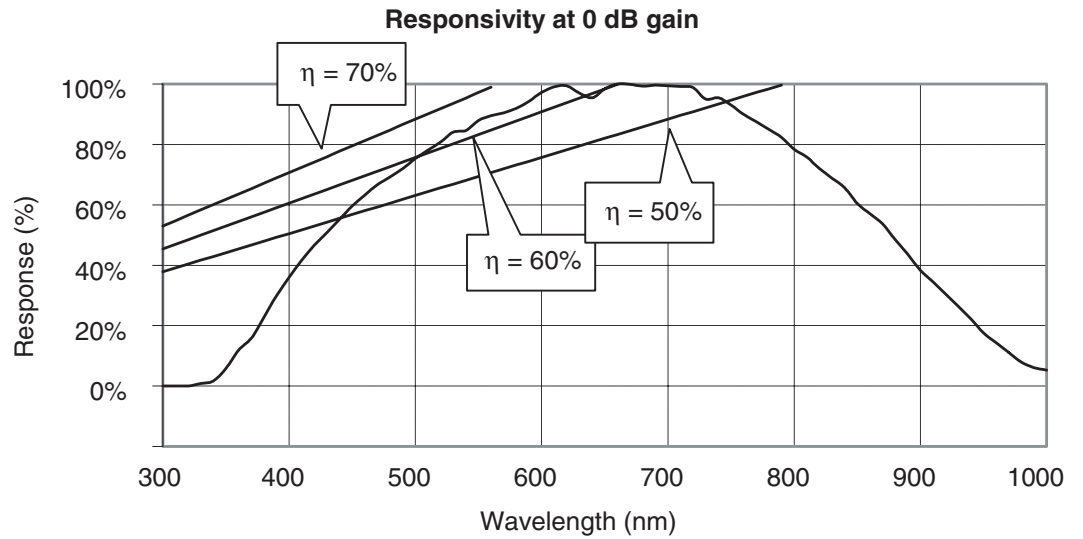
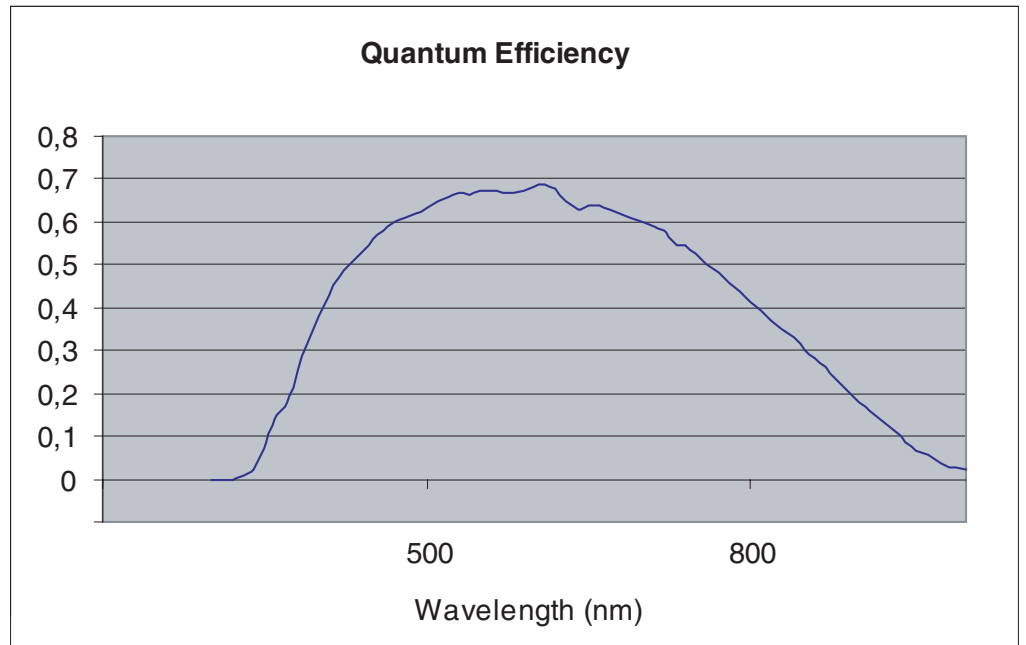


Figure 1-2. Quantum Efficiency





2. Standard Conformity

The cameras have been tested in the following conditions:

- Camera with complete Atmel housing
- Shielded power supply cable
- Camera Link data transfer cable ref. 14B26-SZLB-500-OLC (3M™)
- Linear AC-DC power supply

Atmel recommends using the same configuration to ensure compliance with the following standards.

2.1 CE Conformity

The ATMOS cameras comply with the European directive 89/336/CEE (EN55022 A/CISPR22 A, EN55024, EN61000-6-2).

2.2 FCC conformity

ATMOS Cameras comply with Part 15 of FCC rules. Operation is subject to the following two conditions:

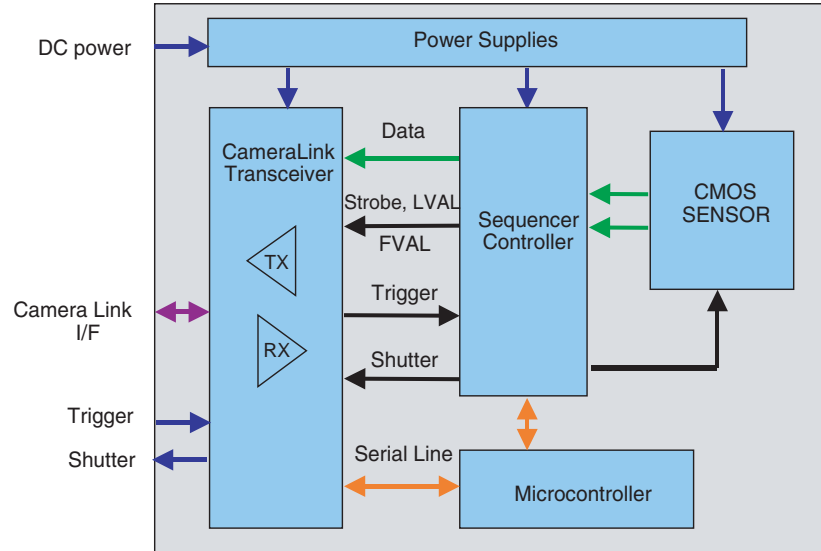
1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

3. Camera Description

Figure 3-1. Camera Synoptic



The camera is based on a single tap CMOS sensor which delivers a 12-bit digital video signal at its output. An FPGA has been implemented for image processing (FPN column correction, conversion LUT, contrast expansion). The camera is powered by a single DC power supply from 12V to 24V. The functional interface (data and control) is provided with the Camera Link interface. The camera uses the base configuration of the Camera Link standard.

Note: DVAL permanently tied to 1 (high) level.

Data is delivered on two channels. The data format configuration might be in 12-bit, 10-bit, or 8-bit. It is possible to use external triggers with the camera (CC1 signal or TTL_IO trigger input) in different trigger modes see ["Synchronization Modes" on page 6](#) The camera configuration and settings are done via the Camera Link serial communication. This interface is used for:

- Gain and offset setting
- Data output format
- Synchronization modes: free-run or external trigger modes
- Shutter time
- Test pattern generation
- Upload and download of correction data (FPN column correction, LUT)

4. Timing

4.1 Synchronization Modes

The camera operates in rolling shutter mode.

4.1.1 Optimal Use of the Rolling Shutter

As shown in the following timing diagrams, [Figure 4-1](#), exposure does not happen at the same time for all lines. When using the camera with a strobe light or a shutter element all the lines are exposed during the same time and no image distortion is visible when capturing fast moving objects.

The integration time for each line is: readout (+ programmable shutter time, when used). A shutter signal is provided to strobe a light source or to drive a shutter element. You can set the camera to operate in one of the following synchronization modes: periodic, triggered, triggered without full reset and ITC. See register Mode Control @ 204H, Internal Register Mapping on [page 16](#).

4.1.2 Free-run Mode (or Periodic Mode)

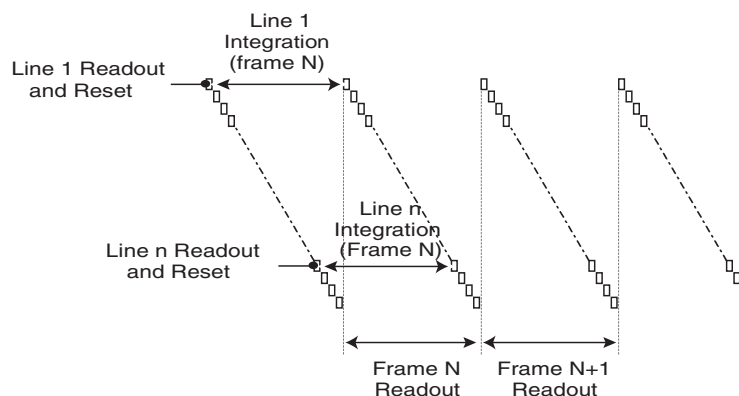
Principle: The camera operates in periodic mode.

The period is defined by readout time (+ programmable shutter time, when used). Valid data is forwarded to the Camera Link interface during the next frame readout starting with the first line.

If shutter time is set to 0:

The frame N is readout while the first line integrates for frame N+1. As soon as the frame N readout has ended starts the readout of frame N + 1.

Figure 4-1. Free-run Mode Chronogram



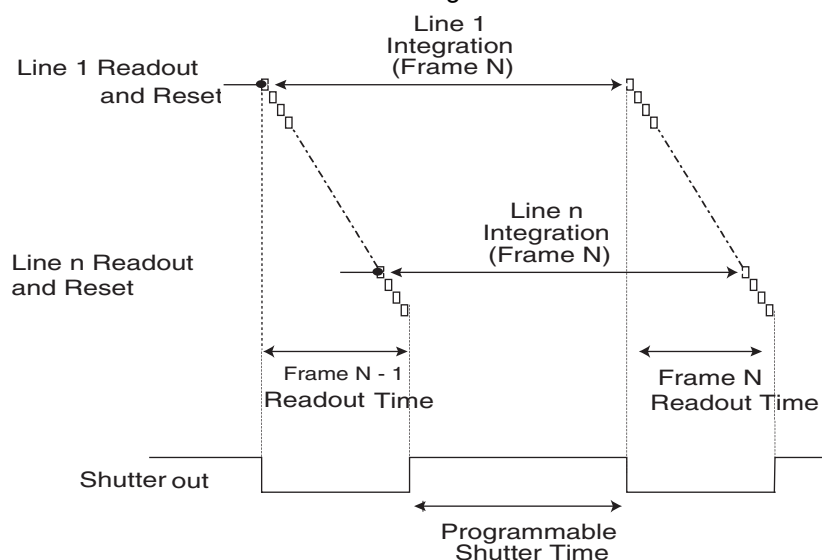
If shutter time is set to > 0:

Readout is suspended between two consecutive frame readout and shutter output signal is activated (programmable polarity) for a time configurable within 0 to Tsh range by step of T1.

Table 4-1. Shutter Time Values at Free-run Mode

Label	Description	2M60	2M30
Tsh	Maximum shutter time (ms)	655	1310
T1	Step duration (µs)	10	20

Figure 4-2. Free-run Mode and Shutter Chronogram



The maximum frame rate of 48 frame/s for the 2M60 camera (or 24 frame/s for the 2M30 camera) is given in this mode with a shutter time set to 0.

See register Aperture Shutter Time @ 246H, Internal Register Mapping on [page 16](#).

4.1.3 Triggered Mode

Principle: An external trigger starts the reset of the sensor, then snap and readout of a frame, the integration time is defined by readout time (+ programmable shutter time, when used).

The trigger event initiates the following sequence:

- Stop of readout frame in progress and reset of readout pointer to line 1
- Readout of previous dummy frame and integration start of the frame N. The readout data of previous frame is not forwarded on Camera Link interface (FVAL inactive)
- Shutter output signal is activated during a time programmable within 0 to Tsh range by step of T1

- Readout of frame N. The readout data is forwarded to the Camera Link interface (FVAL active) starting with the first line
- Readout of dummy frames (to prevent against large dark current integration) while the camera waits for the next trigger event

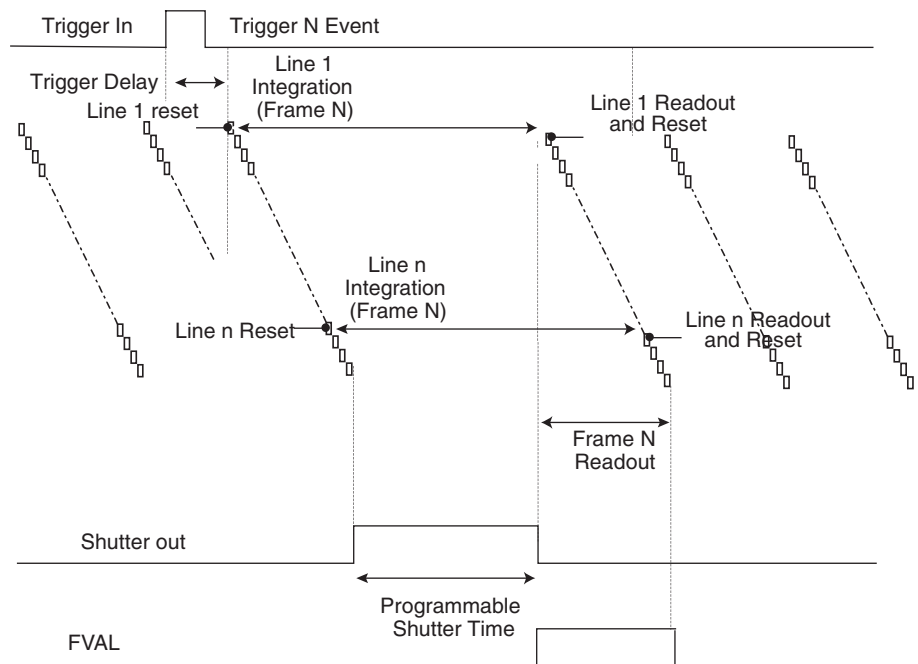
The trigger delay is a few μs . The minimum pulse duration is 1 μs . The edge of trigger is programmable. The source of trigger is selectable between Camera Link CC1 signal and TTL/IO trigger input. The period is defined by readout time + programmable shutter time + readout time + wait. Therefore the minimum period is $2 \times$ readout time.

See register Aperture Shutter Time @ 246H, Internal Register Mapping on [page 16](#).

Table 4-2. Shutter Time Values at Triggered Mode

Label	Description	2M60	2M30
Tsh	Maximum shutter time (ms)	655	1310
T1	Step duration (μs)	10	20

Figure 4-3. Triggered Mode Chronogram



4.1.4 Triggered Mode without Full Reset

Principle: An external trigger starts the snap and readout of a frame, without resetting the sensor. The integration time is defined by readout time (+ programmable shutter time, when used).

The trigger event initiates the following sequence:

- Stop of readout frame in progress and reset of readout pointer to line 1
- Shutter output signal is activated during a time programmable within 0 to Tsh range by step of T1

- Readout of frame N. The readout data is forwarded to the Camera Link interface (FVAL active) starting with the first line
- Readout of dummy frames (to prevent against large dark current integration) while the camera waits for the next trigger event

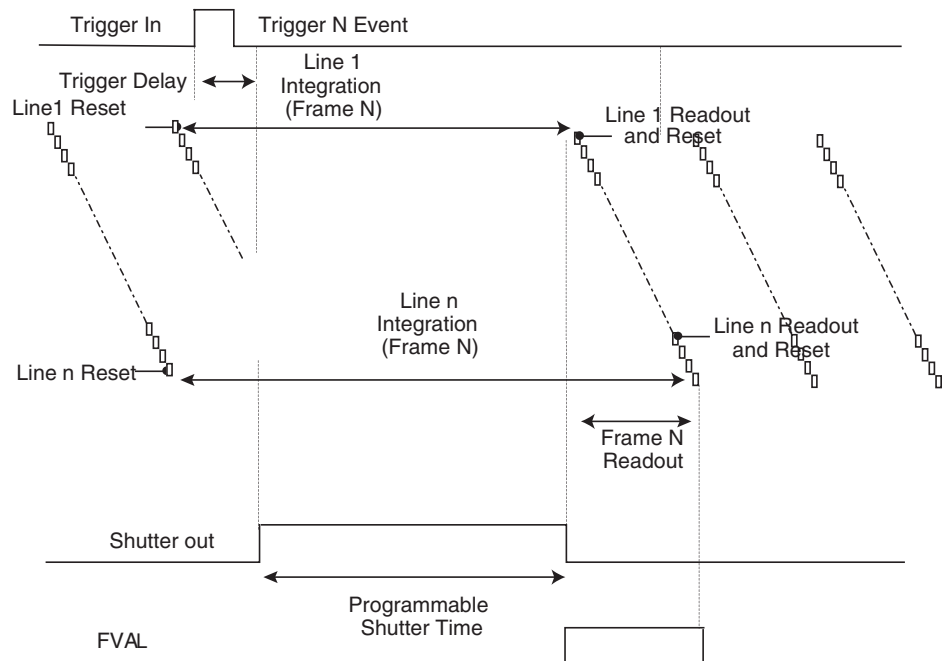
The trigger delay is a few μs . The minimum pulse duration is 1 μs . The edge of trigger is programmable. The source of trigger is selectable between Camera Link CC1 signal and TTL_IO trigger input. The period is defined by the programmable shutter time + readout time + wait. Therefore the minimum period is reduced to 1 \times readout time. As the integration time is not the same for all lines (in the following timing diagram line n integration time is greater than line 1 integration time) this mode must be used with a pulsed light source or a shutter element. Moreover any residual light when shutter output signal is inhibited must be avoided. The exposure time is defined by the shutter time and all the lines are exposed during the same time.

See register Aperture Shutter Time @ 246H Internal Register Mapping on [page 16](#).

Table 4-3. Shutter Time Values at Triggered Mode without Full Reset

Label	Description	2M60	2M30
Tsh	Maximum shutter time (ms)	655	1310
T1	Step duration (μs)	10	20

Figure 4-4. Triggered Mode Without Full Reset Chronogram



4.1.5 ITC Mode

Principle: An external sync controls both the integration time and the frame rate.

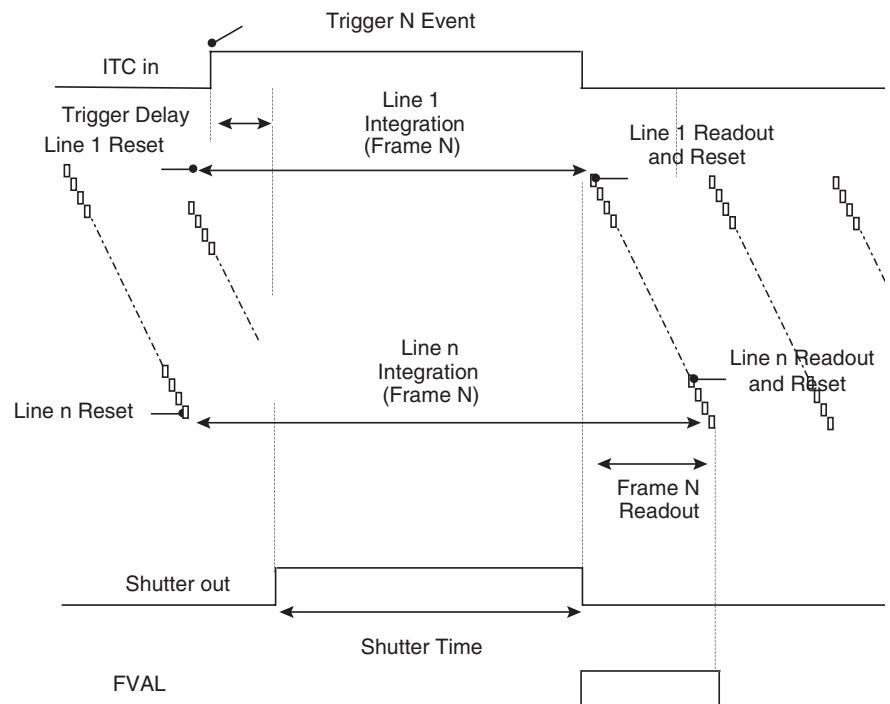
The trigger event initiates the following sequence:

- Stop of readout frame in progress and reset of readout pointer to line 1
- Shutter output signal is activated during a time defined by the high state of the ITC signal
- Readout of frame N. The readout data is forwarded to the Camera Link interface (FVAL active) starting with the first line
- Readout of dummy frames (to prevent against large dark current integration) while the camera waits for the next trigger event

The integration delay is a few μs . The minimum pulse duration is $1 \mu\text{s}$. The source of ITC signal is selectable between Camera Link CC1 signal and TTL_IO trigger input. See Register Mode Control @ 204H Internal Register Mapping on [page 16](#). The period is defined by the ITC signal period.

As the integration time is not the same for all lines (in the following timing diagram line n integration time is greater than line 1 integration time) this mode must be used with a pulsed light source or a shutter element. Moreover any residual light when shutter output signal is inhibited must be avoided. The exposure time is defined by the ITC signal high state time and all the lines are exposed during the same time.

Figure 4-5. ITC Mode Chronogram

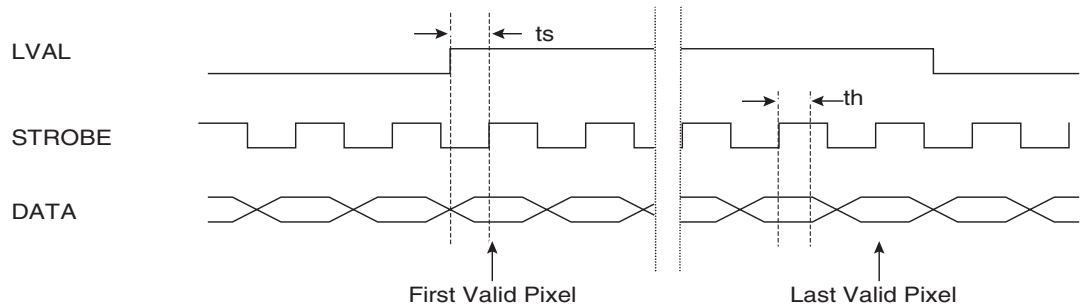


4.2 Output Data Timing

Table 4-4. Timing Values

Label	Description	Min	Typ	Max
Ts	Input setup to clock delay	1ns		
Th	Output hold from clock delay	1ns		

Figure 4-6. Output Data Chronogram



5. Camera Features

5.1 Region of Interest

The full resolution of the camera is 2096 pixels by 1184 lines. You might program a smaller resolution in order to reduce the readout time. You must be careful that depending on the sequencing mode, the exposure time can be reduced too. The authorized values for horizontal size are 32 to 2096 pixels. This value is rounded to the lower multiple of 16 pixels. The authorized values for vertical size are 32 to 1184 lines. This value is rounded to the lower multiple of 9 lines. See registers ROI area @ 280H, 282H, 284H and 286H Internal Register Mapping on [page 16](#).

Examples of frame rate versus resolution:

Table 5-1. R.O.I Performance

ROI Size	Frame Rate 2M60 (fps)	Frame Rate 2M30 (fps)
2096 × 1184	48	24
1920 × 1080	60	30
1600 × 999	75.7	37
640 × 477	157	78

5.2 Analog Gain

The analog gain can be adjusted by setting the gain register via the serial communication.

- Gain adjusted from 0 dB to 18 dB: code 0 to 6
- Step 3 dB
- Nominal gain (factory configuration): 0 dB

See register Sensor Analog Gain @ 240H, Internal Register Mapping on [page 16](#).

5.3 Output Format

The data format available on the Camera Link output interface is programmable via the serial interface.

Note: The pixel depth is set by default at 12-bit, it can be set to 10 or 8-bit. The assignment for each configuration comply with the specifications of the Camera Link interface standard. See register Mode Control bits [3:2] @ 204H, Internal Register Mapping [page 16](#) .

5.4 Test Pattern

In normal mode, the digital video signal from the sensor is available on the Camera Link output interface. For test purposes a digital pattern is generated and is available instead of the video signal in the Camera Link output interface. The pattern can be fixed or sliding. The fixed digital pattern is ramp-up from 960 LSB code to 2008 LSB code (line width). The same pattern is shown for each line:

Figure 5-1. Test Pattern View



The sliding pattern starts with the fixed pattern, the first code of each line is then incremented by two on each frame. It is useful to validate the connection to the acquisition system before the adjustment settings of the image capture. The output format is the only processing which applies to the test pattern. See "[Digital Processing Synoptic](#)" on [page 14](#).

See register Mode Control bits [1:0] @ 204H, Internal Register Mapping on [page 16](#).

5.5 Contrast Expansion

This processing does not apply to the test pattern. The digital gain and offset can be adjusted via the serial communication in order to focus on a particular part of the dynamic range.

- Gain adjusted from x1 to x32.875: code 0 to 255
- Step 0.125
- Nominal gain (factory configuration): $\times 1$

See register Digital Gain @ 242H, Internal Register Mapping on [page 16](#).

- Offset adjusted from -4096 to +4095: code 0 to 8191 in 2's complement
- Step 1
- Nominal offset (factory configuration): 0

See register Digital Offset @ 244H, Internal Register Mapping on [page 16](#).

See register Processing Control bits [1:0] @ 202H, Internal Register Mapping on [page 16](#).

5.6 Look-up Table (LUT)

The look-up Table is a conversion table which applies to the sensor data. At each input pixel value corresponds a single output value. This allows you to apply a correction table like a gamma correction for example. The Look-up Table does not apply to the test pattern. The Look-up Table might be generated by the camera by programming the gamma setting:

- Gamma 0.125 to 7.875: code 1 to 63 (0 not admitted)

You might also write your own correction table via the serial communication channel. Four banks are available to store four distinct correction tables.

See register LUT Coefficient Save in Dataflash @ 10DH, Internal Register Mapping on [page 16](#).

See register LUT Coefficient Restore in Dataflash @ 10EH, Internal Register Mapping on [page 16](#). See register Processing Control bit 2 @ 202H, Internal register mapping on [page 16](#).

5.7 Fixed Pattern Noise (FPN) Correction

The fixed pattern noise (FPN) is a spatial fluctuation of the sensor data particularly between successive columns. The purpose is to calculate an offset for each column of the frame in the darkness. The table of column offsets is stored in the internal memory. If the FPN correction is then enabled the offset values are subtracted to the value of the input pixel. Two methods are available to realize this processing: the off-line calibration and the online correction.

5.8 Off-line Calibration

A calibration step is required while the camera is in darkness condition. Offset coefficients for each column are calculated on an average value measured on the 1024 first lines. Offset coefficients are 8-bit data. Therefore to be efficient the pixel value should be always within the values 1LSB to 255 LSB. If not, the overflow/underflow flags are set in the status register. The calibration step must be done in full resolution. Calibration data can be saved in nonvolatile memory and four distinct banks are reserved for this use. You might access to these banks in read or write mode.

See register Processing Control bits [4:3] @ 202H, Internal register mapping on [page 16](#).

See register Calibration Control @ 200H, Internal register mapping on [page 16](#).

See register FPN Coefficient Save in Dataflash @ 10BH, Internal register mapping on [page 16](#).

See register FPN Coefficient Restore in Dataflash @ 10CH, Internal Register Mapping on [page 16](#).

5.9 Online Correction

No calibration step is required. When online correction is enabled the camera calculates the offset coefficients for each column on masked lines and then processes the input sensor data. These coefficients are updated at each frame. The calculated values are less accurate with these methods but unlike the off-line calibration do not depend on the settings like the analog gain.

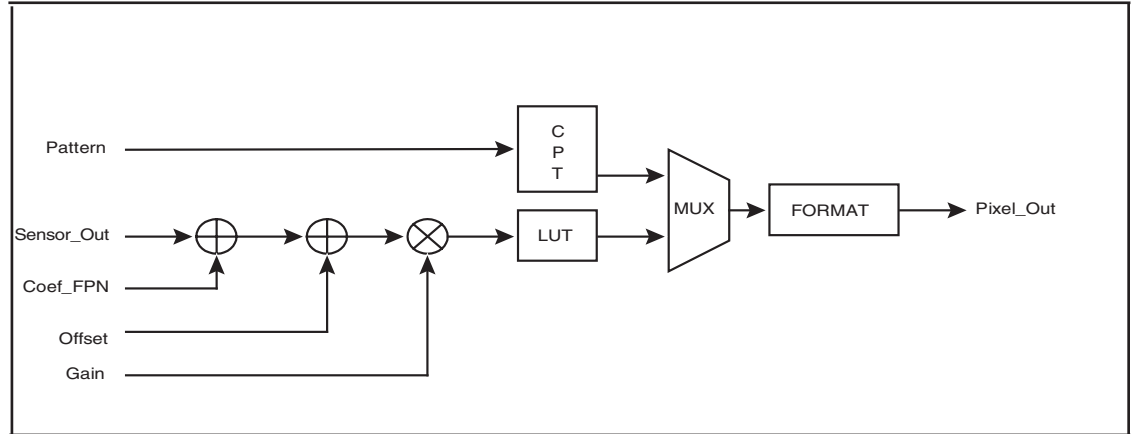
See register Processing Control bits [4:3] @ 202H, Internal Register Mapping on [page 16](#).

See register FPN Coefficient Save in Dataflash @ 10BH, Internal Register Mapping on [page 16](#).

See register FPN Coefficient Restore in Dataflash @ 10CH, Internal Register Mapping on [page 16](#).

5.10 Digital Processing Synoptic

Figure 5-2. Synoptic



5.11 Defective Pixels Correction

The sensor may present defective pixels. Hot pixels have a higher value than the average of their neighbor pixels. A correction can be applied by replacing these defective pixels by the average value of their neighbors. The threshold which determines if a pixel is defective can be programmed. This threshold is defined in LSB value above the average value of the neighbor pixels.

See register Defective Pixel Control @ 2C4H, Internal Register Mapping on [page 16](#).

See register Hot Pixel Detection Threshold @ 2C0H, Internal Register Mapping on [page 16](#).

5.12 LED Indicator

The green LED on the rear panel gives information on the internal state of the camera. On power up, after internal configuration, the LED flashes on and has the following behavior (decreasing priority order):

- Internal hardware error or configuration error: fast blinking
- Waiting for external trigger (triggered and ITC modes): slow blinking
- All other situation: continuous

6. Electrical Interface

6.1 Power Supply

It is recommended to insert a 1A fuse between the power supply and the camera. The voltage ripple of the power supply shall be below ± 50 mVp-p at BW = 50 MHz to have full camera performance.

Table 6-1. Power Supply Description

Signal Name	I/O	Type	Description
PWR	P	-	DC power input: +12V to + 24V
GND	P	-	Electrical and mechanical ground

Note: I = input, O = output, I/O = bi-directional signal, P = power/ground, NC = not connected.

6.2 Command and Control

The Camera Link interface provides four LVDS signals dedicated to camera control (CC1 to CC4). On the ATMOS, one of them is used to synchronize the camera on external events.

Table 6-2. Camera Link Input Description

Signal Name	I/O	Type	Description
TRIG1	I	RS644	CC1 - Synchronization input

Note: I = input, O = output, I/O = bi-directional signal, P = power/ground, NC = not connected.

The TTL/I/O interface provides two TTL signals dedicated to camera control.

Table 6-3. TTL/I/O Description

Signal Name	I/O	Type	Description
TRIGGER	I	5 V-TTL	External trigger input
SHUTTER	O	3 V-TTL	Shutter output, maximum output current 1.6 mA

Note: I = input, O = output, I/O = bi-directional signal, P = power/ground, NC = not connected.

See register Mode Control @ 204H, Internal Register Mapping on [page 16](#).

6.3 Video Data

Data and Enable signals are provided on the Camera Link interface.

Table 6-4. Camera Link Output Description

Signal Name	I/O	Type	Description
ODD-D[11-0]	O	RS644	Odd pixel data, ODD-00 = LSB, ODD-11 = MSB
EVEN-D[11-0]	O	RS644	Even pixel data, EVEN-00 = LSB, EVEN-11 = MSB
STROBE	O	RS644	Output data clock, data valid on the rising edge
LVAL	O	RS644	Line valid or line enable, active high signal
FVAL	O	RS644	Frame valid or frame enable, active high signal

Note: 1. I = input, O = output, I/O = bi-directional signal, P = power/ground, NC = not connected.
 2. Note: DVAL, as defined in the Camera Link standard, is not used. DVAL is permanently tied to 1 (high) level.



6.4 Serial Communication

The Camera Link interface provides two LVDS signal pairs for the communication between the camera and the frame grabber. This is an asynchronous serial communication based on RS-232 protocol.

The configuration of the serial line is:

- Full duplex/without handshaking
- 8-bit data, no parity bit, 1 stop bit
- 9600 bauds at power up, then programmable up to 115200 bauds (see register Communication Speed Multiplier @ 001H, Internal Register Mapping on [page 16](#)).

Table 6-5. Camera Link Serial Communication Description

Signal Name	I/O	Type	Description
SerTFG	O	RS644	Differential pair for serial communication to the frame grabber
SerTC	I	RS644	Differential pair for serial communication from the frame grabber

6.4.1 Internal Register

Table 6-6. Internal Register Mapping

Start Addr (Hex)	Size (Dec)	End Addr (Hex)	Access Type		Factory Settings	Description
			Processing	Internal Task		
000	1		RO	RO		Synchronization register for serial communication (value 00)
001	1		RW	-	1	Communication speed multiplier (9600 - 115,2K): volatile register 1, 2, 3, 4, 6, 8, 12
040	51		RO	-		Hardware identifier
080	8		RO	-		Firmware identifier
0C0	51		RW	-		User identifier
100	4		RW	RW		Status (ref. Camera Status Management)
104	4		WO	-		Lock/Unlock mode: advanced user/user 1: Lock advanced user mode (into user mode) Unlock key value: unlock user
108	1		RO	-		Privilege level 1: Advanced user mode 2: User mode
109	1		WO	-		Current configuration save in Eeprom 1: User settings (allowed only for advanced user mode) 2 to 4: User settings

Table 6-6. Internal Register Mapping (Continued)

Start Addr (Hex)	Size (Dec)	End Addr (Hex)	Access Type		Factory Settings	Description
			Processing	Internal Task		
10A	1		RW	-	0	Current configuration restore from Eeprom 1 to 4: User settings
10B	1		WO	-		FPN coefficient save in dataflash 1 to 4 (1 allowed only for advanced user mode)
10C	1		RW	-	1	FPN coefficient restore in dataflash 1 to 4
10D	1		WO	-		LUT coefficient save in dataflash 1 to 4 (1 allowed only for advanced user mode)
10E	1		RW	-	1	LUT coefficient restore in dataflash 1 to 4
200	2		RW	RW	0	Calibration control [0] = off-line calibration enabled (0: disabled; 1: enabled)
202	2		RW	-	0	Processing control: [0] = offset correction enable (0: disabled; 1: enabled) [1] = gain correction enable (0: disabled; 1: enabled) [2] = look-up table correction enable (0: disabled; 1: enabled)[[4:3] = fpn correction mode (00: disabled; 01: off-line fpn correction enabled; 11: on-line fpn correction enabled)
204	2		RW	-	0	Mode control: [1:0] = test pattern (00: disabled; 01: fixed test pattern; 10: dynamic test pattern) [3:2] = output format (00:12-bit; 01:10-bit; 10:8-bit) [[7:5] = synchronization mode (000: Free-run; 001: External triggered; 010: external triggered without full reset; 011: integration time controlled); others reserved [8] = trigger source (0: Camera Link; 1: external) [9] = trigger polarity (0:positive edge; 1: negative edge) [10] = shutter polarity output (0: positive edge; 1: negative edge)
206	1		WO			Software reset: 1 = camera reset



Table 6-6. Internal Register Mapping (Continued)

Start Addr (Hex)	Size (Dec)	End Addr (Hex)	Access Type		Factory Settings	Description
			Processing	Internal Task		
240	2		RW	-	0	Sensor analog gain: [3:0] = analog gain; value from 0 dB (= 0) to 18 dB (= 6) by step of 3 dB
242	2		RW	-	0	Digital gain (extended dynamic range): [7:0] = gain; value from 1.000 (= 0) to 32.875 (= 255) in Q 8.3 representation
244	2		RW	-	0	Digital offset (extended dynamic range): [12:0] = offset; value from -4096 to + 4095 in 2's complement
246	2		RW	-	1	Aperture shutter time: [15:0] = shutter time; value from 0 to 65535 (for 2M60: 0 to 655 ms by step of 10 μ s) (for 2M30: 0 to 1310 ms by step of 20 μ s)
248	2		RW	-	1600	ERS: [10:0] value from 0% (= 0,Dark) to 100% (= 1600, clear) in Q11.4 representation
280	8	287	RW			ROI area: Addr 280, size 2, default 0: ROI horizontal start value from 0 to 2080 Addr 282, size 2, default 0 ROI vertical start value from 0 to 1182 Addr 284, size 2, default 1920 ROI vertical size value from 32 to 2096 Addr 286, size 2, default 1080 ROI vertical size value from 32 to 1184
2C0	2		RW		50	Hot pixel detection threshold: [10:0] = hot pixel threshold
2C4	1		RW	-	0	Defective pixels control: [0] = hot pixel detection (0: disabled; 1: enabled)
300	1		WO	-		Gamma correction: [5:0] = gamma settings; value from 0.125 (= 1) to 7.875 (= 63) in Q6.3 representation
1000	1312	151F	RW	-	0	FPN coefficients (8-bit): Format: Fpn [0]; Fpn[1]; Fpn [2];...
2000	8192	3FFF	RW	-	linear	Look-up table (4096 \times 16-bit): Format: Lut [0]; Lut [1]; ... ; Lut [4095] value: 0 to 4095

Note: RO: Read Only register, WO: Write Only register, RW: Read and Write register.

6.4.2 Camera Settings Memory

ATMOS cameras have 5 banks to save settings:

- Bank 0 contains the factory settings. This bank cannot be modified by the user
- Bank 1 to 4 are used to store 4 different settings
- Bank 1 might be protected by an advanced user (see Register @ 104H). Contact Atmel for details

7. Connector Description

All connectors are on the rear panel. Better results are obtained by using shielded cables (foil and braid shielded).

Note: cables for digital signals shall be twisted pairs.

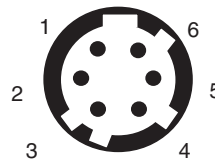
7.1 Power Supply

Camera connector type: Hirose HR10A-7R-6PB (male)

Cable connector type: Hirose HR10A-7P-6S (female)

Figure 7-1. Power Supply Pinout

Power Connector : J01				
Signal	Pin		Signal	Pin
PWR	1		GND	4
NC	2		NC	5
PWR	3		GND	6



Receptacle Viewed from Camera Back


7.2 Camera Link Connector

Standard Camera Link cable shall be used to ensure the full electrical compatibility.

- Camera connector type: MDR-26 (female) ref. 3M 10226-2210VE
- We recommend to use a Camera Link standard shielded cable as 3M 14X26-SZLB-XXX-0LC

Figure 7-2. Camera Link Pinout

Command and Control Connector : J02					
Signal	Pin		Signal	Pin	
GND	1		GND	14	
X0-	2		X0+	15	
X1-	3		X1+	16	
X2-	4		X2+	17	
Xclk-	5		Xclk+	18	
X3-	6		X3+	19	
SerTC+	7		SerTC-	20	
SerTFG-	8		SerTFG+	21	
CC1-	9		CC1+	22	
CC2+	10		CC2-	23	
CC3-	11		CC3+	24	
CC4+	12		CC4-	25	
GND	13		GND	26	



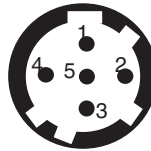
7.3 TTL I/O

Camera connector type: Hirose HR10A-7R-5SB (female)

Cable connector type: Hirose HR10A-7P-5P (male)

Figure 7-3. TTL/IO Pinout

TTL IO Connector : J03				
Signal	Pin		Signal	Pin
TRIGGER	1		GND	4
GND	2		NC	5
SHUTTER	3			



Receptacle Viewed from Camera Back

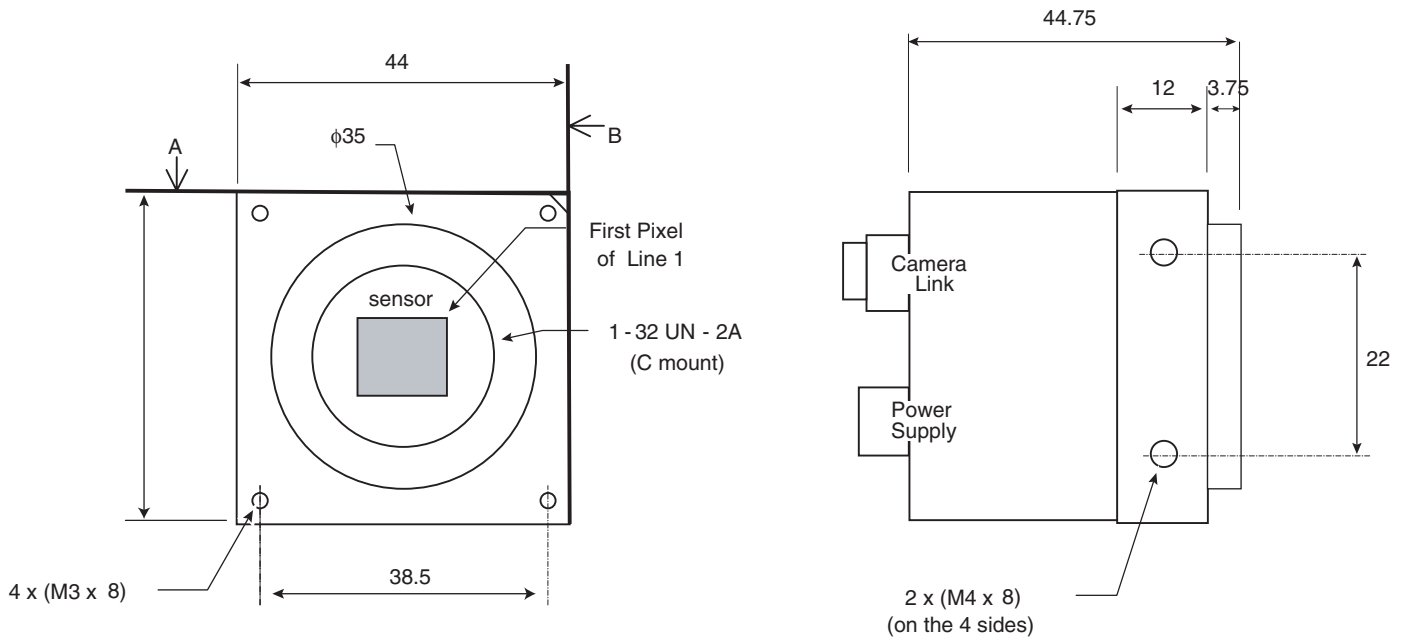
8. Mechanical Drawing

Note: (All dimensions are in mm)

Figure 8-1. Front Panel View



Figure 8-2. Front Panel Mechanical Drawing

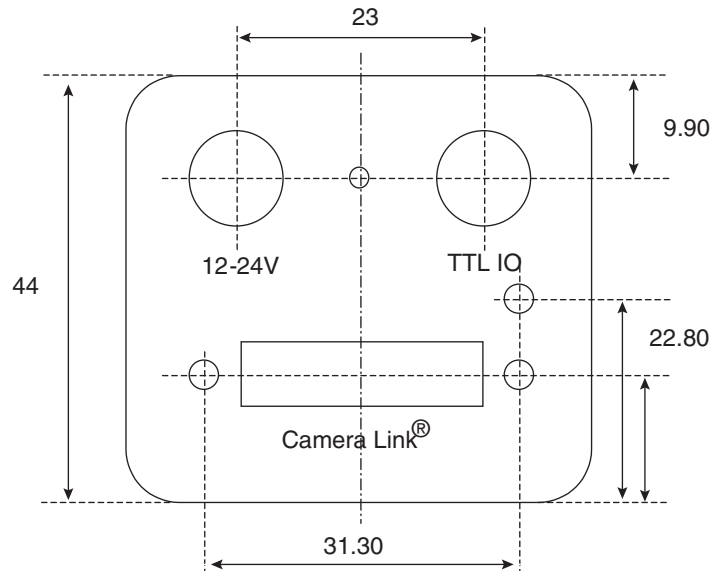


- Note:
1. A and B are mechanical reference plans.
 2. Sensor alignment $\Delta x, y$ refers to the optical axis.
 3. Sensor alignment $\Delta 0_{xy}$ refers to the reference plans.

Figure 8-3. Rear Panel



Figure 8-4. Rear Panel Mechanical Drawing



9. Ordering Code

Table 9-1. Ordering Code

Part Number	Description
AT71-ATM2M60M-B0	ATMOS 2M60 with housing + power supply connector + TTL I/O Connector + CD-Rom
AT71-ATM2M30M-B0	ATMOS 2M30 with housing + power supply connector + TTL I/O Connector + CD-Rom

Delivery:

ATMOS areascan cameras are delivered with:

- Power supply female connector HR10A-7P-6S
- TTL I/O male connector HR10A-7P-5P
- CD-rom with:
 - Friendly software CommCam
 - Documentation

Note: Optical lens is not provided.



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