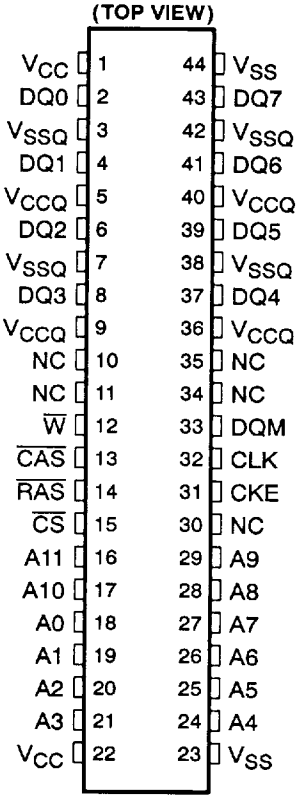
TMS626802, TMS636802
1048576-WORD BY 8-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORIES

SMOS182 – FEBRUARY 1994

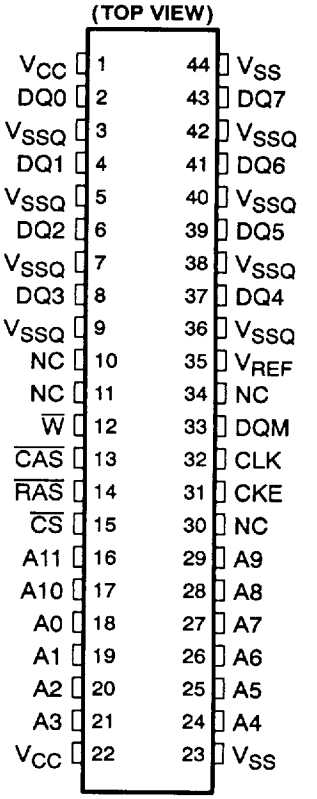
- **Organization . . . 1M × 8 × 2 Banks**
- **3.3-V Power Supply (10% Tolerance)**
- **Two Banks for On-Chip Interleaving (Gapless Accesses)**
- **High Bandwidth – Up to 100-MHz Data Rates**
- **Burst Length Programmable to 1, 2, 4, or 8**
- **Programmable Output Sequence – Serial or Interleave**
- **Chip Select and Clock Enable for Enhanced System Interfacing**
- **Cycle-by-Cycle DQ Bus Mask Capability**
- **Programmable Read Latency From Column Address**
- **Self-Refresh Capability**
- **High-Speed, Low-Noise LVTTL and GTL Interfaces**
- **Power-Down Mode**
- **Compatible With JEDEC Standards**
- **4K Refresh (Total for Both Banks)**
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME	ACTV COMMAND TO READ OR WRT COMMAND	REFRESH TIME INTERVAL
	t_{CK} (MIN)	t_{RCD} (MIN)	t_{REF} (MAX)
TMS6x6802-10	10 ns	30 ns	64 ms
TMS6x6802-12	12.5 ns	35 ns	64 ms
TMS6x6802-15	15 ns	40 ns	64 ms

TMS626802 (LVTTL) DGE PACKAGE (TOP VIEW)



TMS636802 (GTL) DGE PACKAGE (TOP VIEW)



description

The TMS626802 series are high-speed 16777216-bit synchronous dynamic random-access memories organized as two banks of 1048576 words with eight bits per word.

All inputs and outputs of the TMS626802 series are compatible with the low-voltage TTL (LVTTL) interface.

The TMS636802 series are high-speed 16777216-bit synchronous dynamic random-access-memories organized as two banks of 1 048 576 words with eight bits per word.

All inputs and outputs of the TMS636802 series are compatible with the Gunning Transceiver Logic (GTL) interface.

PIN NOMENCLATURE	
A0–A10	Address Inputs
	A0–A10 Row Addresses
	A0–A8 Column Addresses
	A10 Automatic Precharge Select
A11	Bank Select
$\overline{CAS}$	Column-Address Strobe
CKE	Clock Enable
CLK	System Clock
$\overline{CS}$	Chip Select
DQ0–DQ7	SDRAM Data Inputs/Outputs
DQM	Data/Output Enable
NC	No External Connect
$\overline{RAS}$	Row-Address Strobe
V_{CC}	Power Supply (3.3 V Typ)
V_{CCQ}	Power Supply for Output Drivers (3.3 V Typ)
V_{REF}	GTL Reference Voltage
V_{SS}	Ground
V_{SSQ}	Ground for Output Drivers
$\overline{W}$	Write Enable

ADVANCE INFORMATION

description (continued)

These synchronous DRAMs employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost. All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors and caches. The TMS6x6802 synchronous DRAMs are available in 400-mil, 44-pin surface-mount TSOP (II) packages (DGE suffix).

operation

All inputs of the '6x6802 synchronous DRAM are latched on the rising edge of the system (synchronous) clock. The outputs, DQ0–DQ7, are also referenced to the rising edge of CLK. The '6x6802 has two banks that are accessed independently. A bank must be activated before it can be accessed (read from or written to). Refresh cycles refresh both banks alternately.

Five basic commands or functions control most operations of the '6x6802:

- Bank activate/row address entry
- Column address entry/write operation
- Column address entry/read operation
- Bank deactivate
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$/self-refresh entry

Additionally, operation can be controlled by three methods: using chip select ($\overline{\text{CS}}$) to select/deselect the devices, using DQM to enable/mask the DQ signals on a cycle-by-cycle basis, or using CKE to suspend (or gate) the CLK input. The device contains a mode register that must be programmed for proper operation.

Tables 1 through 3 show the various operations that are available on the '6x6802. These truth tables identify the command and/or operations and their respective mnemonics. Each truth table is followed by a legend that explains the abbreviated symbols. An access operation refers to any READ (or READ-P) or WRT (or WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (or READ-P) or WRT (or WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

ADVANCE INFORMATION

EPIC is a trademark of Texas Instruments Incorporated.

operation (continued)

Table 1. Basic Command Truth Table†

COMMAND	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A9–A0	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	X	X	A9 = X A8 = 0 A7 = 0 A6–A0 = V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate/row address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column-address entry/write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column-address entry/write operation with auto-deactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column-address entry/read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column-address entry/read operation with auto-deactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
Burst stop	SB = actv	L	H	H	L	X	X	X	STOP
No operation	X	L	H	H	H	X	X	X	NOOP
Control-input inhibit/No operation	X	H	X	X	X	X	X	X	DESL
CBR refresh‡	T = B = deac	L	L	L	H	X	X	X	REFR

† For execution of these commands on cycle n, CKE(n) must be high and satisfy t_{CESP} from power-down exit (PDE), t_{CES} and nCLE from clock-suspend (HOLD) exit, and t_{CESP} and t_{RC} from self-refresh (SLFR) exit. DQM(n) is a don't care.
‡ CBR or self-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend:

L = Logic low
H = Logic high
X = Don't care
V = Valid
T = Bank T
B = Bank B
actv = Activated
deac = Deactivated
BS = Logic high to select bank T; logic low to select bank B
SB = Bank selected by A11 at cycle n

ADVANCE INFORMATION

operation (continued)

Table 2. CKE-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	CKE (n−1)	CKE (n)	$\overline{CS}$ (n)	$\overline{RAS}$ (n)	$\overline{CAS}$ (n)	$\overline{W}$ (n)	MNEMONIC
Self-refresh entry	T = B = deac	H	L	L	L	L	H	SLFR
Power-down entry at n + 1	T = B = no access operation‡	H	L	L	H	H	H	PDE
		H	L	H	X	X	X	PDE
Self-refresh exit	T = B = self refresh	L	H	L	H	H	H	—
		L	H	H	X	X	X	—
Power-down exit	T = B = power down	L	H	X	X	X	X	—
CLK suspend at n + 1	T or B = access operation‡	H	L	X	X	X	X	HOLD
CLK suspend exit at n + 1	T or B = access operation‡	L	H	X	X	X	X	—

† For execution of these commands, A0–A11 (n) and DQM (n) are don't cares.
‡ An access operation refers to any READ (-P) or WRT (-P) command in progress at cycle n. Access operations include the cycle upon which the READ (-P) or WRT (-P) command is entered and all subsequent cycles through the completion of the access burst.

Legend:

n	=	CLK cycle number
L	=	Logic low
H	=	Logic high
X	=	Don't care
T	=	Bank T
B	=	Bank B
deac	=	Deactivated

ADVANCE INFORMATION

operation (continued)

Table 3. DQM-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	DQM (n)	D0–D7 (n)	Q0–Q7 (n+2)	MNEMONIC
—	T = deac and B = deac	X	N/A	Hi-Z	—
—	T = actv and B = actv (no access operation)‡	X	N/A	Hi-Z	—
Data-in enable	T = write or B = write	L	V	N/A	ENBL
Data-in mask	T = write or B = write	H	M	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	V	ENBL
Data-out mask	T = read or B = read	H	N/A	Hi-Z	MASK

† For execution of these commands, CKE(n) must be high and satisfy t_{CESP} from power-down exit (PDE), t_{CES} and nCLE from clock-suspend (HOLD) exit, and t_{CESP} and t_{RC} from self-refresh (SLFR) exit. $\overline{CS}$ (n), $\overline{RAS}$ (n), $\overline{CAS}$ (n), $\overline{W}$ (n), and A0–A11 (n) are don't cares.

‡ An access operation refers to any READ (-P) or WRT (-P) command in progress at cycle n. Access operations include the cycle upon which the READ (-P) or WRT (-P) command is entered and all subsequent cycles through the completion of the access burst.

Legend:

n	=	CLK cycle number
L	=	Logic low
H	=	Logic high
X	=	Don't care
V	=	Valid
M	=	Masked input data
N/A	=	Not applicable
T	=	Bank T
B	=	Bank B
actv	=	Activated
deac	=	Deactivated
write	=	Acitvated and accepting data in on cycle n
read	=	Activated and delivering data out on cycle n + 2

ADVANCE INFORMATION

burst sequence

All data for the '6x6802 is written or read in a *burst* fashion. That is, a single starting address is entered into the device and then the '6x6802 internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first may be at preceding, as well as succeeding, column addresses depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst (see Tables 4 through 6). The length of the burst sequence can be user programmed to be either 1, 2, 4, or 8 accesses. After a read burst is completed (as determined by the programmed burst length), the outputs are in the high-impedance state until the next read access is initiated. When using terminated DQ buses for GTL interfacing, turning off the output buffers at the device will result in the DQ lines pulling up to the terminating voltage, V_{TT}.

Table 4. 2-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0			
	DECIMAL		BINARY	
	START	2ND	START	2ND
Serial	0	1	0	1
	1	0	1	0
Interleave	0	1	0	1
	1	0	1	0

Table 5. 4-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A1 A0							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH	START	2ND	3RD	4TH
Serial	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	10	11	00	01
	3	0	1	2	11	00	01	10
Interleave	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00

burst sequence (continued)

Table 6. 8-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A2 A1 A0															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

latency

The beginning data output cycle of a read burst can be programmed to occur 1, 2, or 3 CLK cycles after the read command (see setting the mode register, page 9). This feature allows the user to adjust the '6x6802 to operate in accordance with the system's capability to latch the data output from the '6x6802. The delay between the READ command and the beginning of the output burst is known as *read latency* (also known as $\overline{CAS}$ latency). After the initial output cycle has commenced, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies are restricted based on the particular maximum frequency rating of the '6x6802.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and not determined by the mode register contents.

two-bank operation

The '6x6802 contains two independent banks, which can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank must then be deactivated before it can be activated again with a new row address. The bank activate/row address entry command (ACTV) is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ or a WRT command (or READ-P or WRT-P) or by use of the deactivate bank (DEAC) command. Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the bank deactivation description).

two-bank row access operation

The two-bank feature allows the user to access information on random rows at a higher rate of operation than is possible with a standard DRAM. This can be accomplished by activating one bank with a row address and, while the data stream is being accessed to/from that bank, activating the second bank with another row address. When the data stream to/from the first bank is complete, the data stream to/from the second bank can commence without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses. In this manner, operation can continue in an interleaved "ping-pong" fashion. Figure 22 is an example of two-bank row interleaving with automatic deactivate for the case of read latency of 3 and a burst length of 8.

two-bank column access operation

The availability of two banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A11 can be used to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Figure 23 is an example of two-bank column interleaving with a read latency of 3 and a burst length of 2.

bank deactivation (precharge)

Both banks can be simultaneously deactivated (placed in precharge) by use of the DCAB command. A single bank can be deactivated by use of the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A11 selects the bank to be precharged as shown in Table 1. A bank can also be deactivated automatically by use of A10 during a READ or WRT command. If A10 is held high during the entry of a READ or WRT command, the accessed bank (selected by A11) will automatically be deactivated upon completion of the access burst. If A10 is held low during READ or WRT command entry, that bank remains active following the burst. The READ and WRT commands with automatic deactivation are denoted READ-P and WRT-P.

chip select

$\overline{CS}$ (chip select) can be used to select or deselect the '6x6802 for command entry, such as might be required for multiple memory device decoding. If $\overline{CS}$ is held high on the rising edge of CLK (DESL command), the device will not respond to $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ until the device is selected again. Device select is accomplished by holding $\overline{CS}$ low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Tables 1 and 2). The use of $\overline{CS}$ will not affect an access burst that is in progress; the DESL command can only restrict $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ input to the '6x6802.

data/output mask

Masking of individual data cycles within a burst sequence can be accomplished by use of the MASK command (see Table 3). If DQM is held high on the rising edge of CLK during a write burst, the incident data word (referenced to the same rising edge of CLK) on DQ0–DQ7 is ignored. If DQM is held high on the rising edge of CLK for a read burst, DQ0–DQ7 referenced to the second rising edge of CLK are in the high-impedance state. When using terminated DQ buses for GTL interfacing, turning off the output buffers at the device results in the DQ lines pulling up to the terminating voltage, V_{TT}. The application of DQM to data output cycles (READ burst) involves a latency of two CLK cycles, but the application of DQM to data-in cycles (WRITE burst) has no latency. The MASK command (or its opposite, the ENBL command) is performed on a cycle-by-cycle basis, allowing the user to gate any individual data cycle or cycles within either a read or a write burst sequence. Figure 11 shows an example of data/output masking.

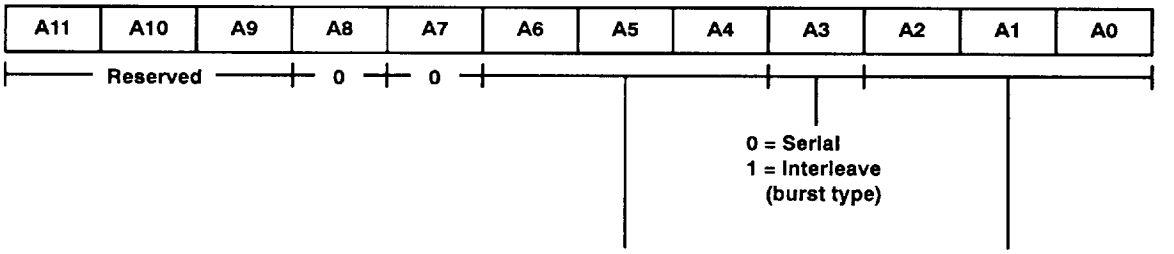
CLK suspend/power-down mode

For normal device operation, CKE should be held high to enable CLK. If CKE goes low during the execution of a READ (or READ-P) or WRT (or WRT-P) operation, the state of the DQ bus occurring at the immediate next rising edge of CLK is frozen at its current state and no further inputs are accepted until CKE is returned high. This is known as a CLK suspend operation and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE is returned high.

If CKE is brought low when no READ (or READ-P) or WRT (or WRT-P) command is in progress, the device enters power-down mode. If both banks are deactivated when power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row active or CBR refresh periods to reduce input buffer power. After power-down mode has been entered, no further inputs are accepted until CKE returns high. When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t_{CESP}) is satisfied. Table 2 shows the command configuration for a CLK suspend/power-down operation, and Figure 14 and Figure 15 show an example of the procedure.

setting the mode register

The '6x6802 contains a mode register that should be programmed by the user with the read latency, the burst type, and the burst length. This is accomplished by executing an MRS command with the information being entered on the address lines A0–A8. A logic 0 should always be entered on A7 and A8, but A9–A11 are don't care entries for the '6x6802. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register will remain unaffected. The MRS command is executed by holding $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ low, and the input mode word valid on A0–A8 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.



REGISTER BITS†			READ LATENCY‡
A6	A5	A4	
0	0	1	1
0	1	0	2
0	1	1	3

† All other combinations are reserved.
‡ Refer to timing requirements for minimum valid read latencies based on maximum frequency rating.

REGISTER BITS§			BURST LENGTH
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

§ All other combinations are reserved.

Figure 1. Mode-Register Programming

ADVANCE INFORMATION

refresh

The '6x6802 must be refreshed at intervals not exceeding t_{REF} (see timing requirements), or data may not be retained. Refresh can be accomplished by performing a read or write access to every row in both banks, or by performing 4096 $\overline{CAS}$-before-$\overline{RAS}$ (REFR) commands, or by placing the device in self-refresh. Regardless of the method used, refresh must be accomplished before t_{REF} has expired.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

Before performing a $\overline{CAS}$-before-$\overline{RAS}$ refresh, both banks must be deactivated (placed in precharge). To enter a REFR command, $\overline{RAS}$ and $\overline{CAS}$ must be low and $\overline{W}$ must be high upon the rising edge of CLK (see Table 1). The refresh address is generated internally such that after 4096 REFR commands, both banks of the '6x6802 will have been refreshed. The external address and bank select (A11) are ignored. The execution of a REFR command automatically deactivates both banks upon completion of the internal CBR cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before t_{REF} expires.

self refresh

To enter self refresh, both banks of the '6x6802 must first be deactivated and a SLFR command executed (see Table 2). The SLFR command is identical to the REFR command except that CKE is low. For proper entry of the SLFR command, CKE is low only for the same rising edge of CLK that $\overline{RAS}$ and $\overline{CAS}$ are low and $\overline{W}$ is high. Otherwise, the device would enter power-down mode. In the self-refresh mode, all refreshing signals are generated internally for both banks with all external signals (except CKE) being ignored. Data can be retained by the device automatically for an indefinite period when power is maintained (consumption is reduced to a minimum). To exit self-refresh mode, CKE must be high. New commands are issued after t_{RC} has expired. If CLK is made inactive during self-refresh, it must be returned to an active and stable condition before CKE is brought high to exit self refresh (see Figure 16). Upon exiting the self-refresh mode, a burst refresh (refresh all 4096 rows) must be executed before continuing with normal operation. This ensures that the '6x6802 is fully refreshed.

interrupted bursts

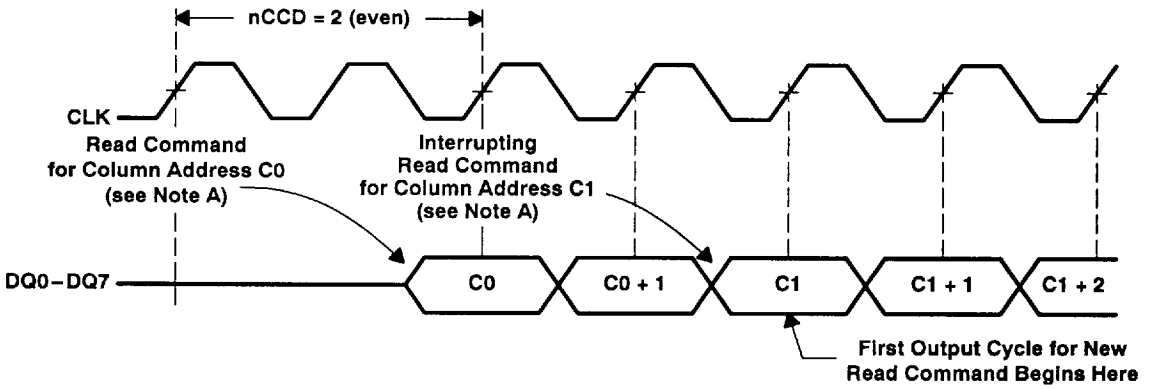
A read or write may be interrupted before the burst sequence has been completed with no adverse effects to the operation. This can be done by entering certain superseding commands as listed in Tables 7 and 8, provided that all timing requirements are met. The command interrupting either a read or a write burst should be entered only on an even number of cycles from the initial burst command (nCCD). The interruption of READ-P and WRT-P operations is not supported.

Table 7. Read-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
DEAC, DCAB	The DQ bus is in the high-impedance state when nHZP cycles are satisfied or upon completion of the read burst, whichever occurs first (see Figure 17).
WRT, WRT-P	The WRT command immediately supersedes the read burst in progress, but DQM must be high nDOD+1 cycles previous to the WRT (or WRT-P) command entry to avoid DQ bus contention (see Figure 3).
READ, READ-P	Current output cycles continue until the programmed latency from the superseding READ (or READ-P) command is met and new output cycles begin (see Figure 2).
STOP	The DQ bus is in the high-impedance state two clock cycles after the stop command is entered or upon completion of the read burst, whichever occurs first. The bank remains active. A new read or write command may not be entered for at least two cycles after the STOP command.

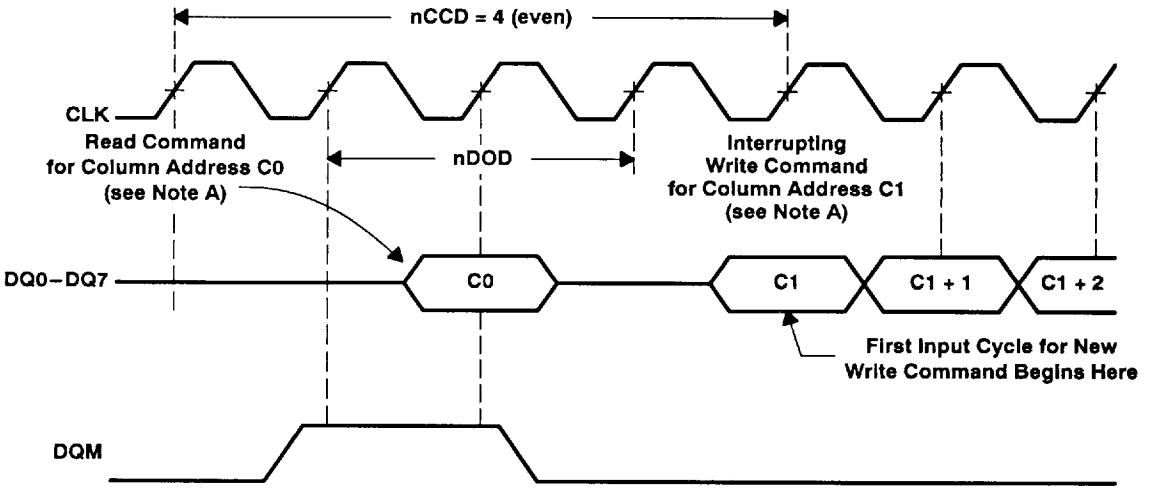
ADVANCE INFORMATION

interrupted bursts (continued)



NOTE A: For the purposes of this example, read latency = 2 and burst length > 2.

Figure 2. Read Burst Interrupted by Read Command



NOTE A: For the purposes of this example, read latency = 2 and burst length > 2.

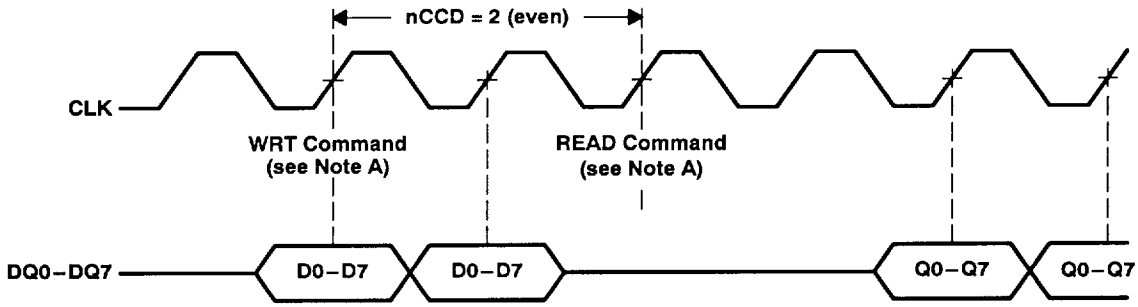
Figure 3. Read Burst Interrupted by Write Command

ADVANCE INFORMATION

Interrupted bursts (continued)

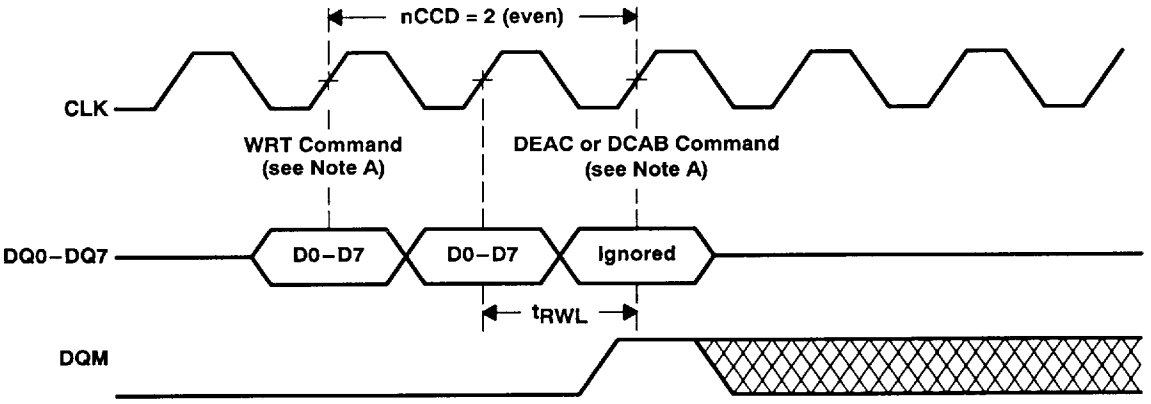
Table 8. Write-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQM must be used to mask the DQ bus such that the write recovery specification (t_{RWL}) is not violated by the interrupt (see Figure 5).
WRT, WRT-P	The new WRT (or WRT-P) command and data in immediately supersede the write burst in progress.
READ, READ-P	Data-in on previous cycle is written. No further data in is accepted (see Figure 4).
STOP	The data on the input pins at the time of the burst STOP command is not written, and no further data is accepted. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command.



NOTE A: For the purposes of this example, read latency = 2, burst length > 2.

Figure 4. Write Burst Interrupted by Read Command



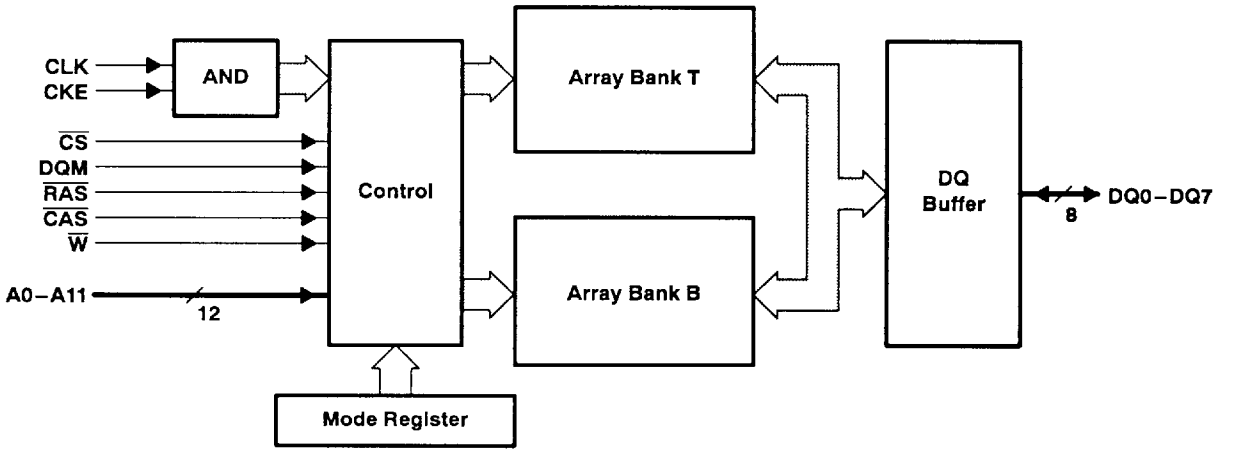
NOTE A: For the purposes of this example, read latency = 2, burst length > 2, and $t_{CK} = t_{RWL}$.

Figure 5. Write Burst Interrupted by DEAC/DCAB Command

power up

Device initialization should be performed after a power up to the full V_{CC} level. After power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands should be performed, and the mode register should be set to complete the device initialization.

functional block diagram



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 4.6 V
Supply voltage range, V_{CCQ} . . . . . – 0.5 V to 4.6 V
Input voltage range (see Note 1) . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS626802			TMS636802			UNIT
		LVTTL INTERFACING			GTL INTERFACING			
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	3	3.3	3.6	3	3.3	3.6	V
V_{CCQ}	Supply voltage for output drivers	3	3.3	3.6	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{SSQ}	Supply voltage for output drivers		0			0		V
V_{TT}	GTL terminator voltage				1.08	1.2	1.32	V
V_{REF}	GTL reference voltage				$2V_{TT}/3 - 2\%$	0.8	$2V_{TT}/3 + 2\%$	V
V_{IH}	High-level input voltage	2		$V_{CC} + 0.3$	$V_{REF} + 0.05$‡	1.2	$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage	– 0.3		0.8	– 0.3	0.4	$V_{REF} - 0.05$‡	V
T_A	Operating free-air temperature	0		70	0		70	°C

‡ V_{IH} and V_{IL} levels are only for DC testing. For AC timing, V_{IH} of 1.2 V and V_{IL} of 0.4 V should be used.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS			TMS6x6802-10			TMS6x6802-12			TMS6x6802-15			UNIT
					MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH} = −2 mA		LVTTL ('626802)	2.4			2.4			2.4			V
		$\|I_{OH}\|$ ≤ 10 µA		GTL ('636802)	V_{TT} − 0.05	1.2		V_{TT} − 0.05	1.2		V_{TT} − 0.05	1.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		LVTTL ('626802)			0.4			0.4			0.4	V
		I_{OL} = 32 mA		GTL ('636802)			0.4			0.4			0.4	
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{CC} + 0.3 V, All other pins = 0 V to V_{CC}					±10			±10			±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CC} + 0.3 V, Output disabled					±10			±10			±10	µA
I_{CC1}	Average read or write current	t_{RC} = MIN, Burst length = 1		1 bank active			90			80			70	mA
				2 banks active			160			150			125	
I_{CC2}	Standby current	Both banks deactivated	CKE = V_{IH} (see Note 3)	LVTTL ('626802)			16			16			16	mA
				GTL ('636802)			20			20			20	
			CKE = V_{IL}	LVTTL ('626802)			2			2			2	
				GTL ('636802)			3			3			3	
			CKE = 0 V (CMOS)	LVTTL ('626802)			1			1			1	
		One or both banks active	CKE = V_{IL}	LVTTL ('626802)			4			4			4	
				GTL ('636802)			5			5			5	
I_{CC3}	Consecutive CBR commands	t_{RC} = MIN					90			80			70	mA
I_{CC4}	Burst current, gapless burst	t_{CK} = MIN, No row activate (ACTV) command allowed					120			100			80	mA
I_{CC6}	Self-refresh current	CKE = V_{IL}		LVTTL ('626802)			2			2			2	mA
				GTL ('636802)			3			3			3	
		CKE = 0 V (CMOS)		LVTTL ('626802)			1			1			1	

NOTES: 2. All specifications apply to the device after power-up initialization.
3. All control and address inputs must be stable and valid.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

		MIN	MAX	UNT
$C_{i(S)}$	Input capacitance, CLK input		7	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0–A11, $\overline{CS}$, DQM, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		5	pF
$C_{i(E)}$	Input capacitance, CKE input		5	pF
C_o	Output capacitance		10	pF

NOTE 4: V_{CC} = 3.3 ± 0.3 V and bias on pins under test is 0 V.

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature†‡

			'6x6802-10		'6x6802-12		'6x6802-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CK}	Cycle time, CLK (system clock)	Read latency = 1	30		35		40		ns
		Read latency = 2	15		17.5		20		
		Read latency = 3	10		12.5		15		
t_{CKH}	Pulse duration, CLK (system clock) high		3		3.5		4		ns
t_{CKL}	Pulse duration, CLK (system clock) low		3		3.5		4		ns
t_{AC}	Access time, CLK ↑ to data out (see Note 5)	Read latency = 1		28		33		38	ns
		Read latency = 2		13		15		18	
		Read latency = 3		8		10		12	
t_{LZ}	CLK to DQ low impedance (see Note 6)		0		0		0		ns
t_{HZ}	CLK to DQ high impedance (see Note 7)	Burst length = 1, Read latency = 1		15		15		15	ns
		All other cases		7		7		7	
t_{DS}	Setup time, data input		2		2		2		ns
t_{AS}	Setup time, address		2		2		2		ns
t_{CS}	Setup time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM)		2		2		2		ns
t_{CES}	Setup time, CKE (suspend entry/exit, power-down entry)		2		2		2		ns
t_{CESP}	Setup time, CKE (power-down/self-refresh exit) (see Note 8)		8		10		12		ns
t_{OH}	Hold time, CLK ↑ to data out		2		2		2		ns
t_{DH}	Hold time, data input		2		3		4		ns
t_{AH}	Hold time, address		2		3		4		ns
t_{CH}	Hold time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM)		2		3		4		ns
t_{CEH}	Hold time, CKE		2		3		4		ns
t_{RC}	REFR command to ACTV, MRS, or REFR command; Self-refresh exit to ACTV, MRS, or REFR command		100		110		130		ns
t_{RAS}	ACTV command to DEAC or DCAB command		60	100 000	70	100 000	80	100 000	ns
t_{RCD}	ACTV command to READ or WRT command		30		35		40		ns
t_{RP}	DEAC or DCAB command to ACTV, MRS, or REFR command		40		40		50		ns

† See Parameter Measurement Information, page 19, for load circuits.
‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 5. t_{AC} is referenced from the rising transition of CLK, that is previous to the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CLK that is read latency – 1 cycles after the READ command.
6. t_{LZ} is measured from the rising transition of CLK that is read latency – 1 cycles after the READ command.
7. t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
8. If $t_{CESP} > t_{CK}$, NOOP or DESL commands must be entered until t_{CESP} is met. CLK must be active and stable (if CLK was turned off for power down) before CKE is returned high.

ADVANCE INFORMATION

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†‡

			'6x6802-10		'6x6802-12		'6x6802-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{APR}	Final data out of READ-P operation to ACTV, MRS, or REFR command		$t_{RP} + (nEP \times t_{CK})$						ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, or REFR command	Burst length = 1	60+t_{CK}		60+t_{CK}		80+t_{CK}		ns
		Burst length > 1	60		60		80		
t_{RWL}	Final data in to DEAC or DCAB command	Burst length = 1	20+t_{CK}		20+t_{CK}		30+t_{CK}		ns
		Burst length > 1	20		20		30		
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		20		25		30		ns
t_T	Transition time, all inputs (see Note 9)		1	5	1	5	1	5	ns
t_{REF}	Refresh interval			64		64		64	ms

† See Parameter Measurement Information, page 19, for load circuits.
‡ All references are made to the rising transition of CLK, unless otherwise noted.
NOTE 9: Transition time, t_T, is measured between V_{IH} and V_{IL}.

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature‡

			'6x6802-10		'6x6802-12		'6x6802-15		UNIT§
			MIN	MAX	MIN	MAX	MIN	MAX	
nEP	Final data out to DEAC or DCAB command	Burst length = 1, Read latency = 1	1		1		1		cycles
		Burst length = 1, Read latency = 2	0		0		0		
		Burst length = 1, Read latency = 3	−1		−1		−1		
		Burst length > 1, Read latency = 1	0		0		0		cycles
		Burst length > 1, Read latency = 2	−1		−1		−1		
		Burst length > 1, Read latency = 3	−2		−2		−2		
nHZP	DEAC or DCAB interrupt of data-out burst to DQ high impedance (see Note 10)	Read latency = 1	1		1		1		cycles
		Read latency = 2	2		2		2		
		Read latency = 3	3		3		3		
nCCD	READ or WRT command to interrupting STOP, READ, WRT, DEAC, or DCAB command (i = 1, 2, 3, . . .) (see Note 11)		2i		2i		2i		cycles
nCWL	Final data in to READ or WRT command in either bank	Burst length = 1	2		2		2		cycles
		Burst length > 1	1		1		1		cycles
nWCD	WRT command to first data in		0	0	0	0	0	0	cycles
nDID	ENBL or MASK command to data in		0	0	0	0	0	0	cycles
nDOD	ENBL or MASK command to data out		2	2	2	2	2	2	cycles
nCLE	HOLD command to suspended CLK edge; HOLD operation exit to entry of any command		1	1	1	1	1	1	cycles
nRSA	MRS command to ACTV, REFR, SLFR, or MRS command		2		2		2		cycles
nCDD	DESL command to control input inhibit		0	0	0	0	0	0	cycles

‡ All references are made to the rising transition of CLK, unless otherwise noted.
§ A CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during the time when CKE is asserted low).
NOTES: 10. A data-out burst can be interrupted only on an even number of clock cycles after the initial READ command is entered (refer to nCCD).
11. A read or write burst can be interrupted only at even number cycle intervals after entry of the initial READ or WRT command.

ADVANCE INFORMATION

Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters

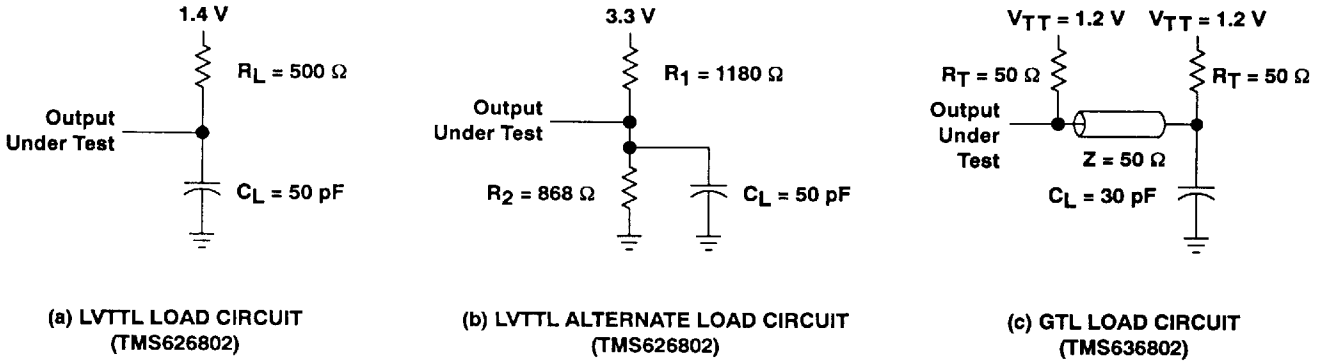
			TMS6x6802-10					TMS6x6802-12				TMS6x6802-15			UNITS
	Operating frequency		100	80	66	50	33	80	66	50	33	66	50	33	MHz
t_{CK}	Cycle time, CLK (system clock)		10	12.5	15	20	30	12.5	15	20	30	15	20	30	ns
	KEY PARAMETER		**NUMBER OF CYCLES REQUIRED**												
	Read latency, minimum programmed value		3	3	2	2	1	3	3	2	2	3	2	2	cycles
t_{RCD}	ACTV command to READ or WRT command		3	3	2	2	1	3	3	2	2	3	2	2	cycles
t_{RAS}	ACTV command to DEAC or DCAB command		6	5	4	3	2	6	5	4	3	6	4	3	cycles
t_{RP}	DEAC or DCAB command to ACTV, MRS, or REFR command		4	4	3	2	2	4	3	2	2	4	3	2	cycles
t_{RC}	REFR command to ACTV, MRS, or REFR command; self-refresh exit to ACTV, MRS or REFR command		10	8	7	5	4	9	8	6	4	9	7	5	cycles
t_{RWL}	Final data in to DEAC or DCAB command	Burst length = 1	3	3	3	2	2	3	3	2	2	3	3	2	cycles
		Burst length > 1	2	2	2	1	1	2	2	1	1	2	2	1	cycles
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		2	2	2	1	1	2	2	2	1	2	2	1	cycles
t_{APR}	Final data out of READ-P operation to ACTV, MRS, or REFR command	Burst length = 1, Read latency = 1	—	—	—	—	3	—	—	—	—	—	—	—	cycles
		Burst length = 1, Read latency = 2	—	—	3	2	2	—	—	2	2	—	3	2	cycles
		Burst length = 1, Read latency = 3	3	3	2	1	1	3	2	1	1	3	2	1	cycles
		Burst length > 1, Read latency = 1	—	—	—	—	2	—	—	—	—	—	—	—	cycles
		Burst length > 1, Read latency = 2	—	—	2	1	1	—	—	1	1	—	2	1	cycles
		Burst length > 1, Read latency = 3	2	2	1	0	0	2	1	0	0	2	1	0	cycles
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, or REFR command	Burst length = 1	7	6	5	4	3	6	5	4	3	7	5	4	cycles
		Burst length > 1	6	5	4	3	2	5	4	3	2	6	4	3	cycles

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

PARAMETER MEASUREMENT INFORMATION

general information for ac timing measurements

The ac timing measurements are based on signal rise and fall times equal to 1 ns (t_T = 1 ns) and a midpoint reference level of 1.4 V for LVTTL and 0.8 V for GTL. For signal rise and fall times greater than 1 ns, the reference level should be changed to V_{IH} min and V_{IL} max instead of the midpoint level. All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted. All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted. All specifications referring to consecutive commands are specified as consecutive commands for the same bank unless otherwise noted.

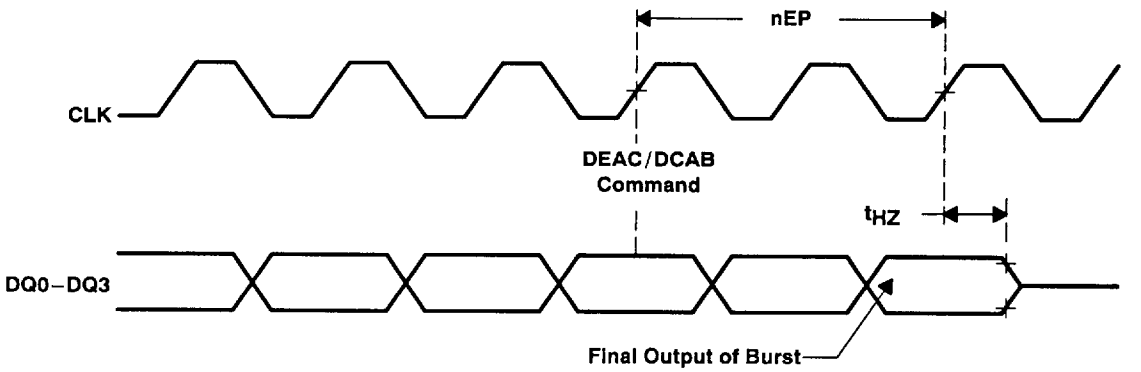


(a) LVTTL LOAD CIRCUIT (TMS626802)

(b) LVTTL ALTERNATE LOAD CIRCUIT (TMS626802)

(c) GTL LOAD CIRCUIT (TMS636802)

Figure 6. Load Circuits



NOTE A: For purposes of this example, assume read latency = 3 and burst length > 1.

Figure 7. nEP, Final Data Output to DEAC or DCAB Command

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

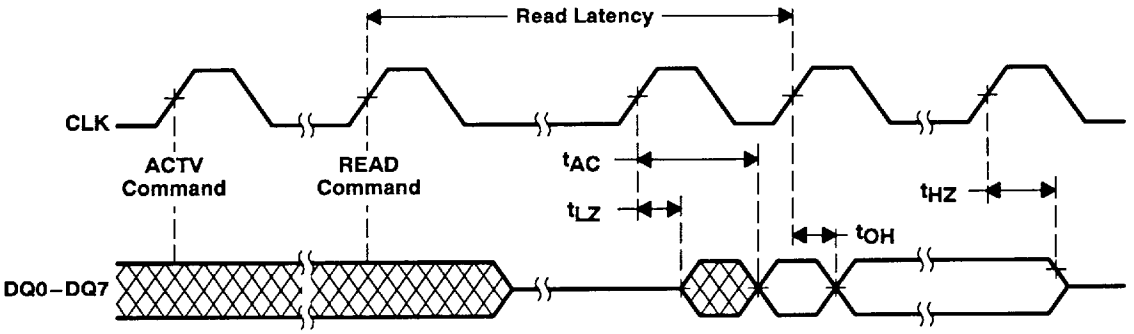
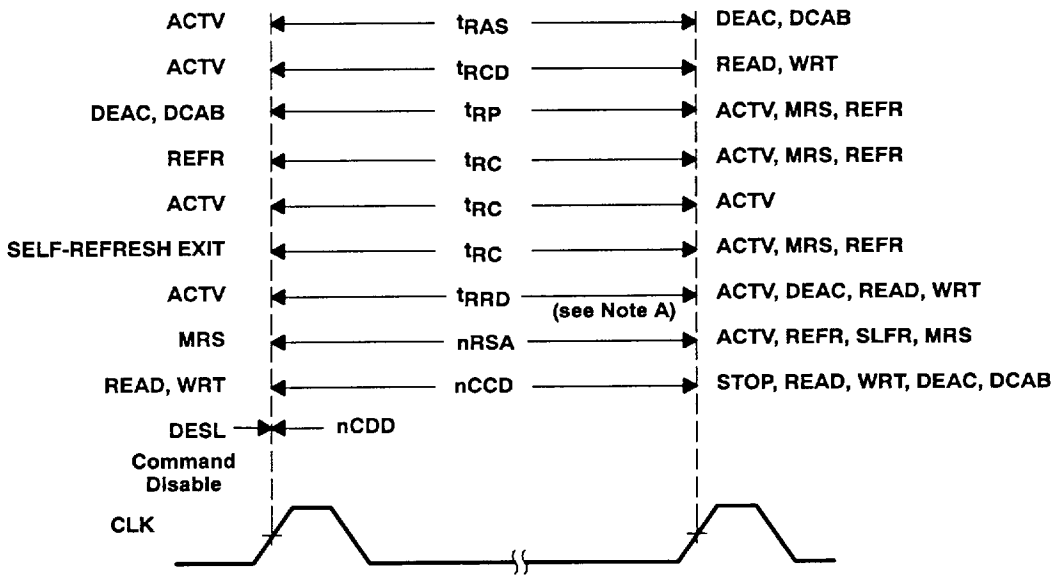


Figure 8. Output Parameters



NOTE A: t_{RRD} is specified for command execution in one bank to command execution in the other bank.

Figure 9. Command-to-Command Parameters

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

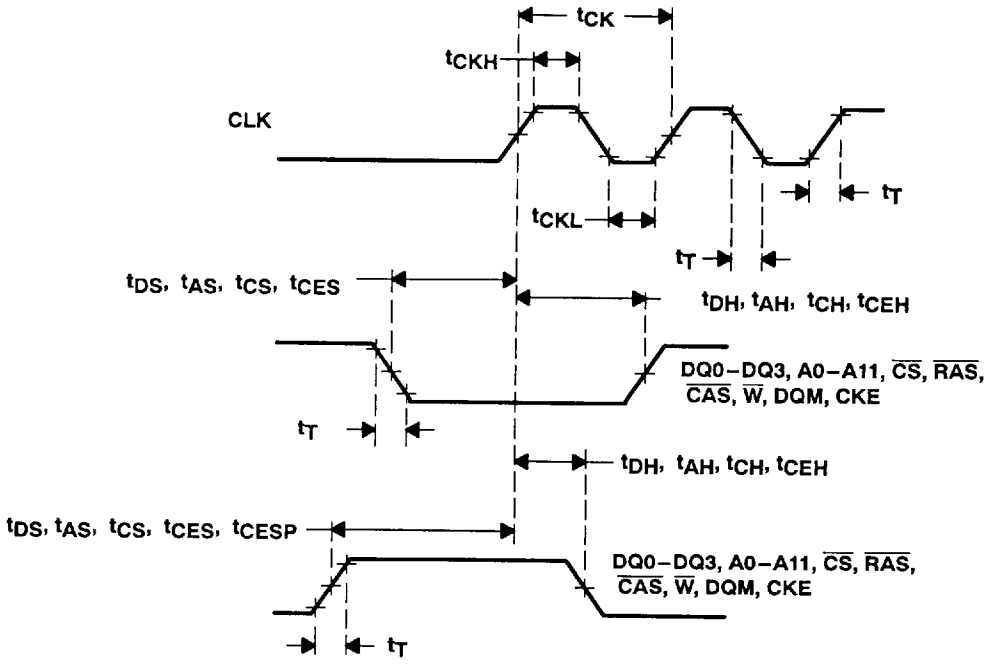
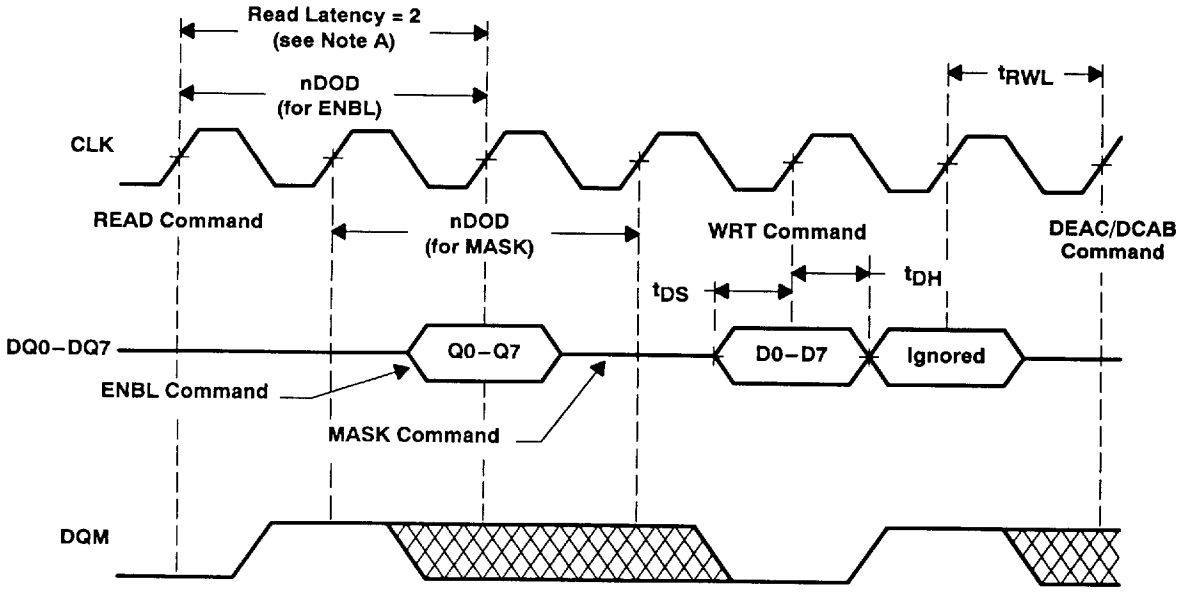


Figure 10. Input Attribute Parameters

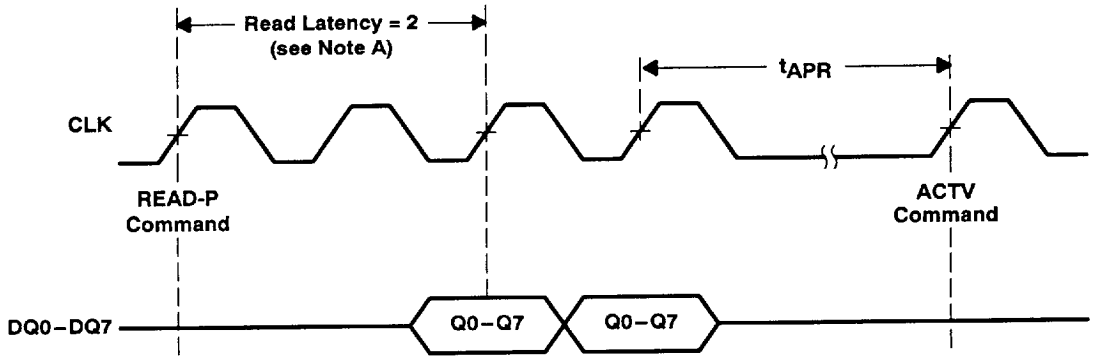


NOTE A: For purposes of this example, assume read latency = 2 and burst length = 2.

Figure 11. DQ Masking

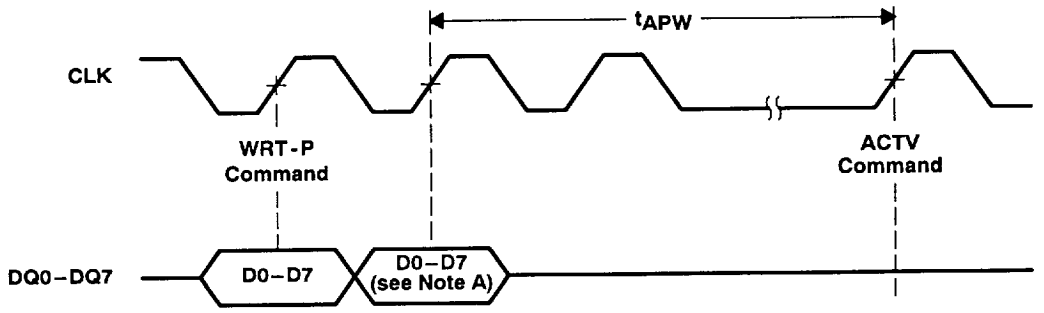
ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: For purposes of this example, assume read latency = 2 and burst length = 2.

Figure 12. Read Automatic Deactivate (Autoprecharge)



NOTE A: For purposes of this example, the burst length = 2.

Figure 13. Write Automatic Deactivate (Autoprecharge)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

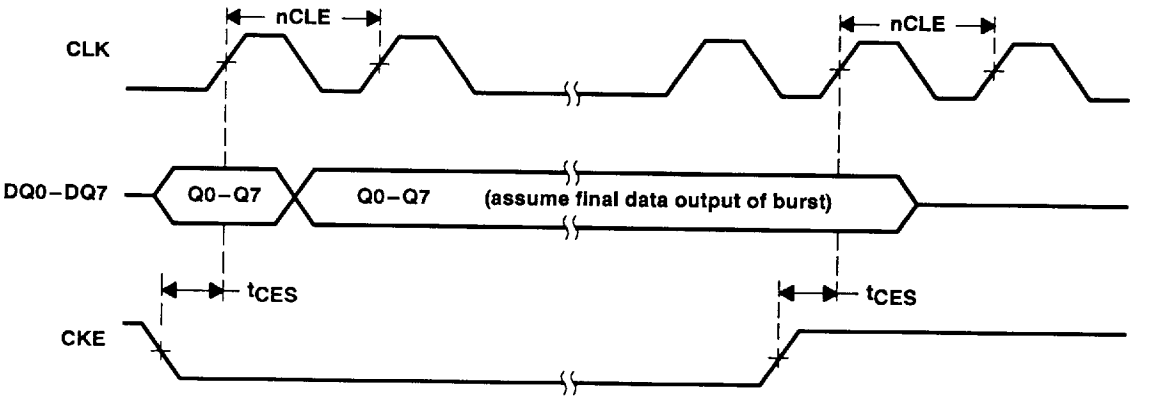


Figure 14. CLK Suspend Operation

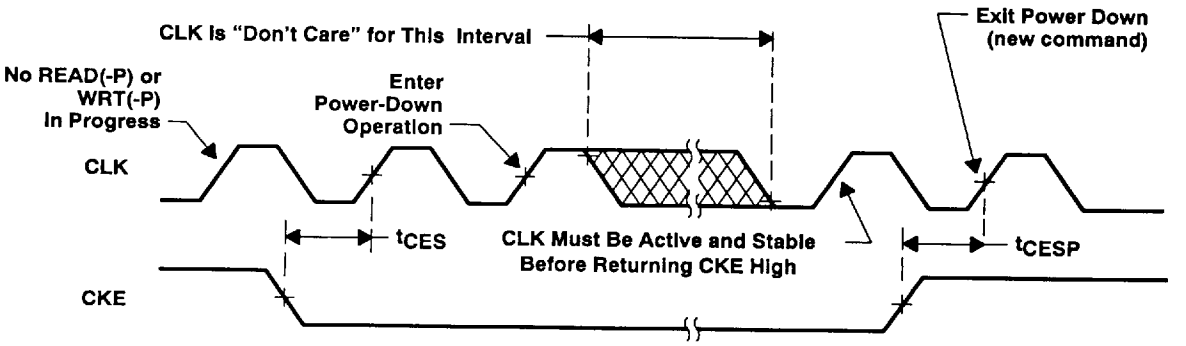
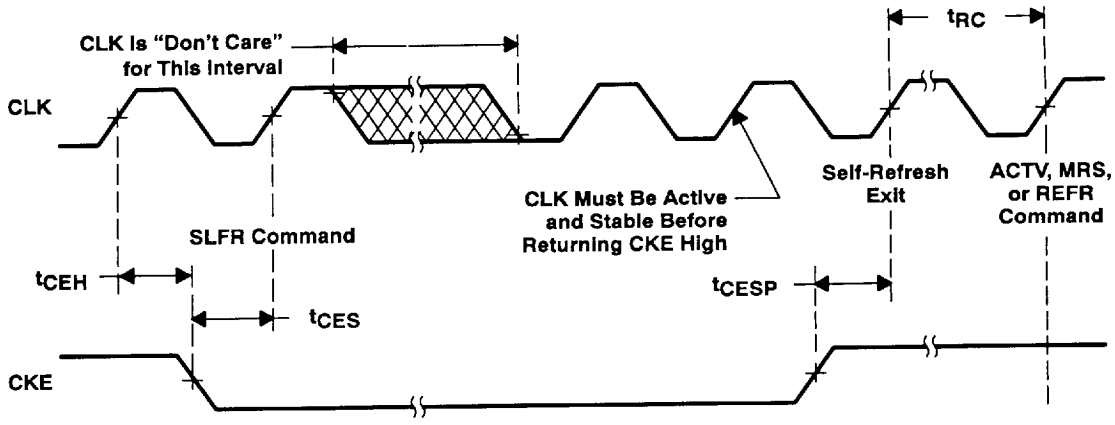


Figure 15. Power-Down Operation

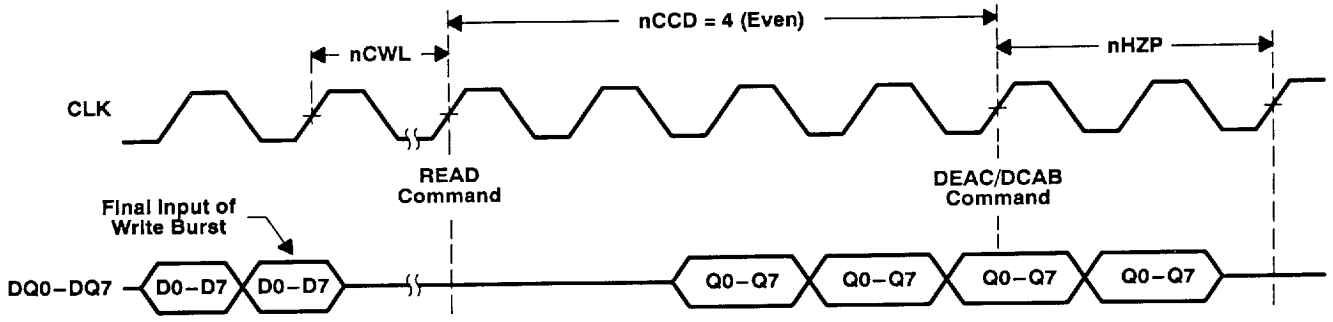
ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE: Assume both banks are previously deactivated.

Figure 16. Self-Refresh Entry/Exit

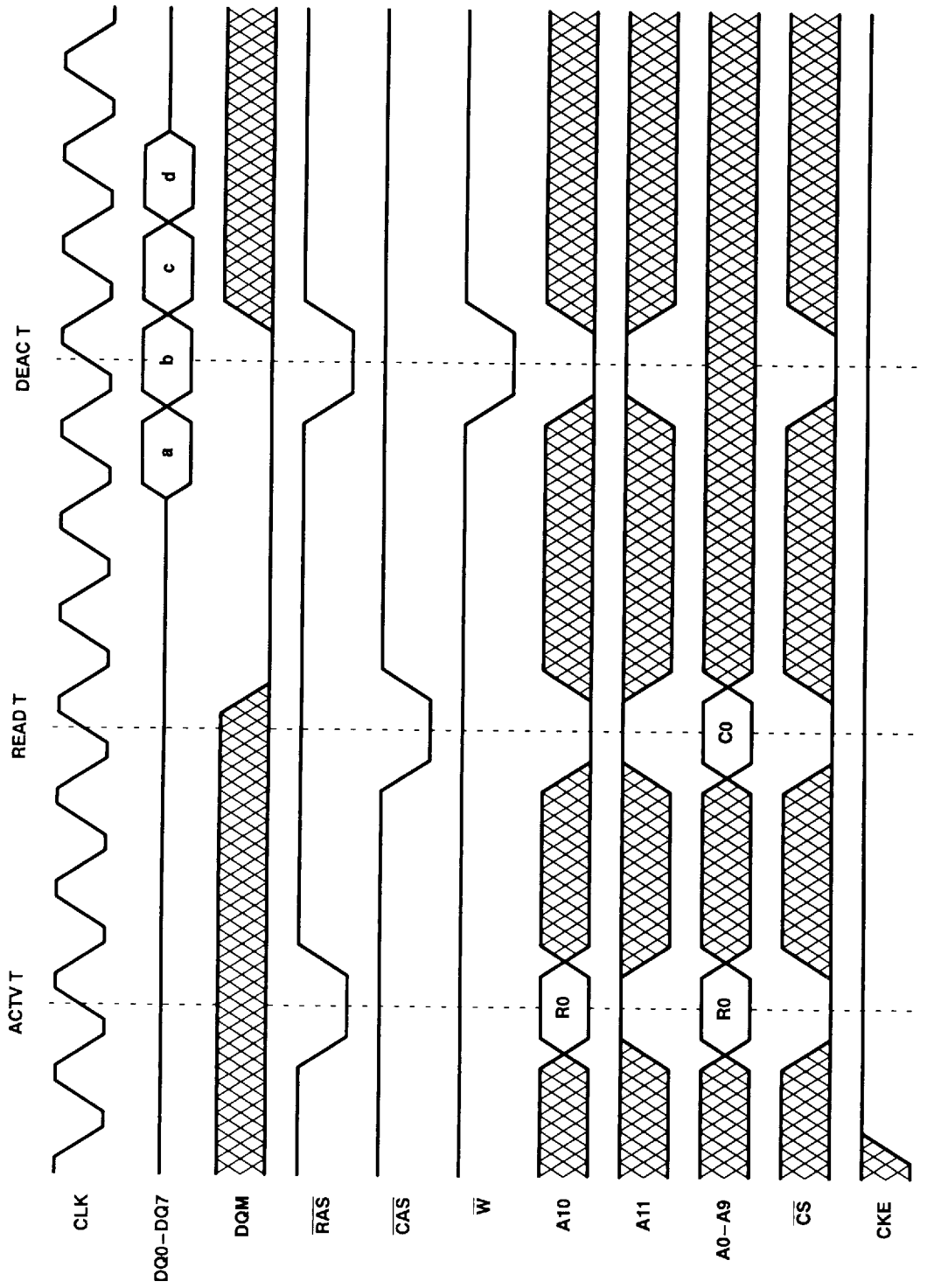


NOTE: Assume read latency = 2 and burst length = 8.

Figure 17. Write Burst Followed by DEAC/DCAB-Interrupted Read

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d
Q	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3

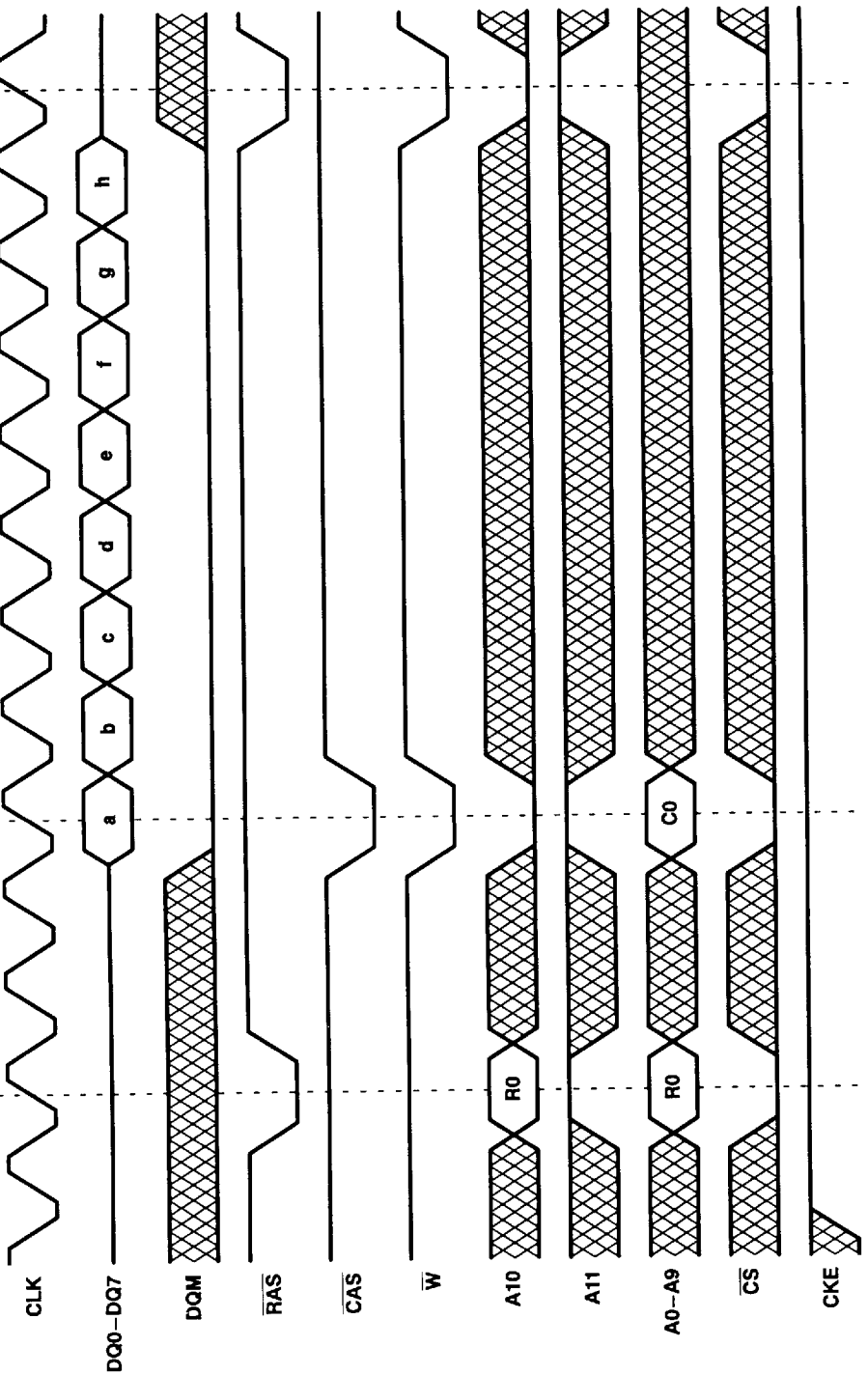
† Column address sequence depends on programmed burst type and C0 (see Table 5).

NOTE: This example illustrates minimum t_{RCD} and nEP for the '6x6802-10 at 100 MHz, the '6x6802-12 at 80 MHz, and the '6x6802-15 at 66 MHz.

Figure 18. Read Burst (read latency = 3, burst length = 4)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



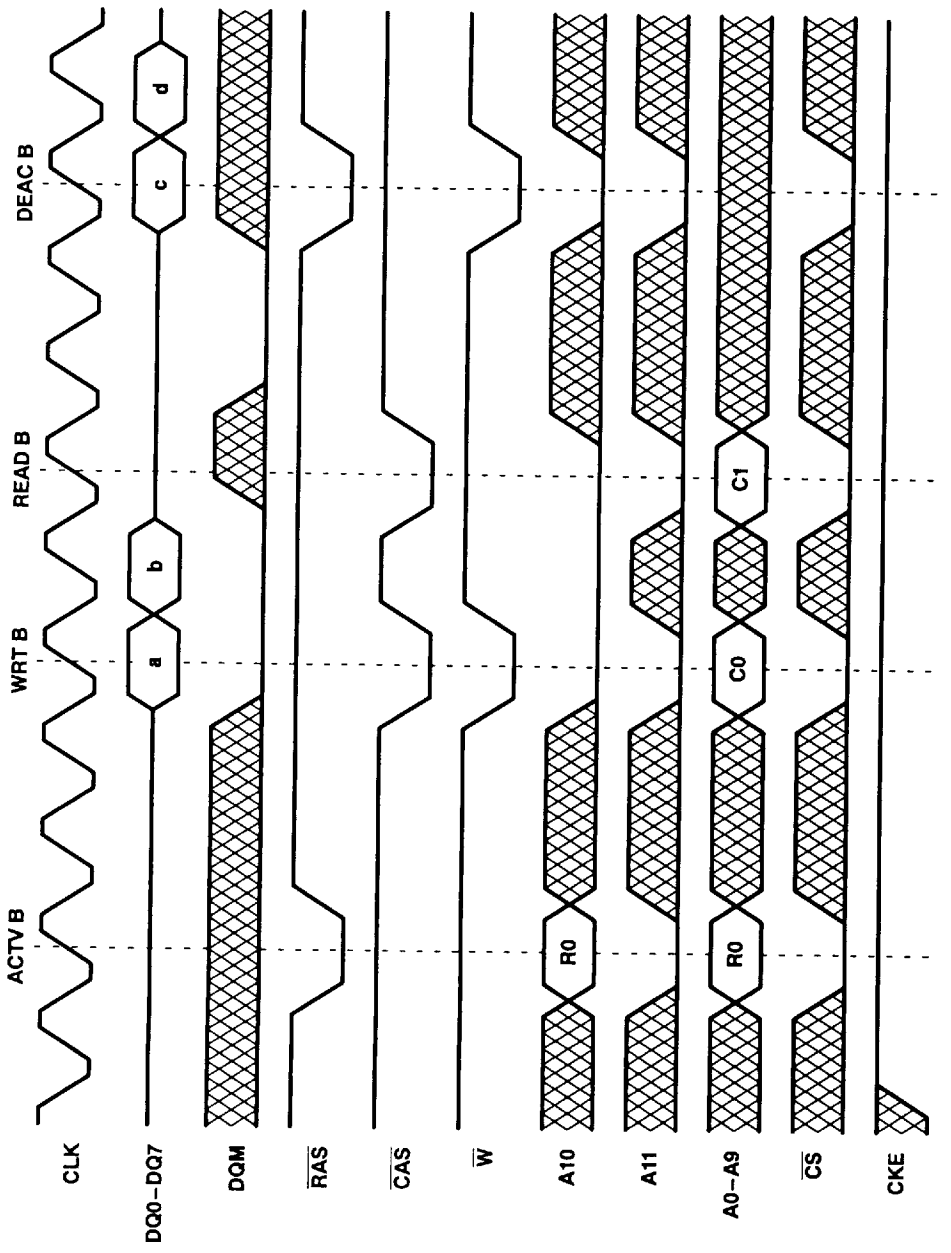
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
D	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3	C0 + 4	C0 + 5	C0 + 6	C0 + 7

† Column address sequence depends on programmed burst type and C0 (see Table 6).
NOTE: This example illustrates minimum t_{RCD} and t_{RWL} for the '6x6802-10 at 50 MHz, the '6x6802-12 at 50 MHz, and the '6x6802-15 at 33 MHz.

Figure 19. Write Burst (burst length = 8)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



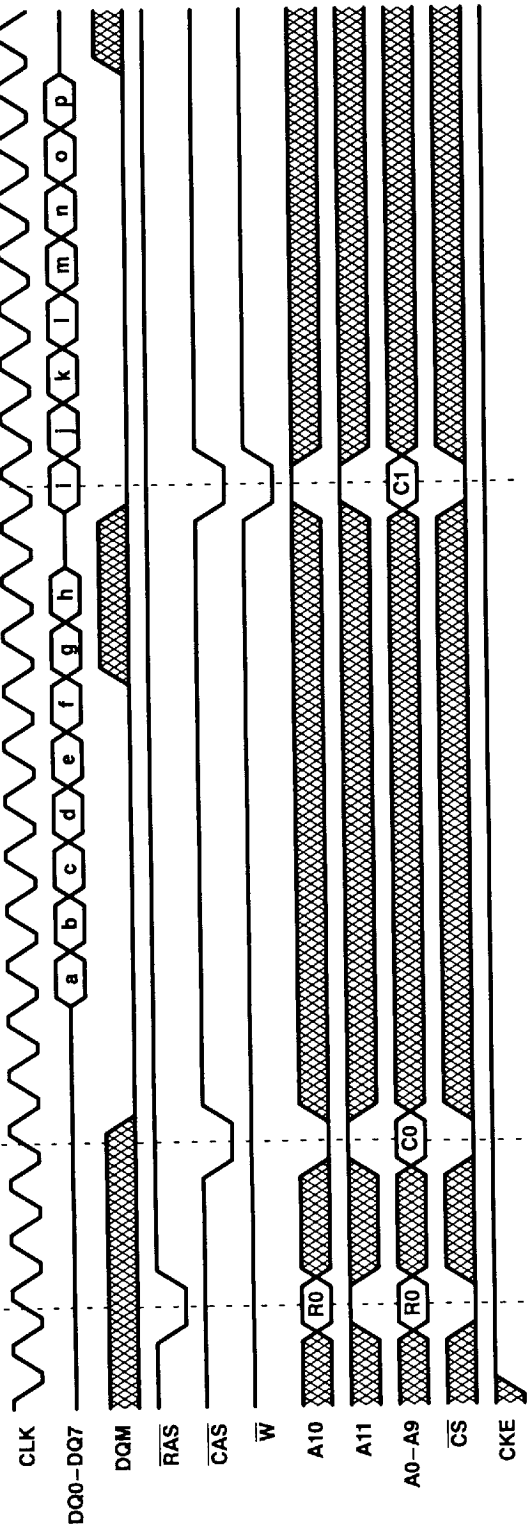
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d
D	B	R0	C0†	C0 + 1	C1‡	C1 + 1
Q	B	R0				

† Column address sequence depends on programmed burst type and C0 (see Table 4).
‡ Column address sequence depends on programmed burst type and C1 (see Table 4).
NOTE: This example illustrates minimum t_{RCD} for the '6x6802-10 at 100 MHz, the '6x6802-12 at 80 MHz, and the '6x6802-15 at 66 MHz.

Figure 20. Write-Read Burst (read latency = 3, burst length = 2)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



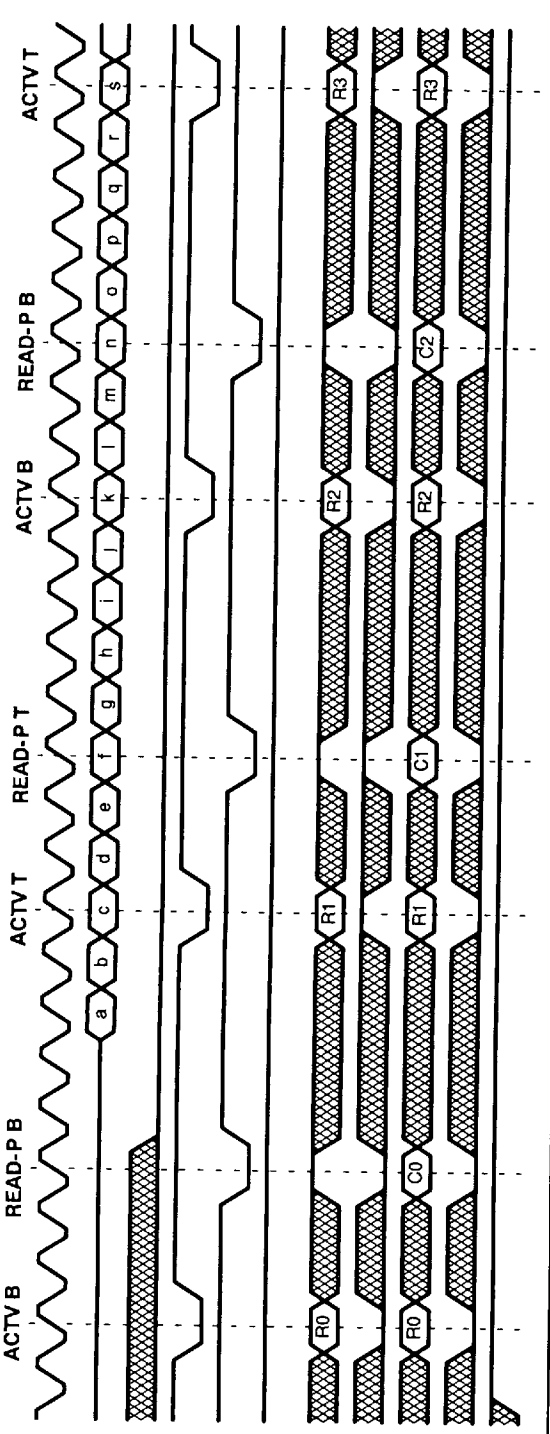
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7								
D	T	R0									C1‡	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7

† Column address sequence depends on programmed burst type and C0 (see Table 6).
‡ Column address sequence depends on programmed burst type and C1 (see Table 6).
NOTE: This example illustrates minimum t_{RCD} for the '6x6802-10 at 100 MHz, the '6x6802-12 at 80 MHz, and the '6x6802-15 at 66 MHz.

Figure 21. Read-Write Burst With Automatic Deactivate (read latency = 3, burst length = 8)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



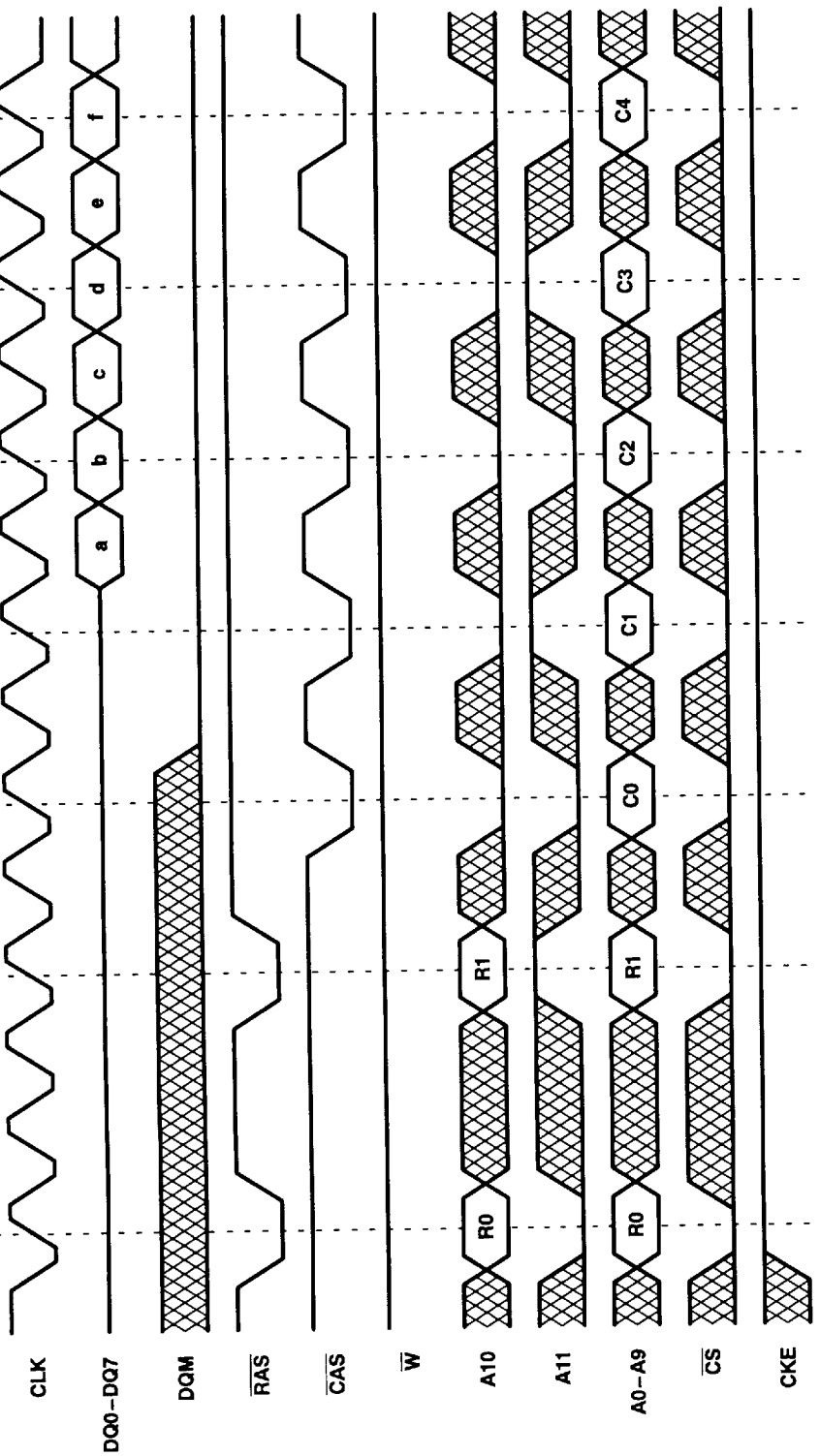
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	. . .
Q	B	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7												
Q	T	R1	C1‡	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7												
Q	B	R2	C2§	C2+1	C2+2	. . .																

† Column address sequence depends on programmed burst type and C0 (see Table 6).
‡ Column address sequence depends on programmed burst type and C1 (see Table 6).
§ Column address sequence depends on programmed burst type and C2 (see Table 6).
NOTE: This example illustrates minimum t_{RCD} for the '6x6802-10 at 100 MHz, the '6x6802-12 at 80 MHz, and the '6x6802-15 at 66 MHz.

Figure 22. Two-Bank Row Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



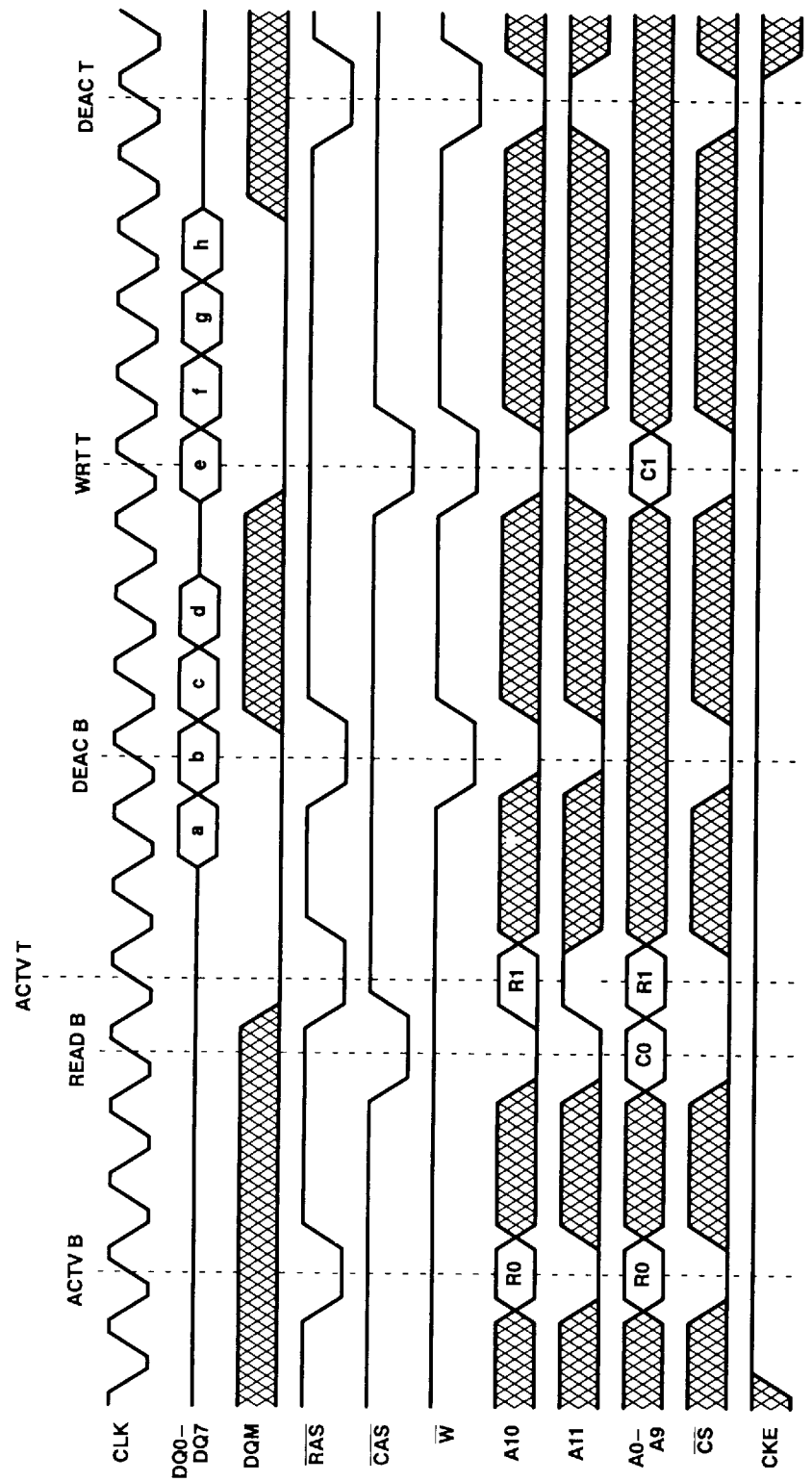
BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	...	...
Q	B	R0	C0†	C0 + 1	C1‡	C1 + 1	C2§	C2 + 1	...	...
Q	T	R1								
Q	B	R0								
.	.	.								

† Column address sequence depends on programmed burst type and C0 (see Table 4).
‡ Column address sequence depends on programmed burst type and C1 (see Table 4).
§ Column address sequence depends on programmed burst type and C2 (see Table 4).

Figure 23. Two-Bank Column Interleaving Read Bursts (read latency = 3, burst length = 2)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	B	R0	C0†	C0 + 1	C0 + 2	C0 + 3				
D	T	R1					C1‡	C1 + 1	C1 + 2	C1 + 3

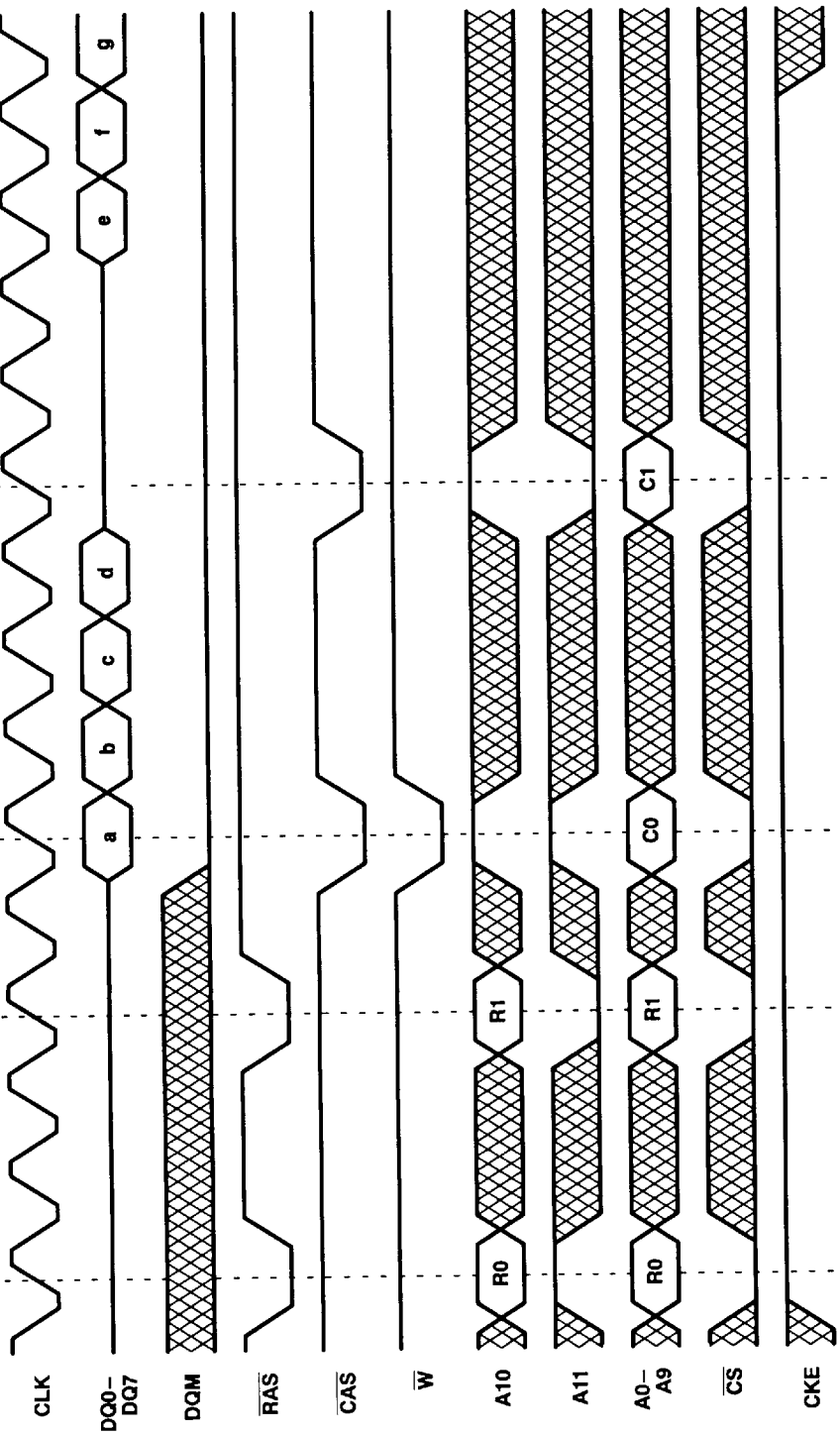
† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 5.)

NOTE: This example illustrates a minimum t_{RCD} and nEP read burst, and a minimum t_{RWL} write burst for the '6x6802-10 at 100 MHz, the '6x6802-12 at 80 MHz, and the '6x6802-15 at 66 MHz.

Figure 24. Read-Burst Bank B, Write-Burst Bank T (read latency = 3, burst length = 4)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



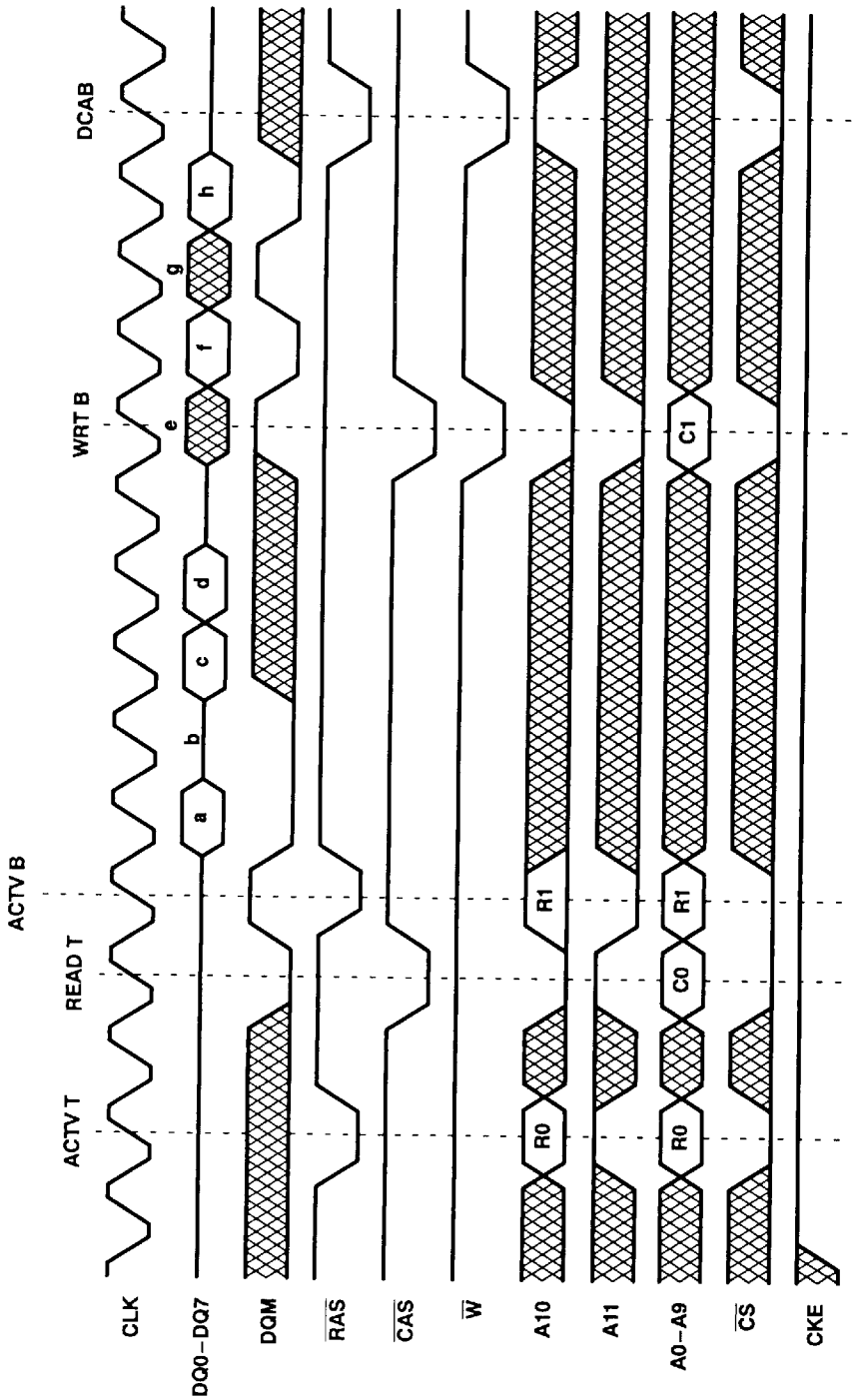
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
D	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3				
Q	B	R1					C1‡	C1 + 1	C1 + 2	C1 + 3

† Column address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column address sequence depends on programmed burst type and C1 (see Table 5).
NOTE: This example illustrates minimum nCWL for the '6x6802-10 at 100 MHz, the '6x6802-12 at 80 MHz, and the '6x6802-15 at 66 MHz.

Figure 25. Write-Burst Bank T, Read-Burst Bank B With Automatic Deactivate (read latency = 3, burst length = 4)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3				
D	B	R1					C1‡	C1+1	C1+2	C1+3

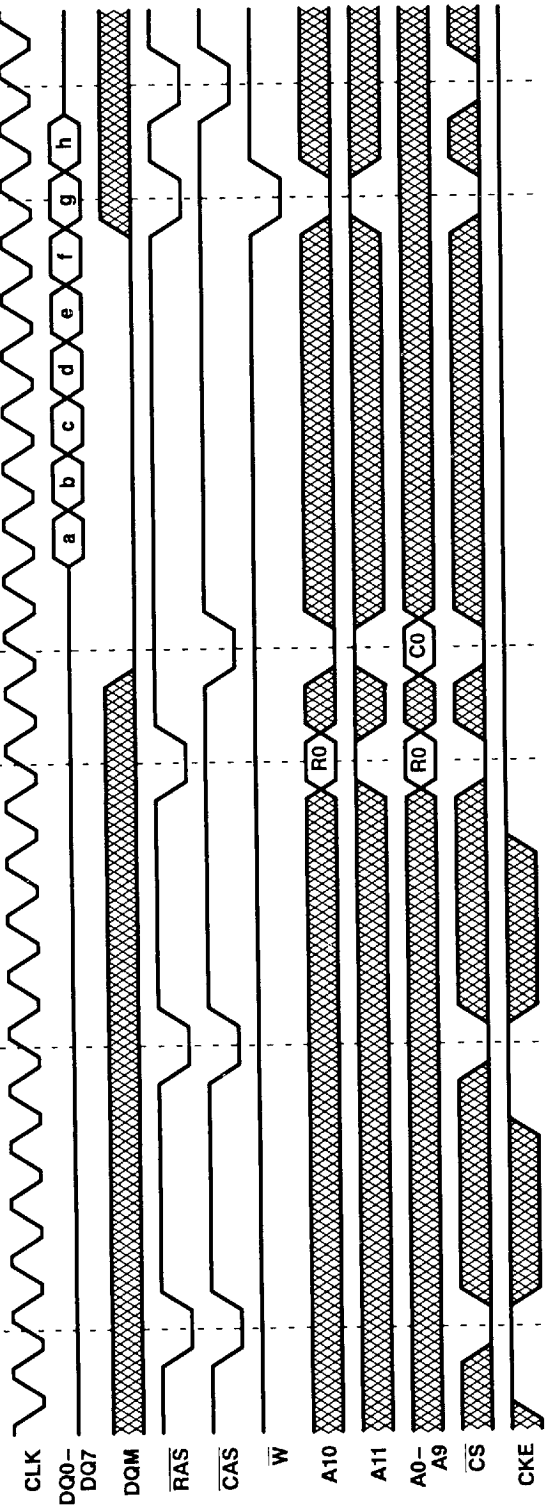
† Column address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column address sequence depends on programmed burst type and C1 (see Table 5).

NOTE: This example illustrates a minimum t_{RCD} read burst and minimum t_{RWL} write burst for the '6x6802-10 at 50 MHz, the '6x6802-12 at 50 MHz, and the '6x6802-15 at 33 MHz.

Figure 26. Use of DQM for Output and Data-In Cycle Masking (read-burst bank T, write-burst bank B, deactivate all banks) (read latency = 2, burst length = 4)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7

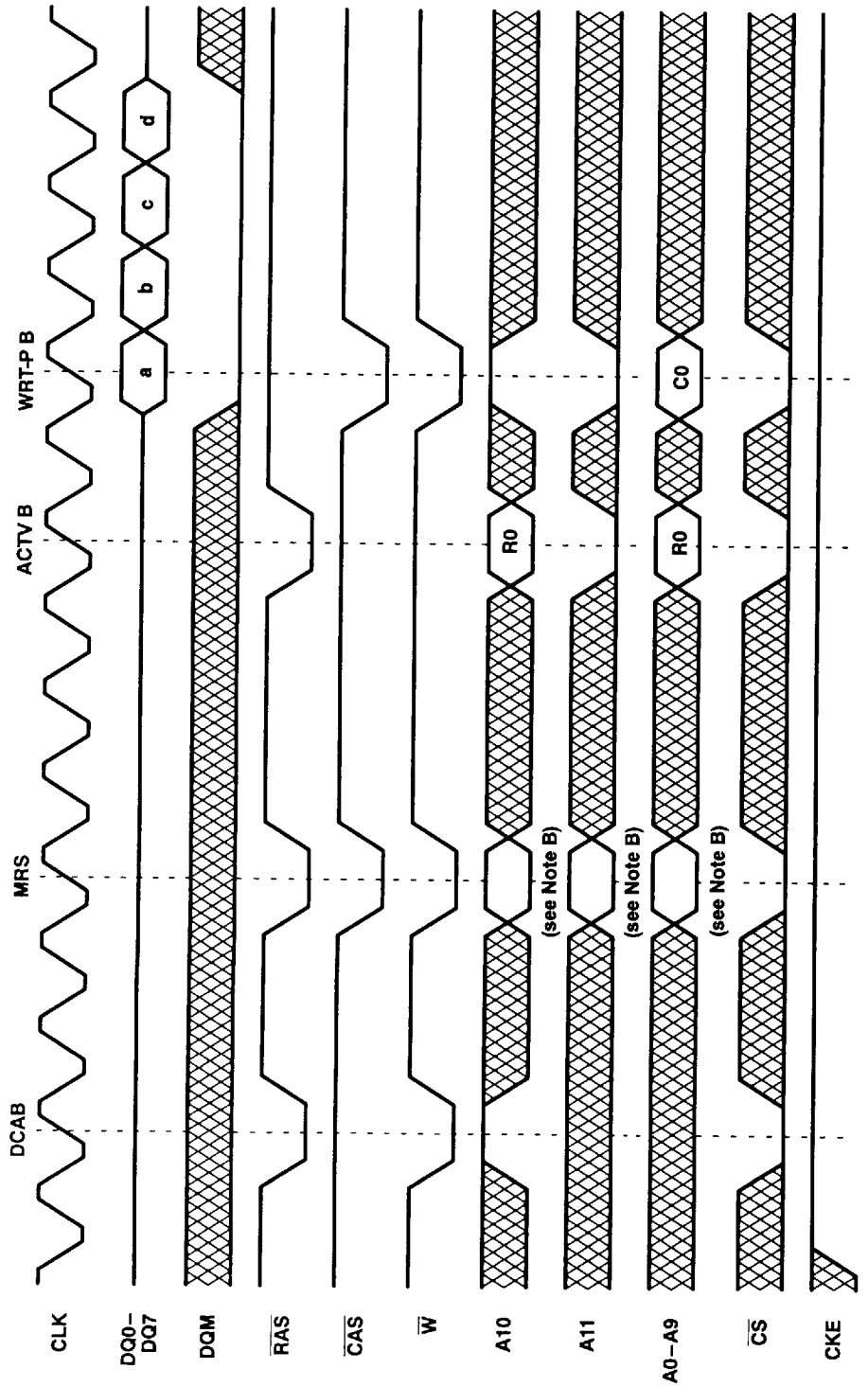
† Column address sequence depends on programmed burst type and C0 (see Table 6).

NOTE: This example illustrates minimum t_{RC}, t_{RCD}, nEP, and t_{RP} for the '6x6802-10 at 50 MHz, the '6x6802-12 at 33 MHz, and the '6x6802-15 at 33 MHz.

Figure 27. Refresh Cycles (refreshes followed by read burst followed by refresh)
(read latency = 2, burst length = 8)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



BURST TYPE	BANK	ROW	BURST CYCLE			
(D/Q)	(B/T)	ADDR	a	b	c	d
D	B	R0	C0†	C0+1	C0+2	C0+3

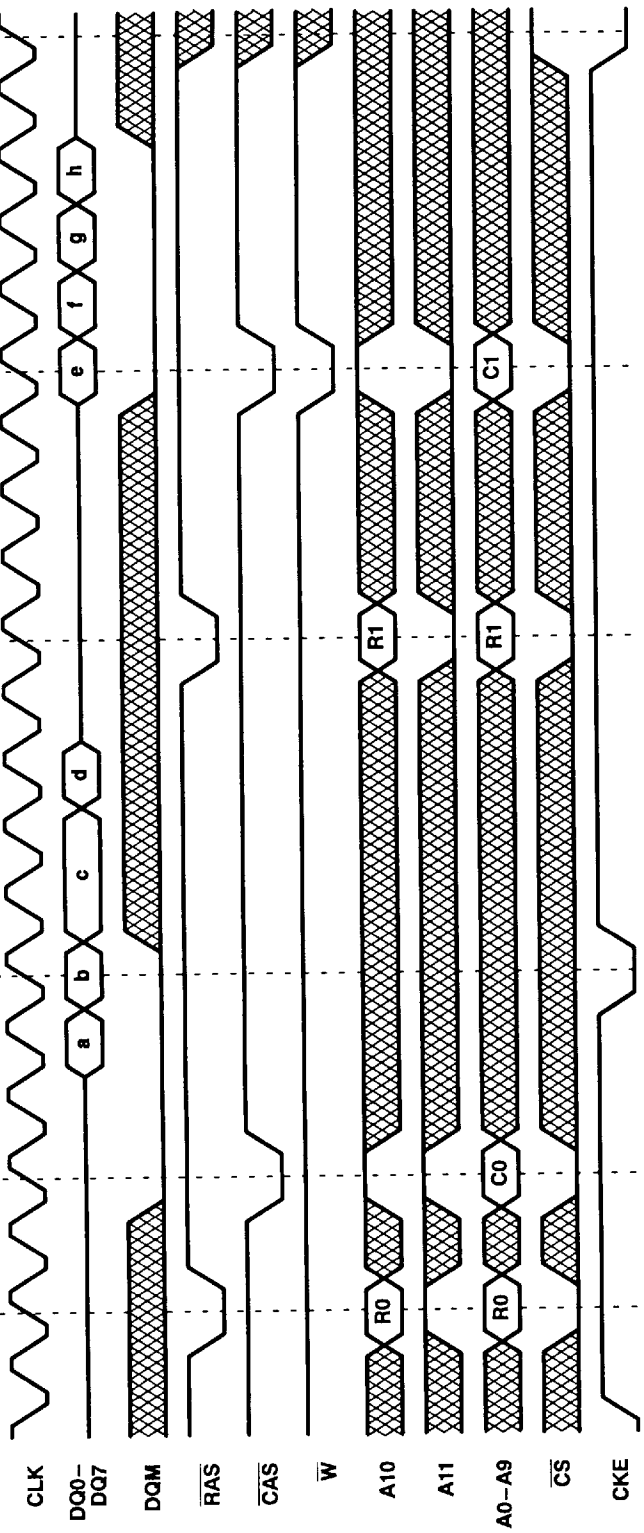
† Column address sequence depends on programmed burst type and C0 (see Table 5).

NOTES: A. This example illustrates minimum t_{RCD} for the '6x6802-10 at 66 MHz, the '6x6802-12 at 50 MHz, and the '6x6802-15 at 50 MHz.
B. Refer to Figure 1.

**Figure 28. Mode Register Programming (deactivate all, mode program, write burst with automatic deactivate)
(read latency = 2, burst length = 4)**

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3				
D	B	R1					C1‡	C1+1	C1+2	C1+3

† Column address sequence depends on programmed burst type and C0 (see Table 5).
‡ Column address sequence depends on programmed burst type and C1 (see Table 5).

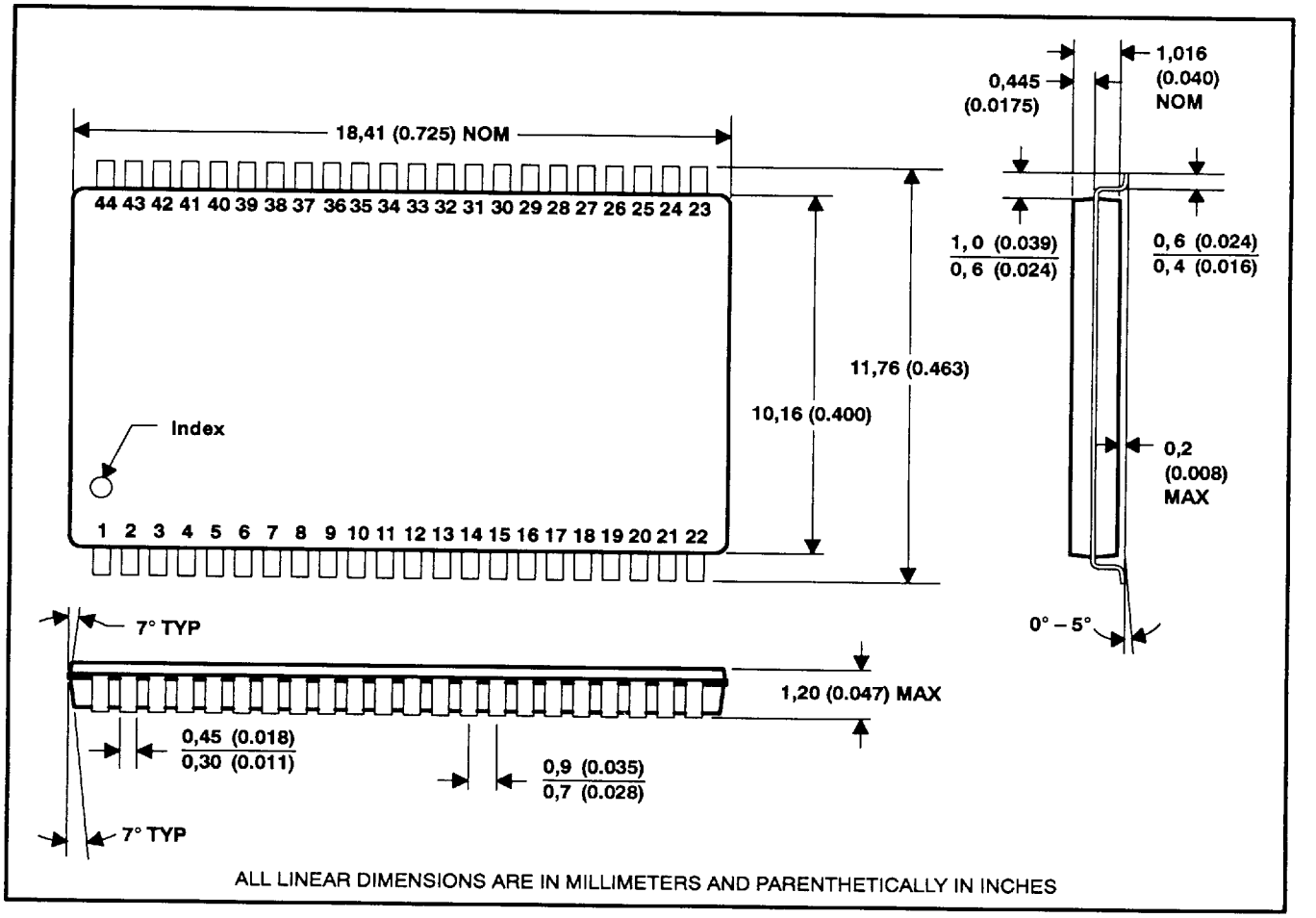
NOTE: This example illustrates minimum t_{RCD} for the '6x6802-10 at 66 MHz, the '6x6802-12 at 50 MHz, and the '6x6802-15 at 50 MHz.

Figure 29. Use of CKE for Clock Gating (hold) and Standby Mode (read-burst bank T with hold, write-burst bank B, standby mode) (read latency = 2, burst length = 4)

ADVANCE INFORMATION

MECHANICAL DATA

44-lead thin small-outline package (DGE suffix)



ADVANCE INFORMATION

device symbolization