FUJITSU MICROELECTRONICS
DATA SHEET

DS05-11464-1E

MEMORY Consumer FCRAM™
CMOS

512M Bit (4 bank x 2M word x 64 bit)
Consumer Applications Specific Memory for SiP

MB81EDS516445

■ DESCRIPTION

The Fujitsu MB81EDS516445 is a CMOS Fast Cycle Random Access Memory (FCRAM*) with Low Power Double Data Rate (LPDDR) SDRAM Interface containing 536,870,912 storages accessible in a 64-bit format. MB81EDS516445 is suited for consumer application requiring high data band width with low power consumption.

* : FCRAM is a trademark of Fujitsu Microelectronics Limited, Japan

■ FEATURES

- 2 M word × 64 bit × 4 banks organization
- DDR Burst Read/Write Access Capability
  -t_{CK} = 4.6 ns Min / 216 MHz Max (Tj ≤ + 105 °C)
  -t_{CK} = 5 ns Min / 200 MHz Max (Tj ≤ + 125 °C)
- Low Voltage Power Supply: $V_{DD} = V_{DDQ}$ + 1.7 V to + 1.9 V
- Junction Temperature: T_J = − 10 °C to + 125 °C
- 1.8 V-CMOS compatible inputs
- Burst Length: 2, 4, 8, 16
- CAS latency: 2, 3, 4
- Clock Stop capability during idle periods
- Auto Precharge option for each burst access
- Configurable Driver Strength and Pre Driver Strength
- Auto Refresh and Self Refresh Modes
- Deep Power Down Mode
- Low Power Consumption
  -I_{DD4R} =300 mA Max @ 3.46 GByte/s
  -I_{DD4W} =380 mA Max @ 3.46 GByte/s
- 8 K refresh cycles / 4 ms (Tj ≤+125 °C)

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■ PIN DESCRIPTIONS

Symbol	Type	Function		
CK, $\overline{CK}$	Input	Clock		
CKE	Input	Clock Enable		
$\overline{CS}$	Input	Chip Select		
$\overline{RAS}$	Input	Row Address Strobe		
$\overline{CAS}$	Input	Column Address Strobe		
$\overline{WE}$	Input	Write Enable		
BA[1:0]	Input	Bank Address Inputs		
A[12:0]	Input	Address Inputs	Row	A0 to A12
			Column	A0 to A7
AP(A10)	Input	Auto Precharge Enable		
DM[7:0] *1	Input	Input Data Mask Enable		
DQ[63:0] *1, *2	I/O	Data Bus Input / Output		
DQS[7:0] *2	I/O	Data Strobe		
V_{DDQ}, V_{DD}	Supply	Power Supply		
V_{SSQ}, V_{SS}	Supply	Ground		

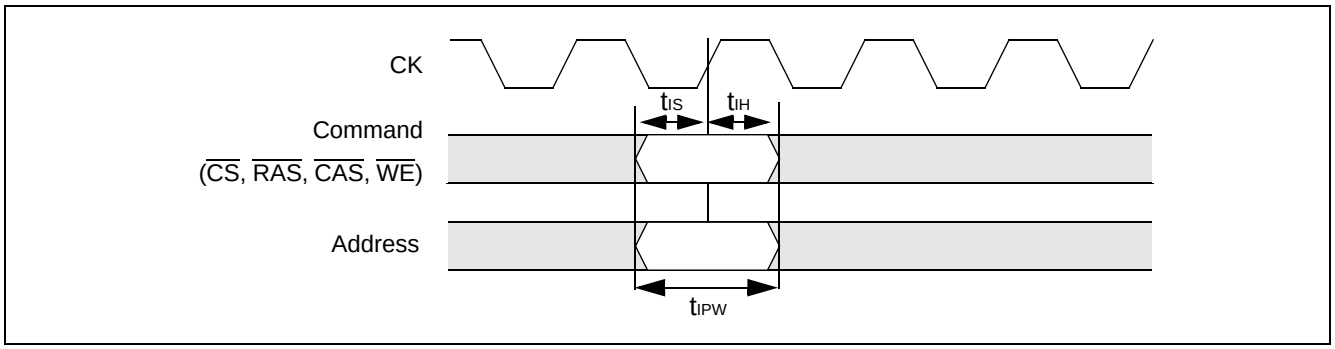
*1 : DM0, DM1, DM2, DM3, DM4, DM5, DM6 and DM7 correspond to DQ[7:0], DQ[15:8], DQ[23:16], DQ[31:24], DQ[39:32], DQ[47:40], DQ[55:48] and DQ[63:56].

*2 : DQS0, DQS1, DQS2, DQS3, DQS4, DQS5, DQS6 and DQS7 correspond to DQ[7:0], DQ[15:8], DQ[23:16], DQ[31:24], DQ[39:32], DQ[47:40], DQ[55:48] and DQ[63:56].

6. Address Inputs (A0 to A12)

Address input selects an arbitrary location of a total of 2,097,152 words of each memory cell matrix. Total 21 address input signals are required to decode such a matrix. Row Address (RA) is input from A0 to A12 and Column Address (CA) is input from A0 to A7. Row addresses are latched with ACTIVE (ACT) command, and Column addresses and Auto Precharge (AP) bit are latched with Read (READ or READA) or Write command (WRIT or WRITA).

• Command and address inputs setup and hold time



7. Input Data Mask (DM0 to DM7)

DM is an input mask signal for write data. Input data is masked when DM is sampled High on the both edges of DQS along with input data. DM0, DM1, DM2, DM3, DM4, DM5, DM6 and DM7 correspond to DQ[7:0], DQ[15:8], DQ[23:16], DQ[31:24], DQ[39:32], DQ[47:40], DQ[55:48] and DQ[63:56] respectively. Refer to the “DQ/DQS/DM Correspondence Table”.

8. Data Bus Input / Output (DQ0 to DQ63)

DQ is data bus input / output signal.

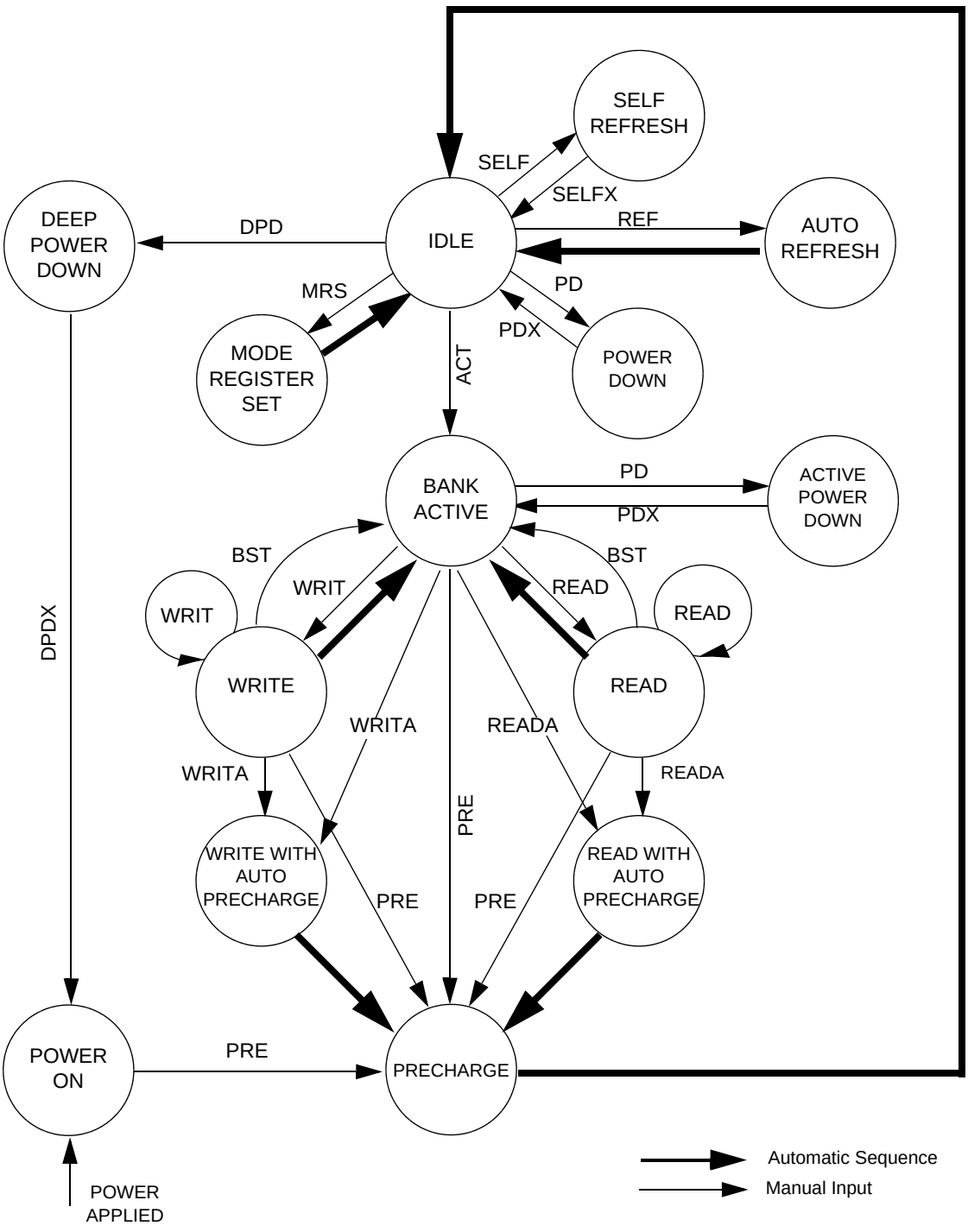
9. Data Strobe (DQS0 to DQS7)

DQS is edge aligned with output read data and center aligned with input write data. DQS0, DQS1, DQS2, DQS3, DQS4, DQS5, DQS6 and DQS7 correspond to DQ[7:0], DQ[15:8], DQ[23:16], DQ[31:24], DQ[39:32], DQ[47:40], DQ[55:48] and DQ[63:56] respectively. Refer to the “DQ/DQS/DM Correspondence Table”.

• DQ/DQS/DM Correspondence Table

DQ	DQS	DM
DQ[7:0]	DQS0	DM0
DQ[15:8]	DQS1	DM1
DQ[23:16]	DQS2	DM2
DQ[31:24]	DQS3	DM3
DQ[39:32]	DQS4	DM4
DQ[47:40]	DQS5	DM5
DQ[55:48]	DQS6	DM6
DQ[63:56]	DQS7	DM7

■ SIMPLIFIED STATE DIAGRAM



Note: "■SIMPLIFIED STATE DIAGRAM" is based on the single bank operation.
State transition of multi bank operation are not described in all detail.

Mode Register Table

Mode Register

BA_1	BA_0	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0	0	0	0	0	0	0	0	CL			0	BL			Mode Register

A_6	A_5	A_4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Extended Mode Register

BA_1	BA_0	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0	1	0	0	0	0	0	0	PDS	DS	0	0	0	0	0	Extended Mode Register

A_6	Pre Driver Strength
0	Fast
1	Slow

A_5	Driver Strength
0	Normal
1	Weak

3. Burst Length (BL)

Burst Length (BL) is the number of word to be read or write as the result of a single READ or WRITE command. It can be set on 2, 4, 8, 16 words boundary through Mode Register. The burst type is sequential that is incremental decoding scheme within a boundary address to be determined by burst length. Device internal address counter assigns +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (= 0).

Burst Length	Starting Column Address				Burst Address Sequence (Hexadecimal)
	A_3	A_2	A_1	A_0	
2	X	X	X	0	0 - 1
	X	X	X	1	1 - 0
4	X	X	0	0	0 - 1 - 2 - 3
	X	X	0	1	1 - 2 - 3 - 0
	X	X	1	0	2 - 3 - 0 - 1
	X	X	1	1	3 - 0 - 1 - 2
8	X	0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
	X	0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0
	X	0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1
	X	0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2
	X	1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
	X	1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4
	X	1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5
	X	1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E

4. CAS Latency (CL)

CAS Latency (CL) is the delay between READ command being registered and first read data becoming available during read operation. First read data will be valid after (CL-1) $\times$ t_{CK} + t_{AC} from the CK rising edge where Read command being latched.

5. Driver Strength (DS)

Driver Strength (DS) is to adjust the driver strength of data output.

6. Pre Driver Strength (PDS)

Pre Driver Strength (PDS) is to adjust the transition time of the data output without changing the output driver impedance.

■ COMMAND TRUTH TABLE

1) Basic Command Truth Table

Command	Symbol	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10 (AP)	A[9:0], A11, A12
DESELECT *1	DESL	H	X	X	X	X	X	X
NO OPERATION *1	NOP	L	H	H	H	X	X	X
BURST TERMINATE *2, *3	BST	L	H	H	L	X	X	X
READ *3, *4	READ	L	H	L	H	V	L	CA
READ with Auto-precharge *3, *4	READA	L	H	L	H	V	H	CA
WRITE *3, *4	WRIT	L	H	L	L	V	L	CA
WRITE with Auto-precharge *3, *4	WRITA	L	H	L	L	V	H	CA
BANK ACTIVE *4, *5	ACT	L	L	H	H	V	RA	
PRECHARGE SINGLE BANK *5, *6	PRE	L	L	H	L	V	L	X
PRECHARGE ALL BANKS *5, *6	PALL	L	L	H	L	X	H	X
AUTO REFRESH *6	REF	L	L	L	H	X	X	X
MODE REGISTER SET *7	MRS	L	L	L	L	V	V	V

Note: V = Valid, L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, RA = Row Address, CA = Column Address
All commands are assumed to be valid state transitions and latched on the rising edge of CK. CKE assume to be kept High.

*1: NOP and DESL commands have the same functionality. Unless specifically noted, NOP will represent both NOP and DESL command in later description.

*2: When the current state is IDLE and CKE=L, BST command will represent DPD command. Refer to the “■CKE COMMAND TRUTH TABLE”.

*3: BST command can be applied to READ or WRIT. READA and WRITA must not be terminated by BST command.

*4: READ, READA, WRIT and WRITA commands can be issued after the corresponding bank has been activated by ACT commands. Refer to the “■SIMPLIFIED STATE DIAGRAM”.

*5: ACT command can be issued after corresponding bank has been precharged by PRE or PALL command. Refer to the “■ SIMPLIFIED STATE DIAGRAM”.

*6: REF command can be issued after all banks have been precharged by PRE or PALL command. Refer to the “■SIMPLIFIED STATE DIAGRAM”.

*7: MRS command can be issued after all banks have been precharged and all DQ are in High-Z. Mode Register and Extended Mode Register are selected through BA input. Mode Register and Extended Mode Register must be set by MRS command after power up.

2) CKE Command Truth Table

Command	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A[12:0]
		n-1	n						
SELF REFRESH ENTRY *1	SELF	H	L	L	L	L	H	X	X
SELF REFRESH EXIT *2	SELFX	L	H	L	H	H	H	X	X
				H	X	X	X	X	X
POWER DOWN ENTRY *1	PD	H	L	L	H	H	H	X	X
				H	X	X	X	X	X
POWER DOWN EXIT	PDX	L	H	L	H	H	H	X	X
				H	X	X	X	X	X
DEEP POWER DOWN ENTRY *1	DPD	H	L	L	H	H	L	X	X
DEEP POWER DOWN EXIT	DPDX	L	H	L	H	H	H	X	X
				H	X	X	X	X	X

Note: V = Valid, L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}

*1: SELF and DPD commands can be issued after all banks have been precharged and all DQ are in High-Z.

*2: CKE should be held High more than t_{REFC} period after SELFX.

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
READ	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst Terminate → BANK ACTIVE
	L	H	L	H	BA, CA, AP	READ/READA	Interrupt burst read by new burst read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal
	L	L	H	H	BA, RA	ACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL	Terminate burst read by precharge → IDLE
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	
WRITE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst terminate → BANK ACTIVE
	L	H	L	H	BA, CA, AP	READ/READA	Interrupt burst write by new burst read; Determine AP *5
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Interrupt burst write by new burst write; Determine AP
	L	L	H	H	BA, RA	ACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
READ WITH AUTO PRECHARGE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	
WRITE WITH AUTO PRE-CHARGE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Write Recovering	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Start Write; Determine AP
	L	L	H	H	BA, RA	ACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	
Precharging	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT	
	L	L	H	L	BA, AP	PRE/PALL	NOP *2
	L	L	L	H	X	REF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

■ BANK OPERATION COMMAND TABLE

Minimum clock latency or delay time for single bank operation

1st Command	2nd Command (same bank)										
	MRS	ACT	READ	READA	WRIT	WRITA	BST	PRE	PALL	REF	SELF
MRS	t_{MRD}	t_{MRD}	—	—	—	—	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}
ACT	—	—	t_{RCD}	*4 t_{RCD}	t_{RCD}	*5 t_{RCD}	—	t_{RAS}	t_{RAS}	—	—
READ	—	—	1	1	*6 BL/2 +CL	*6 BL/2 +CL	1	*3 1	*3 1	—	—
READA	*1, *2 BL/2 + t_{RP}	BL/2 + t_{RP}	—	—	—	—	BL/2 + t_{RP}	BL/2 + t_{RP}	BL/2 + t_{RP}	*1 BL/2 + t_{RP}	*1, *2 BL/2 + t_{RP}
WRIT	—	—	*6 2 + t_{WTR}	*6 2 + t_{WTR}	1	1	1	*3 BL/2 + 1 + t_{WR}	*3 BL/2 + 1 + t_{WR}	—	—
WRITA	*1, *2 BL/2 + 1 + t_{DAL}	BL/2 + 1 + t_{DAL}	—	—	—	—	BL/2 +1 + t_{DAL}	BL/2 +1 + t_{DAL}	BL/2 +1 + t_{DAL}	*1 BL/2 +1 + t_{DAL}	*1, *2 BL/2 +1 + t_{DAL}
READ - BST	—	—	1	1	CL	CL	1	*3 1	*3 1	—	—
WRIT - BST	—	—	1 + t_{WTR}	1 + t_{WTR}	1	1		*3 1 + t_{WR}	*3 1 + t_{WR}	—	—
PRE	*1, *2 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	*1 t_{RP}	*1, *2 t_{RP}
PALL	*2 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	t_{RP}	*2 t_{RP}
REF	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
SELFX	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}

" - " : illegal

*1: Assume all banks are in IDLE state.

*2: Assume output is in High-Z state.

*3: Assume t_{RAS} (Min.) is satisfied.

*4: ACT to READA interval must be longer than t_{RAS} - BL/2.

*5: ACT to WRITA interval must be longer than t_{RAS} - (1 + BL/2 + t_{WR}).

*6: Assume appropriate DM masking.

Minimum clock latency or delay time for multi bank operation

		2nd Command (other bank)										
		MRS	**ACT**	**READ**	**READA**	**WRIT**	**WRITA**	**BST**	**PRE**	**PALL**	**REF**	**SELF**
1st Command	**MRS**	t_{MRD}	t_{MRD}	—	—	—	—	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}
	ACT	—	t_{RRD}	1	1	1	1	1	1	t_{RAS}	—	—
	READ	—	*1, *3 1	1	1	*5 BL/2 +CL	*5 BL/2 +CL	1	1	*4 1	—	—
	READA	*1, *2 BL/2 + t_{RP}	*1, *3 1	BL/2	BL/2	*5 BL/2 +CL	*5 BL/2 +CL	BL/2 + t_{RP}	1	*4 BL/2 + t_{RP}	*1 BL/2 + t_{RP}	*1 BL/2 + t_{RP}
	WRIT	—	*1, *3 1	*5 2 + t_{WTR}	*5 2 + t_{WTR}	1	1	1	1	*4 BL/2 + 1 + t_{WR}	—	—
	WRITA	*1 BL/2 + 1 + t_{DAL}	*1, *3 1	*5 BL/2 + 1 + t_{WTR}	*5 BL/2 + 1 + t_{WTR}	BL/2	BL/2	BL/2 +1 + t_{DAL}	1	*4 BL/2 + 1 + t_{DAL}	*1 BL/2 + 1 + t_{DAL}	*1 BL/2 + 1 + t_{DAL}
	READ - BST	—	*1, *3 1	1	1	CL	CL	1	1	*4 1	—	—
	WRIT - BST	—		1 + t_{WTR}	1 + t_{WTR}	1	1		1	*4 1 + t_{WR}	—	—
	PRE	*1, *2 t_{RP}	*1, *3 1	1	1	1	1	1	1	1	*1 t_{RP}	*1, *2 t_{RP}
	PALL	*1 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	t_{RP}	t_{RP}
	REF	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
	SELFX	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}

" - " : illegal

*1: Assume other bank is in IDLE state.

*2: Assume output is in High-Z state.

*3: Assume t_{RRD} is satisfied.

*4: Assume t_{RAS} is satisfied.

*5: Assume appropriate DM masking.

■ COMMAND DESCRIPTION

1. DESELECT (DESL)

When $\overline{CS}$ is High at the CK rising edge, all input signals are neglected. Internal operation such as burst cycle is held.

2. NO OPERATION (NOP)

NOP disables address and data input and internal operation such as burst cycle is held.

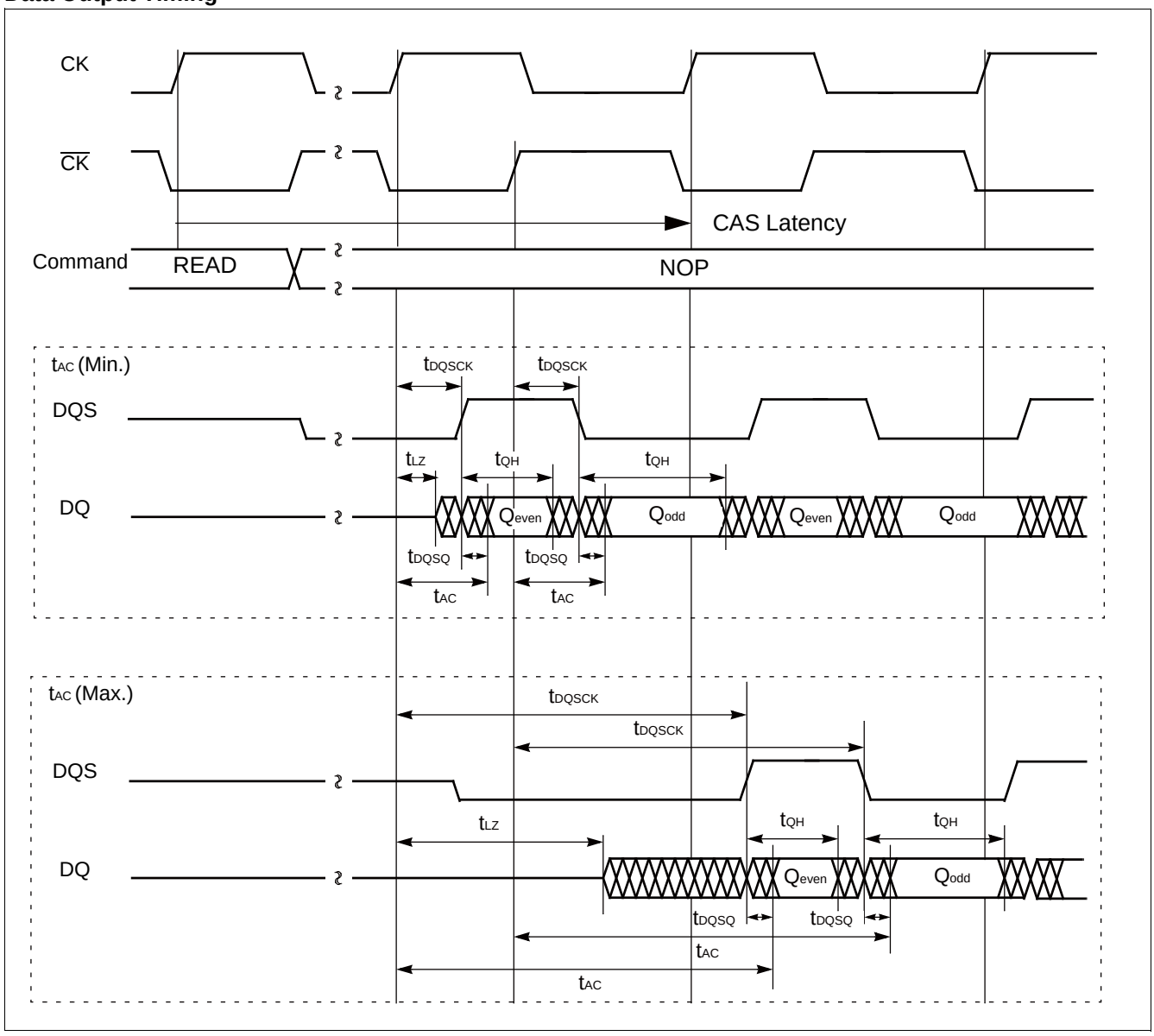
3. BANK ACTIVE (ACT)

ACT activates the bank selected by BA and latch the row address through A0 to A12.

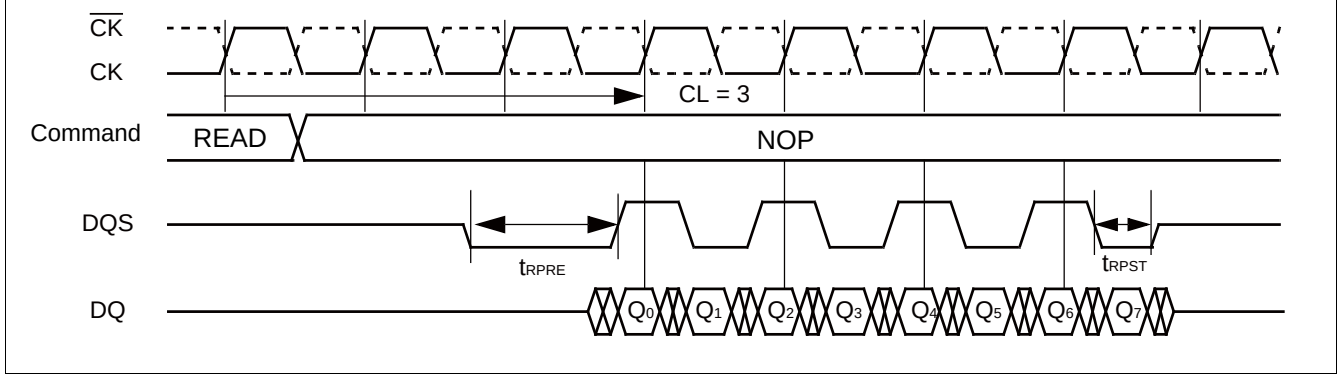
4. READ (READ)

READ initiates burst read operation to an activated row address. Address inputs of A[7:0] determine starting column address and A10 determines whether Auto Precharge is used or not. Initially DQS output Low level then start toggling together with data output with respect to CL and BL. The read data output is edge-aligned with first rising edge of DQS and successive read data output are edge-aligned to the successive edge of DQS. The CK drives the rising edge of DQS and Even data, and the $\overline{CK}$ drives the falling edge of DQS and Odd data.

Data Output Timing



Read Preamble and Postamble @CL = 3



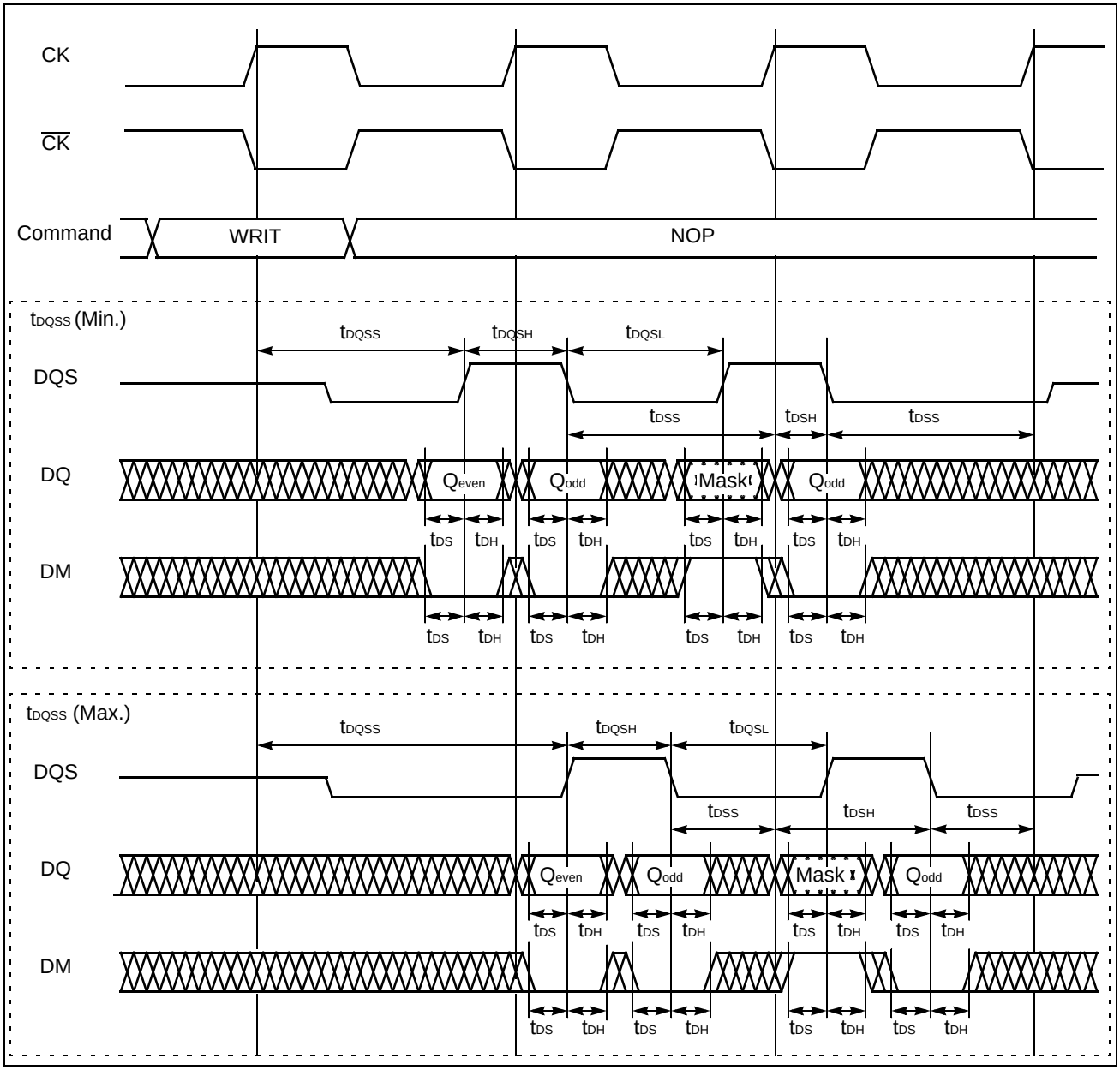
5. READ with Auto Precharge (READA)

READA commands can be issued by READ command with AP (A10) = H. Auto precharge is a feature which precharge the activated bank after the completion of burst read operation. The t_{RAS} is defined from between ACTIVE (ACT) command to the internal precharge which starts after BL/2 from READA command. READ with Auto precharge operation should not be interrupted by subsequent READ, READA, WRITE, WRITA commands. Next ACTIVE (ACT) command can be issued after BL/2 + t_{RP} after READA command.

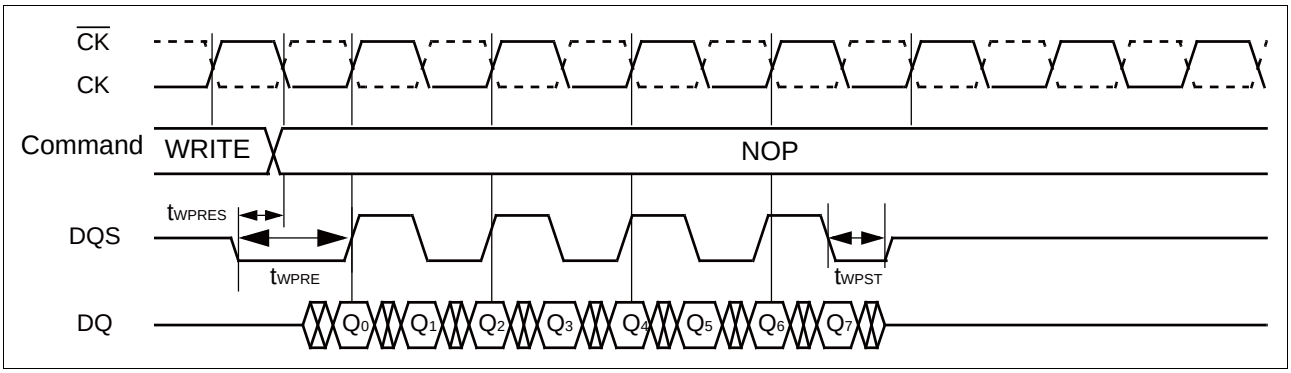
6. WRITE (WRIT)

WRIT initiates burst write operation to an active row address. Address inputs of A[7:0] determine starting column address and AP(A10) determines whether Auto Precharge is used or not. DQS input must be provided in order to latch the input data. DQS must be brought to Low to satisfy the specified time duration of the Write Preamble Setup Time to CK (t_{WPRES}). Input data window must be guaranteed with specified minimum setup and hold time against edge of DQS input (t_{DS}, t_{DH}). The input data appearing on DQ is written into memory cell array subject to the DM input logic level appearing coincident with the input data. If a given signal on DM is registered Low, the corresponding data will be written into the cell array. And if a given signal on DM is registered High, the corresponding data will be masked and write will not be executed to that byte. After data input with respect to BL is completed, DQS must be kept low for the specified minimum value of Write Postamble Time (t_{WPST}).

Data Input Timing



Write Preamble and Postamble



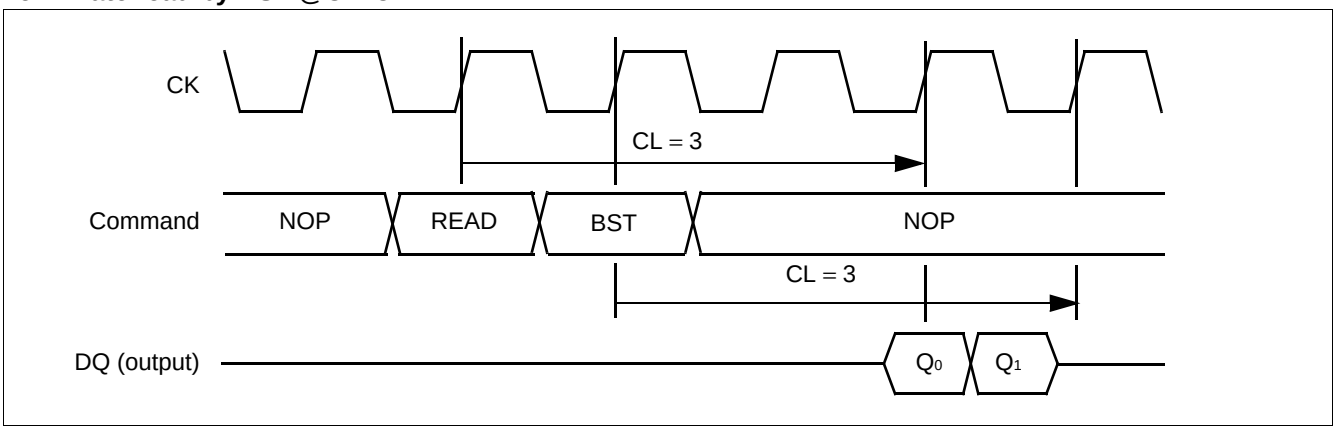
7. WRITE with Auto Precharge (WRITA)

WRITA commands can be issued by WRIT command with AP (A10) = H. Auto precharge is a feature which precharge the activated bank after the completion of burst write operation. The t_{RAS} is defined from between ACTIVE (ACT) command to the internal precharge which starts after 1+ BL/2 + t_{WR} from WRITA command. WRIT with Auto precharge operation should not be interrupted by subsequent READ, READA, WRIT, WRITA commands. Next ACTIVE (ACT) command can be issued after 1+ BL/2 + t_{DAL} after WRITA command.

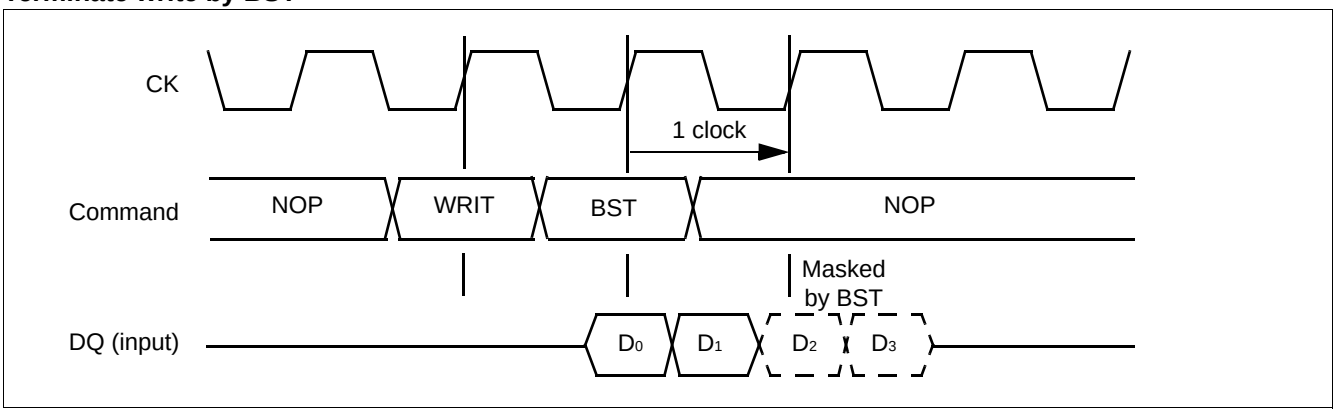
8. BURST TERMINATE (BST)

BST terminates the burst read or write operation. When a burst read is terminated by BST command, the data output will be in High-Z after CAS latency from the BST command. When a burst write is terminated by BST command, the data input after 1 clock from BST command will be masked.

Terminate read by BST @CL=3



Terminate write by BST



9. PRECHARGE SINGLE BANK (PRE)

PRECHARGE SINGLE BANK (PRE) command starts precharge operation for a bank selected by BA. A selected bank will be in IDLE state after specified time duration of t_{RP} from PRE command. A10 determines whether one or all banks are precharged. If AP(A10) = L, a bank to be selected by BA is precharged.

10. PRECHARGE ALL BANK (PALL)

PRECHARGE ALL BANKS (PALL) command starts precharge operation for all banks. All banks will be in IDLE state after specified time duration of t_{RP} from PALL command. A10 determines whether one or all banks are precharged. If AP(A10) = H, all banks are precharged and BA input is a “don't care”.

11. AUTO REFRESH (REF)

AUTO REFRESH (REF) command starts internal refresh operation which uses the internal refresh address counter. All banks must be precharged prior to the Auto-refresh command. Data retention capability depends on the Junction Temperature (Tj). Total 8,192 AUTO REFRESH (REF) commands must be asserted within the following refresh period of t_{REF}.

Tj Max (°C)	t_{REF} (ms)
+ 105	64
+ 125	16.7

12. SELF-REFRESH ENTRY (SELF)

SELF REFRESH ENTRY (SELF) commands can be issued by AUTO REFRESH (REF) command in conjunction with CKE = Low after last read data has been appeared on DQ. During Self Refresh mode, stored data can be retained without external clocking and all inputs except for CKE will be “don't care”. Self refresh mode can be used when Tj is less than + 85°C. Auto Refresh must be issued to retain data when Tj is greater than + 85 °C.

13. SELF-REFRESH EXIT (SELFX)

To exit self-refresh mode, apply minimum t_{IS} after CKE brought High, and then the NO OPERATION command (NOP) or the DESELECT command (DESL) should be asserted within one t_{REFC} period. CKE should be held High within one t_{REFC} period after t_{IS}. Refer to the “(15) Self Refresh Entry and Exit” in “■TIMING DIAGRAMS” for the detail. It is recommended to assert an Auto-refresh command just after the t_{REFC} period to avoid the violation of refresh period.

14. MODE REGISTER SET (MRS)

MODE REGISTER SET (MRS) commands to program the mode registers. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command. MRS command should only be issued on conditions that all DQs are in High-Z and all banks are in IDLE state. The contents of the mode registers is undefined after the power-up and Deep Power Down Exit. Therefore MRS must be issued to set each content of mode registers after initialization. Refer to the “Power Up Initialization” in “ ■FUNCTIONAL DESCRIPTION”.

15. POWER DOWN ENTRY (PD)

POWER DOWN ENTRY (PD) commands to drive the device in Power Down mode and maintains low power state as long as CKE is kept Low. During Power Down state, all inputs signals are “don't care” except for CKE. Power Down mode must be entered on condition that all DQs are in High-Z.

16. POWER DOWN EXIT (PDX)

POWER DOWN EXIT (PDX) commands to resume the device from Power Down mode. Any commands can be detected 1 clock after PDX commands.

17. DEEP POWER DOWN ENTRY (DPD)

DEEP POWER DOWN ENTRY (DPD) commands to drive the device in Deep Power Down mode which is the lowest power consumption but all stored data and the contents of mode registers will be lost. During Deep Power Down state, all inputs signals except for CKE are “don't care” and all DQs and DQS will be in High-Z. Deep Power Down mode must be entered on conditions that all DQs are in High-Z and all banks are in IDLE state.

18. DEEP POWER DOWN EXIT (DPDX)

DEEP POWER DOWN EXIT (DPDX) commands to resume the device from Deep Power Down mode. Power up initialization procedure must be performed after DPDX commands. Refer to the “Power Up Initialization” in “■ FUNCTIONAL DESCRIPTION”.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage *	V_{DD},V_{DDQ}	-0.5 to +2.3	V
Input / Output Voltage *	V_{IN}, V_{OUT}	-0.5 to +2.3	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-55 to +125	°C

*: All voltages are referenced to V_{SS}.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage*1	V_{DD}, V_{DDQ}	1.7	1.8	1.9	V
	V_{SS}, V_{SSQ}	0	0	0	V
DC Input High Voltage*2	$V_{IH\ (DC)}$	$V_{DDQ} \times 0.7$	—	V_{DDQ} + 0.3	V
AC Input High Voltage*2	$V_{IH\ (AC)}$	$V_{DDQ} \times 0.8$	—	V_{DDQ} + 0.3	V
DC Input Low Voltage*3	$V_{IL\ (DC)}$	-0.3	—	$V_{DDQ} \times 0.3$	V
AC Input Low Voltage*3	$V_{IL\ (AC)}$	-0.3	—	$V_{DDQ} \times 0.2$	V
Junction Temperature	T_j	-10	—	+125	°C

*1: V_{DDQ} must be less than or equal to V_{DD}.

*2: Maximum DC voltage on input or I/O pins is V_{DDQ} + 0.3 V. During voltage transitions, inputs may positive overshoot to V_{DDQ} + 1.0V for periods of up to 3 ns.

*3: Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, inputs may negative overshoot to V_{SSQ} - 1.0V for periods of up to 3 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ CAPACITANCE

(T_a = + 25 °C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance, Except for DM	C_{IN1}	1	—	2.5	pF
Input Capacitance for DM	C_{IN2}	2	—	4	pF
I/O Capacitance	$C_{I/O}$	2	—	4	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Condition		Value		Unit
				Min.	Max.	
Output High Voltage	$V_{OH(DC)}$	I_{OH} = -0.1 mA		V_{DDQ} – 0.2	—	V
Output Low Voltage	$V_{OL(DC)}$	I_{OL} = 0.1 mA		—	0.2	V
Input Leakage Current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DDQ}, All other pins not under test = 0 V		– 5	5	µA
Output Leakage Current	I_{LO}	0 V ≤ V_{IN} ≤ V_{DDQ}, Data out disabled		– 5	5	µA
Operating One Bank Active-Precharge Current	I_{DD0}	t_{RC} = t_{RC} min, t_{CK} = t_{CK} min, CKE = V_{IH}, $\overline{CS}$ = V_{IH} addresses inputs are SWITCHING; data bus inputs are STABLE	Tj ≤ + 105 °C	—	65	mA
			Tj ≤ + 125 °C	—	75	
Precharge Standby Current	I_{DD2P}	All banks idle, CKE = V_{IL}, $\overline{CS}$ = V_{IH}, t_{CK} = t_{CK} min, address and control inputs are SWITCHING; data bus inputs are STABLE	Tj ≤ + 105 °C	—	6	mA
			Tj ≤ + 125 °C	—	9	
	I_{DD2N}	All banks idle, CKE = V_{IH}, $\overline{CS}$ = V_{IH}, t_{CK} = t_{CK} min, address and control inputs are SWITCHING; data bus inputs are STABLE	Tj ≤ + 105 °C	—	15	mA
			Tj ≤ + 125 °C	—	20	
Operating Burst Read Current	I_{DD4R}	One bank active, BL = 4, t_{CK} = t_{CK} min, Output pin open, Gapless data, address inputs are SWITCHING; 50% data change each burst transfer		—	300	mA
Operating Burst Write Current	I_{DD4W}	One bank active, BL = 4, t_{CK} = t_{CK} min, Gapless data, address inputs are SWITCHING; 50% data change each burst transfer		—	380	mA
Auto Refresh Current	I_{DD5}	t_{RC} = t_{RFC} min, t_{CK} = t_{CK} min, CKE = V_{IH}, address and control inputs are SWITCHING; data bus inputs are STABLE		—	120	mA

(Continued)

(Continued)

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Self Refresh Current	I_{DD6}	CKE = V_{IL}, $\overline{CS}$ = V_{IL}, address and control inputs are STABLE; data bus inputs are STABLE	—	6	mA
Deep Power Down Current	I_{DD8}	address and control inputs are STABLE; data bus inputs are STABLE	—	300	µA

Notes: • All voltages are referenced to V_{SS}.

- After power on, initialization following power-up timing is required. DC characteristics are guaranteed after the initialization.
- I_{DD} depends on the output termination or load condition, clock cycle rate, signal clocking rate. The specified values are obtained with the output open condition.

2. AC Characteristics

(Under recommended operating conditions unless otherwise noted)*1, *2

Parameter			Symbol	Value		Unit
				Min.	Max.	
DQ Output Access Time from CK/$\overline{CK}$ (t_{CK} = t_{CK} min)*3, *4, *7			t_{AC}	2	6	ns
DQS Output Access Time from CK/$\overline{CK}$ *3, *4			t_{DQSCK}	2	6	ns
Clock High Level Width *3			t_{CH}	2	—	ns
Clock Low Level Width *3			t_{CL}	2	—	ns
Delay between CK and $\overline{CK}$ *4			t_{DC}	0.45	0.55	t_{CK}
Clock Cycle Time	CL = 2		t_{CK}	15	—	ns
	CL = 3			7.4		
	CL = 4	Tj ≤ + 105 °C		4.6		
		Tj ≤ + 125 °C		5		
DQ and DM Input Setup Time *3		Tj ≤ + 105 °C	t_{DS}	0.4	—	ns
		Tj ≤ + 125 °C		0.5		
DQ and DM Input Hold Time *3		Tj ≤ + 105 °C	t_{DH}	0.4	—	ns
		Tj ≤ + 125 °C		0.5		
DQ and DM Input Pulse Width			t_{DIPW}	0.35	—	t_{CK}
Address and Control Input Setup Time *3			t_{IS}	0.9	—	ns
Address and Control Input Hold Time *3			t_{IH}	0.9	—	ns
Address and Control Input Pulse Width			t_{IPW}	0.6	—	t_{CK}
DQ Low-Z Time from CK/$\overline{CK}$ *3, *5			t_{LZ}	0	—	ns
DQ High-Z Time from CK/$\overline{CK}$ *3, *5, *6			t_{HZ}	—	6	ns
DQS to DQ Skew *4			t_{DQSQ}	—	0.4	ns
DQ Output Hold Time from DQS *3, *4			t_{QH}	t_{DC} – 0.5	—	ns
WRIT Command to 1st DQS Latching Transition			t_{DQSS}	0.75	1.25	t_{CK}
DQS Input High Level Width			t_{DQSH}	0.35	—	t_{CK}
DQS Input Low Level Width			t_{DQSL}	0.35	—	t_{CK}
DQS Falling Edge to CK Setup Time			t_{DSS}	0.2	—	t_{CK}
DQS Falling Edge Hold Time from CK			t_{DSH}	0.2	—	t_{CK}
MRS Command Period			t_{MRD}	2	—	t_{CK}
Write Preamble Setup Time			t_{WPRES}	0	—	ns
Write Preamble Time			t_{WPRE}	0.25	—	t_{CK}
Write Postamble Time			t_{WPST}	0.4	0.6	t_{CK}
Read Preamble Time		CL = 2	t_{RPRE}	0.5	1.1	t_{CK}
		CL = 3, 4		0.9	1.1	
Read Postamble Time			t_{RPST}	0.4	0.6	t_{CK}

(Continued)

(Continued)

(Under recommended operating conditions unless otherwise noted)*1, *2

Parameter		Symbol	Value		Unit
			Min.	Max.	
ACT to PRE, PALL Command Period *7		t_{RAS}	37	8000	ns
ACT to ACT Command Period (Same Bank) *7		t_{RC}	59.2	—	ns
REF to ACT, REF Command Period		t_{REFC}	100	—	ns
ACT to READ or WRIT Command Period		t_{RCD}	20	—	ns
Precharge Period *7		t_{RP}	18	—	ns
ACT to ACT Command Period (Other Bank)		t_{RRD}	9.2	—	ns
Write Recovery Time		t_{WR}	12	—	ns
Data Input to ACT, REF Command Period	CL = 2	t_{DAL}	1 CLK + t_{RP}	—	ns
	CL = 3		2 CLK + t_{RP}		
	CL = 4		3 CLK + t_{RP}		
Internal Write to READ Command Period		t_{WTR}	9.2	—	ns
Average Refresh Period *8	Tj ≤ + 105°C	t_{REFI}	—	7.8	µs
	Tj ≤ + 125°C			2.0	
Average Periodic Refresh Interval	Tj ≤ + 105°C	t_{REF}	—	64	ms
	Tj ≤ + 125°C			16.7	
Transition Time *9		t_T	—	1	ns

* 1: AC characteristics are measured after the Power up initialization procedure.

* 2: $V_{DD} \times 0.5$ is the reference level for 1.8 V I/O for measuring timing of input/output signals.

* 3: If input signal transition time (t_T) is longer than 1 ns; [(t_T/2) − 0.5] ns should be added to t_{AC} (Max), t_{DQSCK} (Max) and t_{HZ} (max) spec values, [(t_T/2) − 0.5] ns should be subtracted from t_{LZ} (Min) and t_{QH} (Min) spec values, and (t_T - 1.0) ns should be added to t_{CH} (Min), t_{CL} (Min), t_{IS} (Min), t_{IH} (Min), t_{DS} (Min) and t_{DH} (Min) spec values.

* 4: The data valid window is defined as t_{QH} - t_{DQSQ}. The data valid window depends on t_{DC} which is defined between rising edge of CK and rising edge of $\overline{CK}$. The data valid window is guaranteed when t_{DC} is satisfied.

* 5: t_{AC}, t_{DQSCK}, t_{LZ} and t_{HZ}, are measured under output load circuit shown in " 3. Measurement Condition of AC Characteristics" in " ■ ELECRTRICAL CHARACTERISTICS" and Driver Strength (DS) = Normal, Pre Driver Strength (PDS) = Fast are assumed.

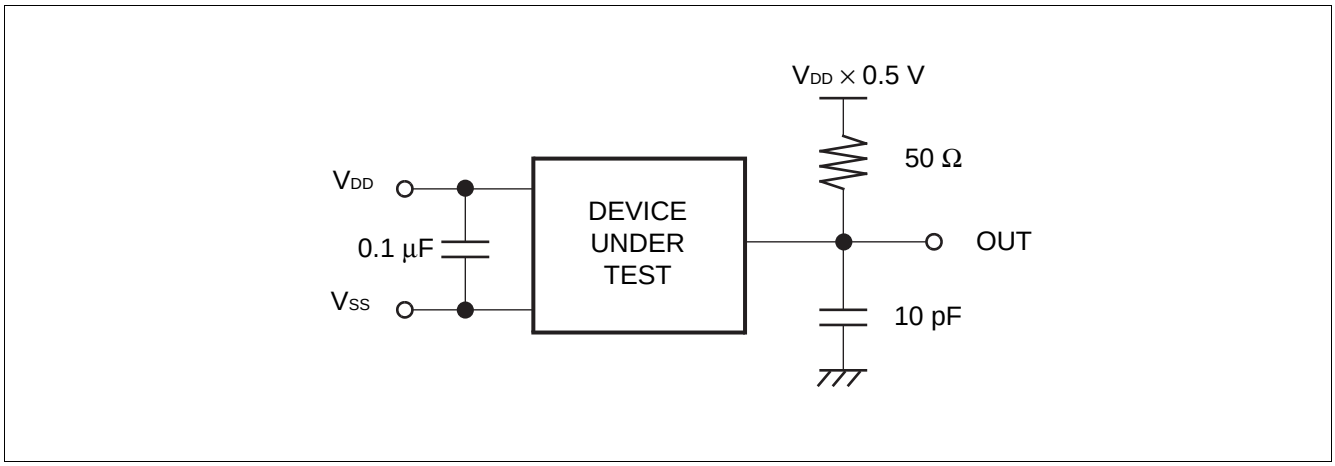
* 6: Specified where output buffer is no longer driven.

* 7: The sum of actual clock count of t_{RAS} and t_{RP} must be equal or greater than specified minimum t_{RC}.

* 8: This value is for reference only.

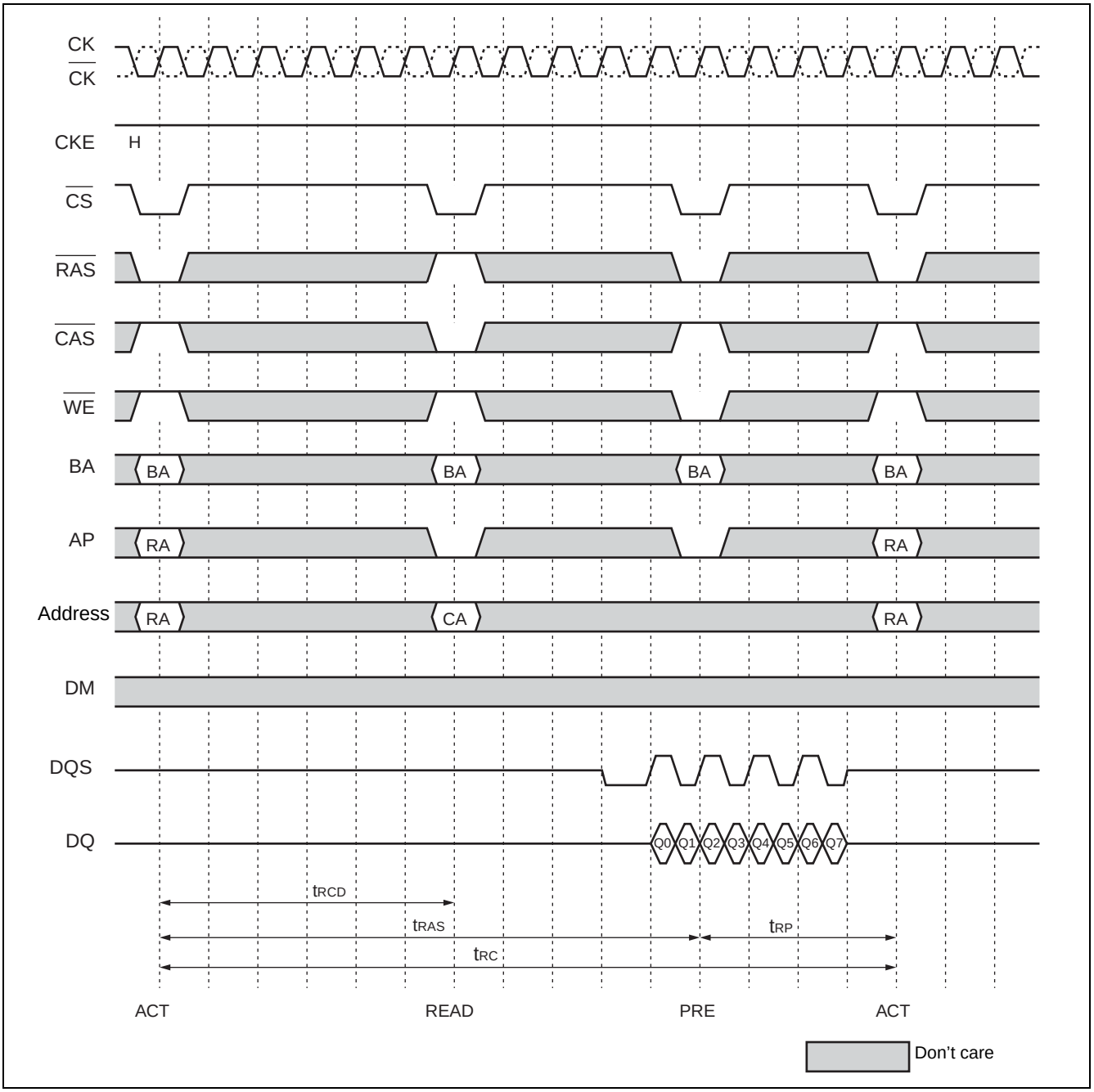
* 9: Transition times are measured between V_{IH} (AC) min and V_{IL} (AC) max.

3. Measurement Condition of AC Characteristics



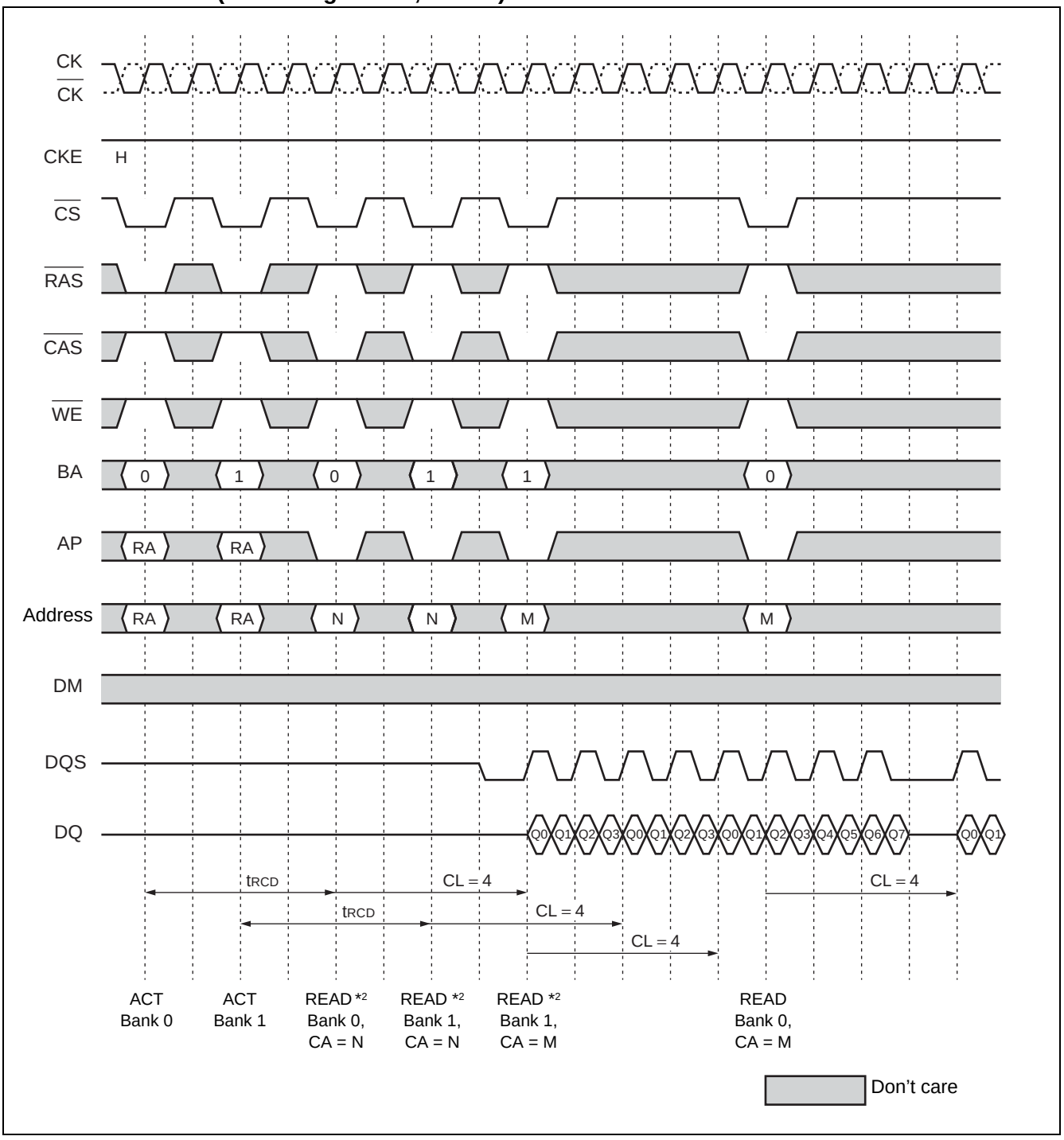
■ TIMING DIAGRAMS

1. Read* (Assuming CL = 4, BL = 8)



* : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

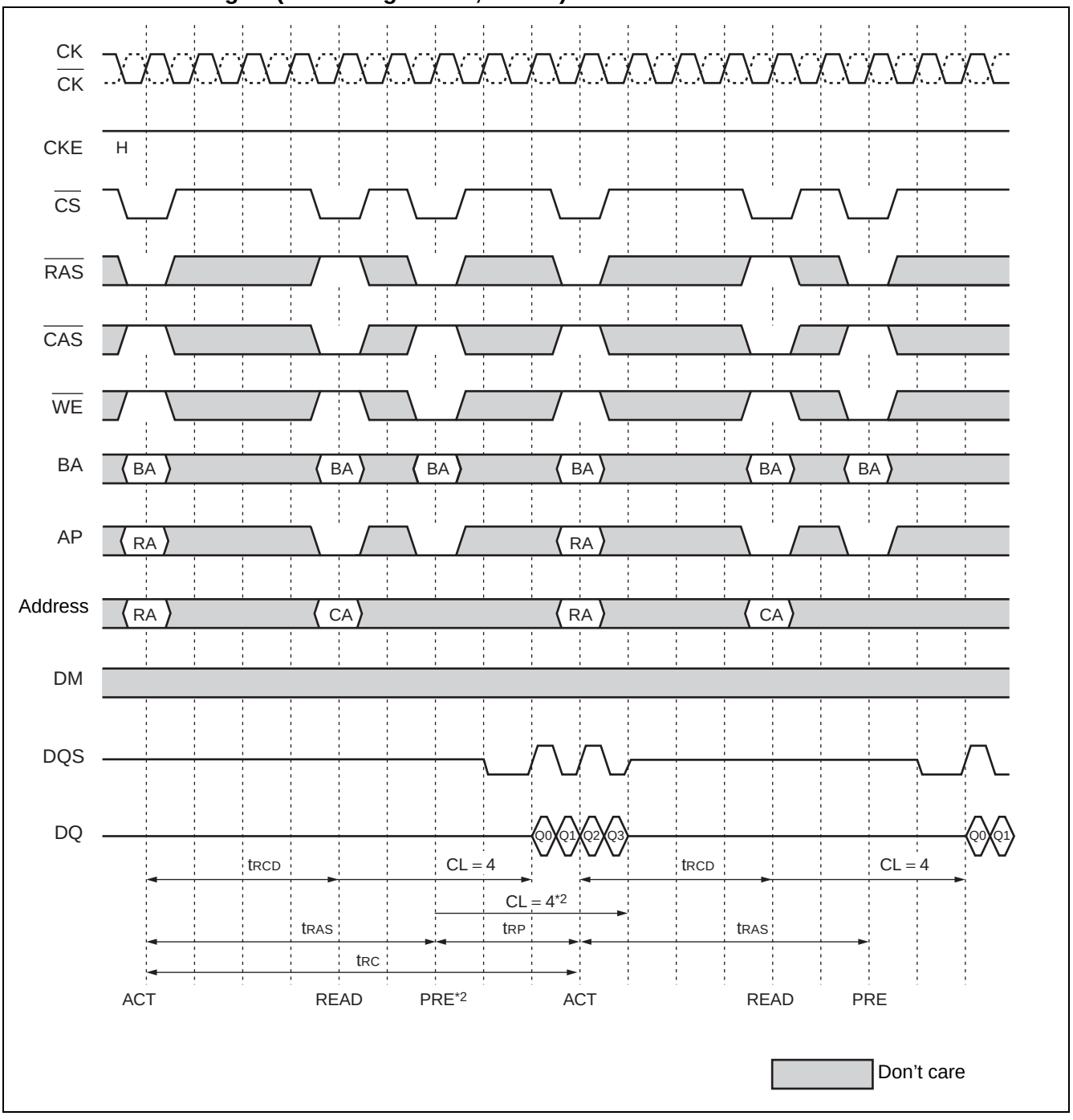
2. Read to Read*1 (Assuming CL = 4, BL = 8)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Previous burst read can be interrupted by subsequent burst read.

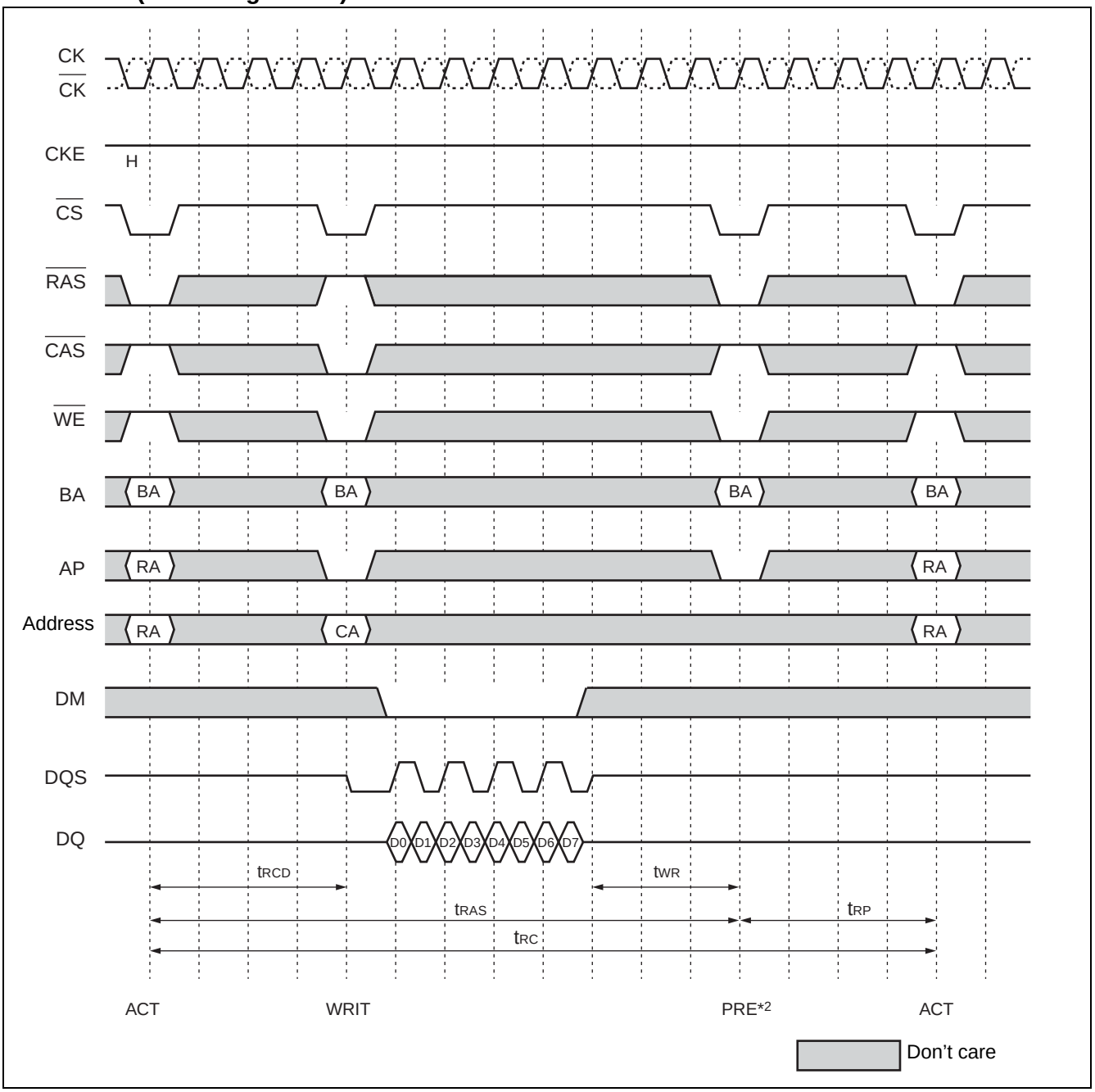
3. Read to Precharge *1(Assuming CL = 4, BL = 8)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Burst read operation can be terminated by PRE command. All DQ pins become High-Z after CL from PRE command.

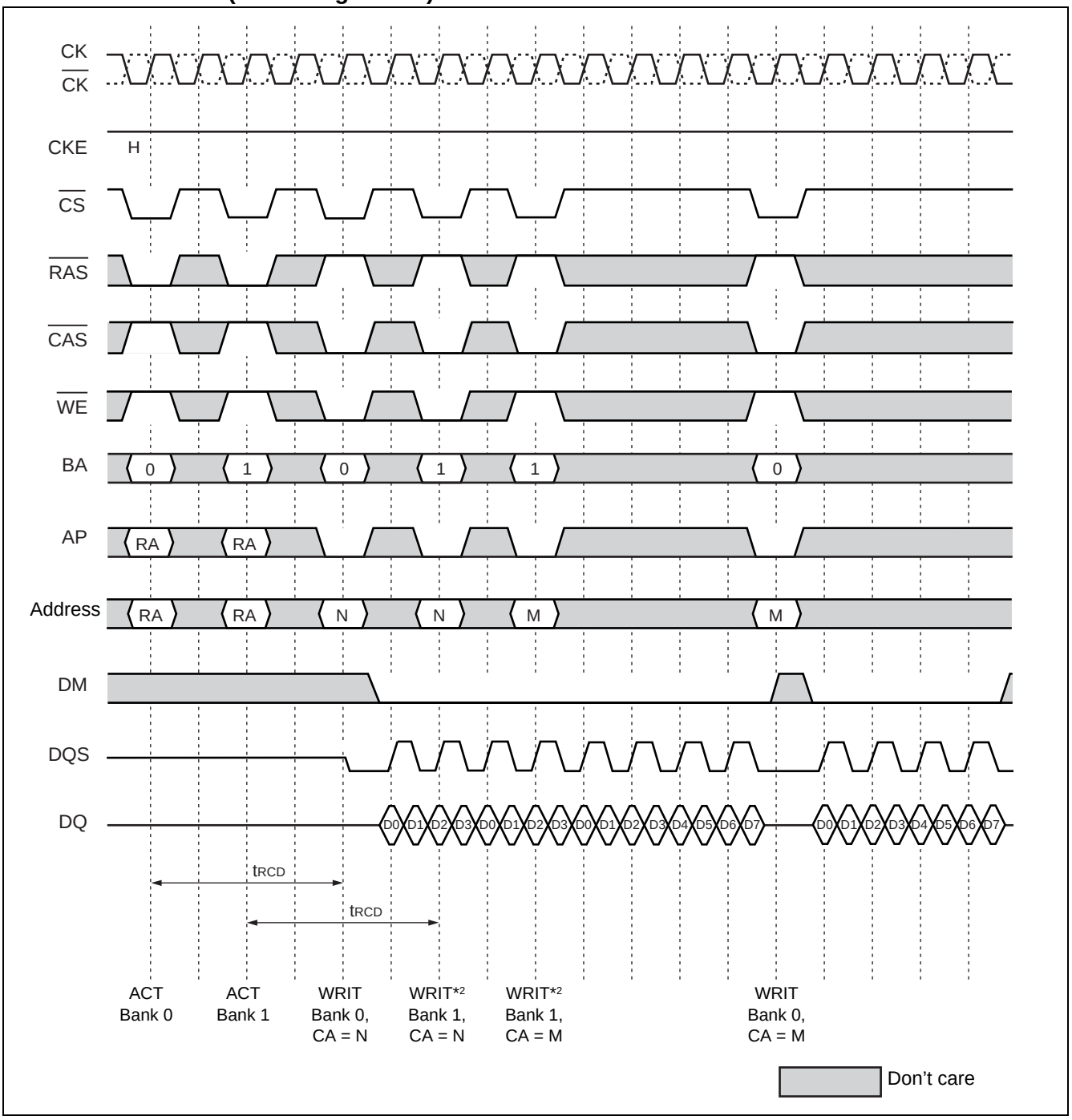
5. Write *1 (Assuming BL = 8)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Burst write operation should not be terminated by PRE command. PRE can be issued after 1 + BL/2 + t_{WR} from WRIT command.

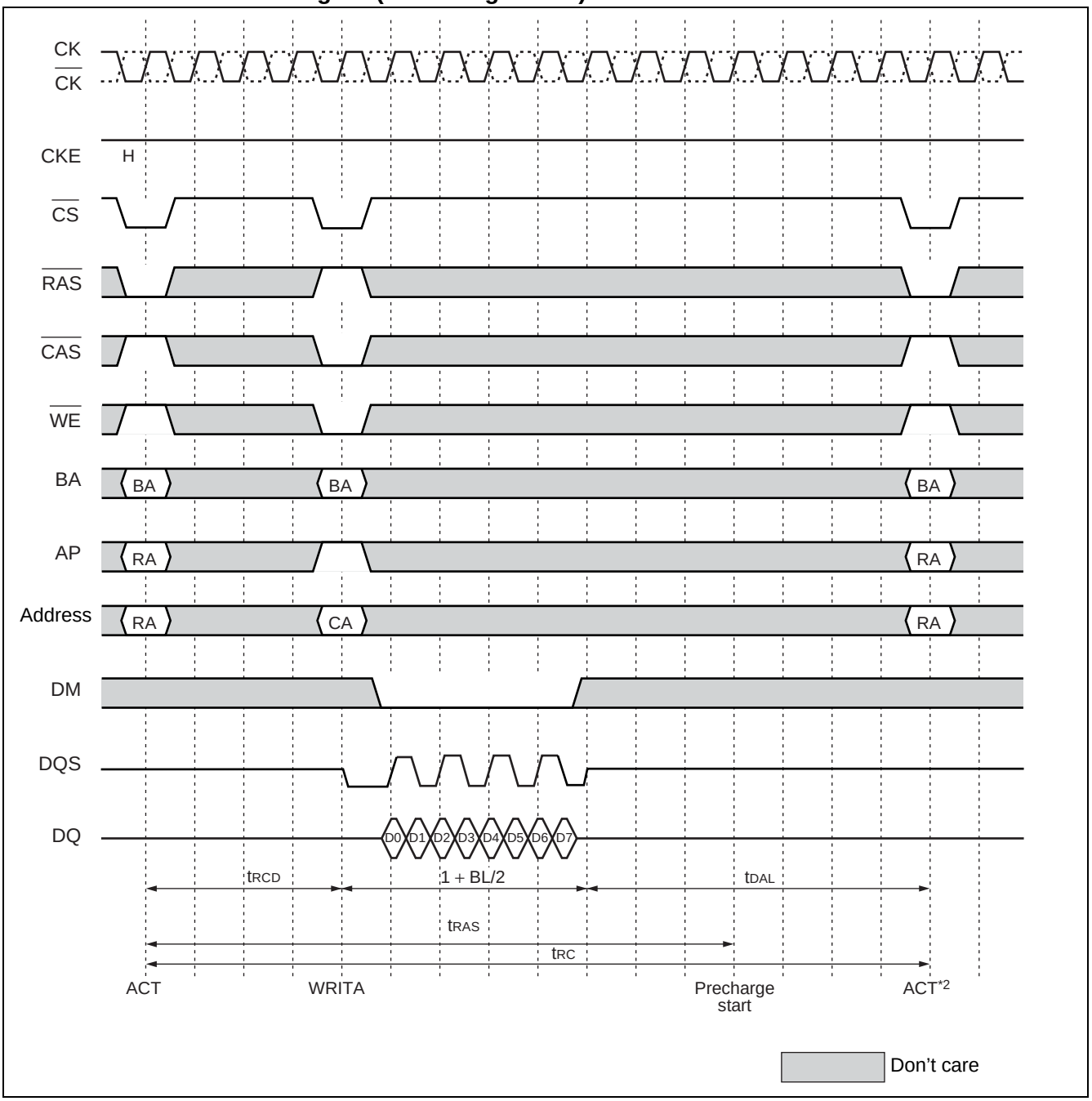
6. Write to Write *1 (Assuming BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : Previous burst write can be interrupted by subsequent burst write.

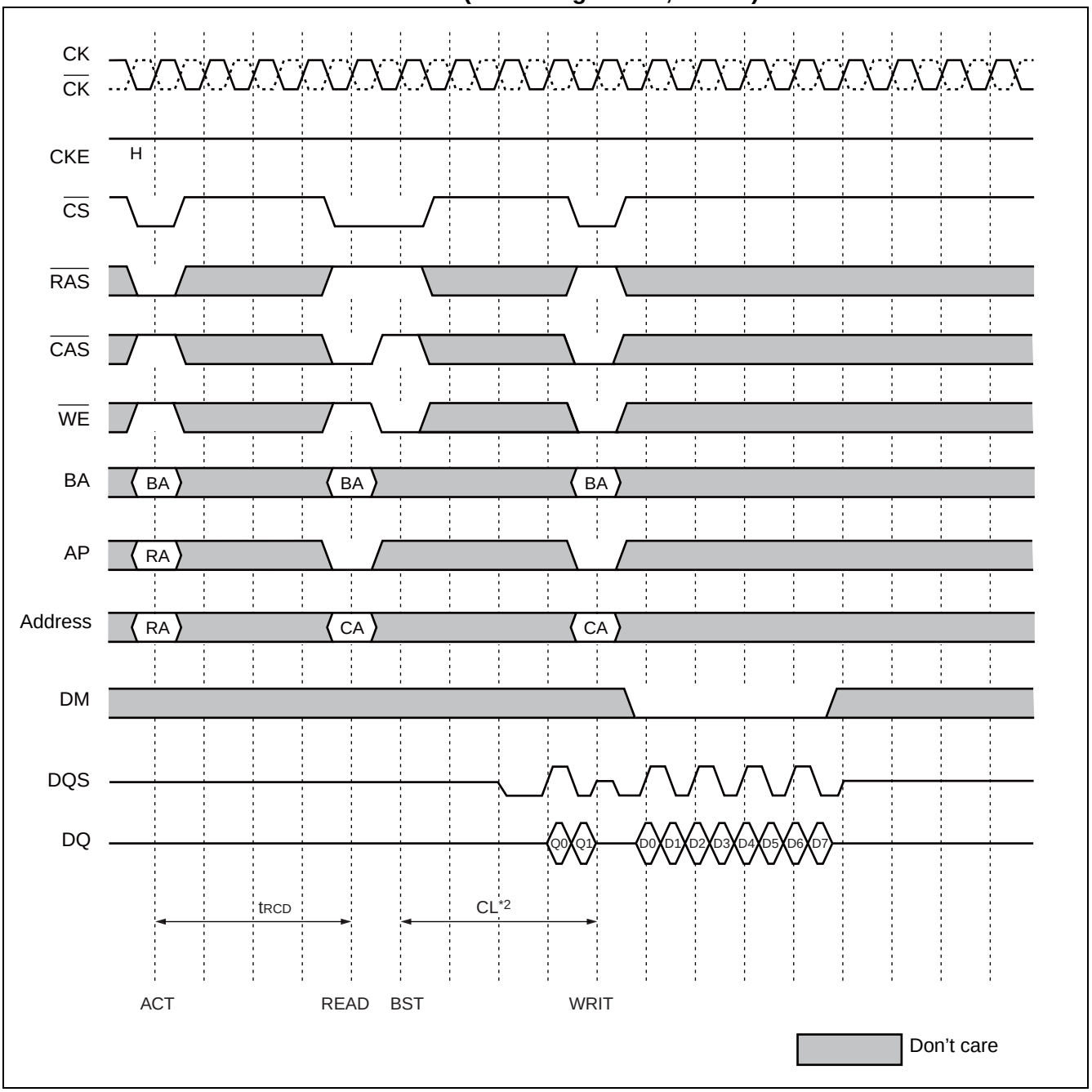
7. Write with Auto-Precharge *1 (Assuming BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : Next ACT command can be issued after 1 + BL/2 + t_{DAL} (Min) from WRITA command. t_{RC} must be satisfied.

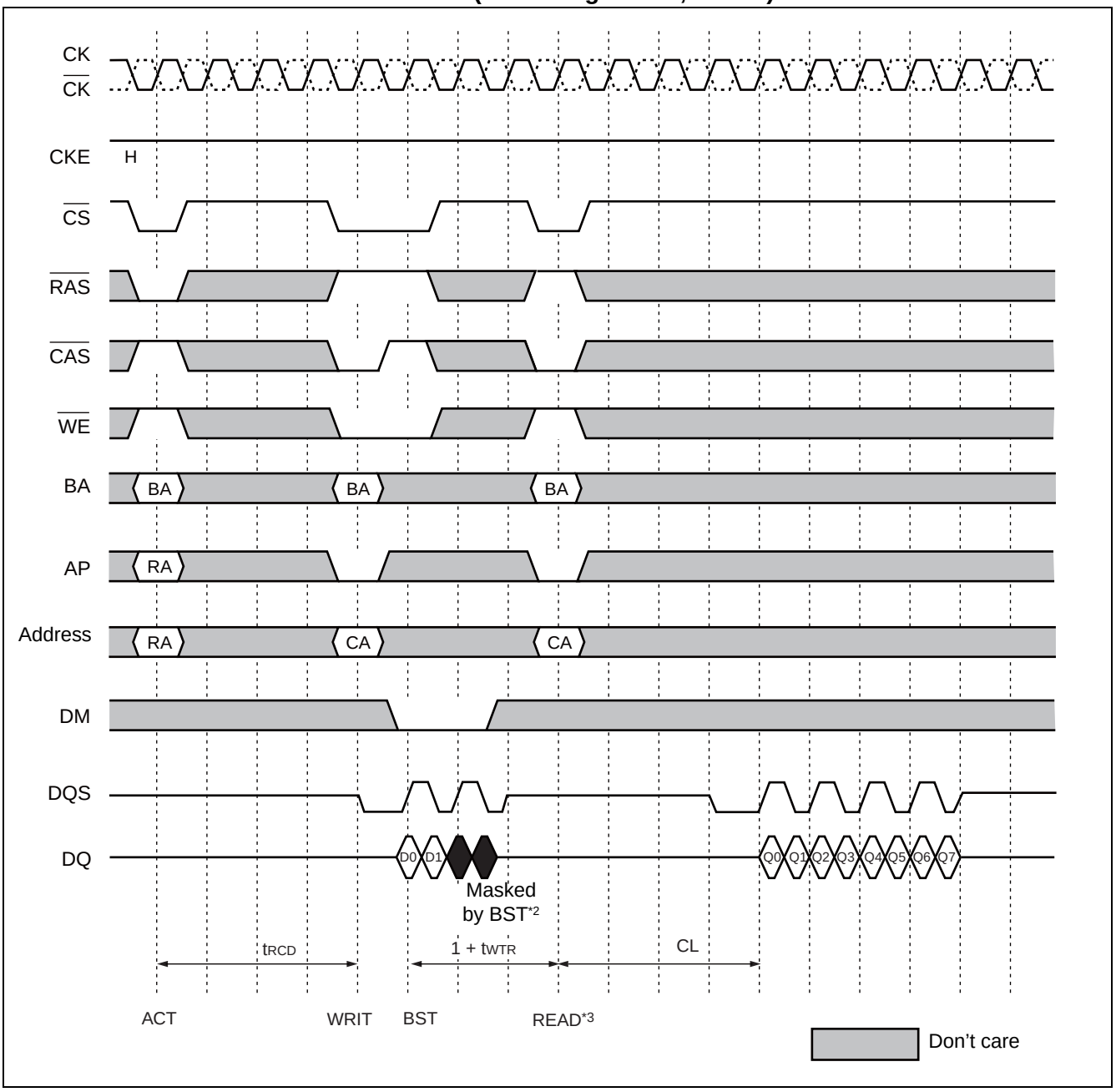
9. Read to Write with BST Command *1 (Assuming CL = 4, BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : WRIT command can be issued after CL from burst read termination by BST command.

11. Write to Read with BST Command *1 (Assuming CL = 4, BL = 8)

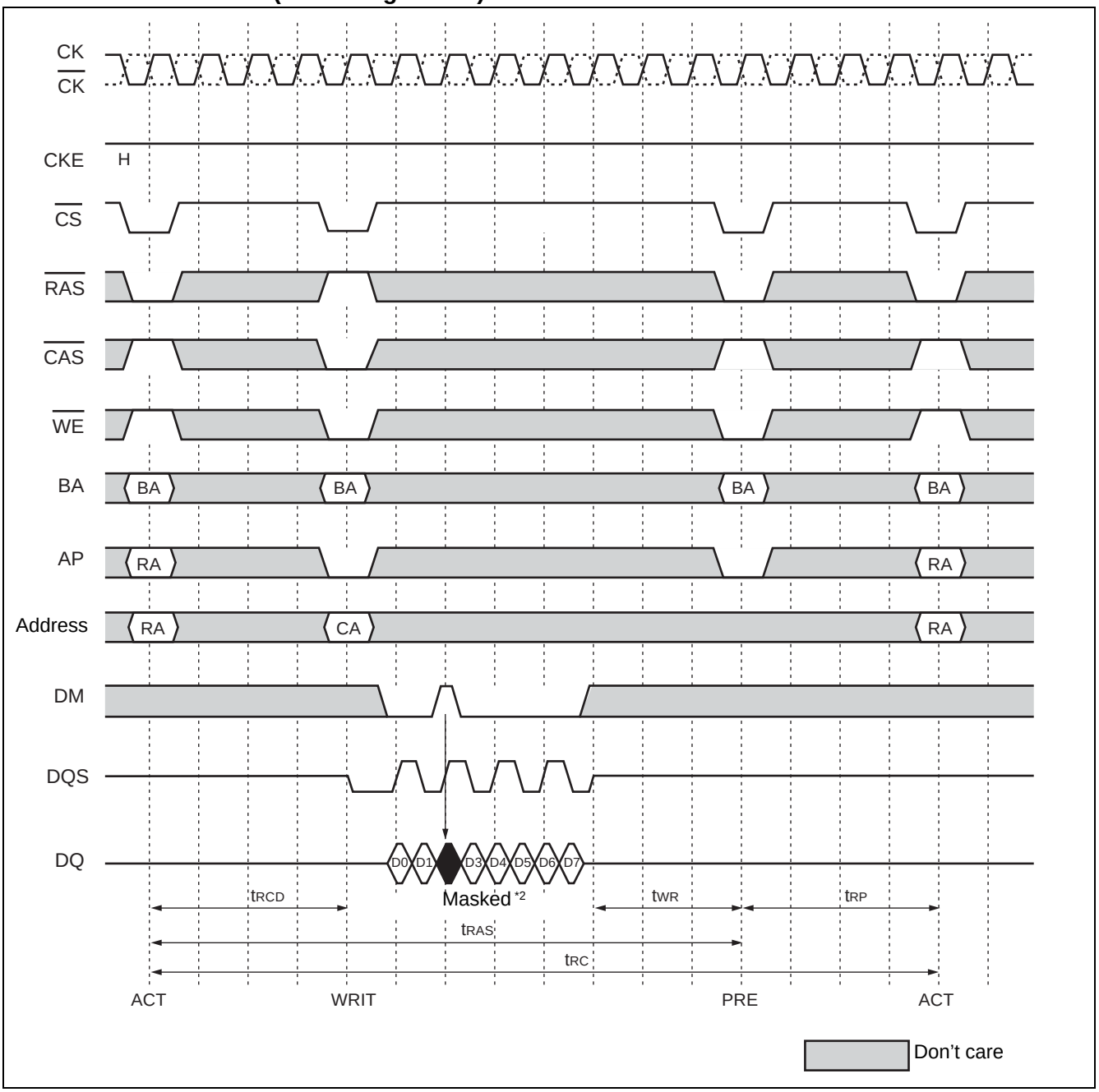


*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : The data input after 1 clock from BST command will be masked.

*3 : READ command can be issued after 1 + t_{WTR} from burst write termination by BST command.

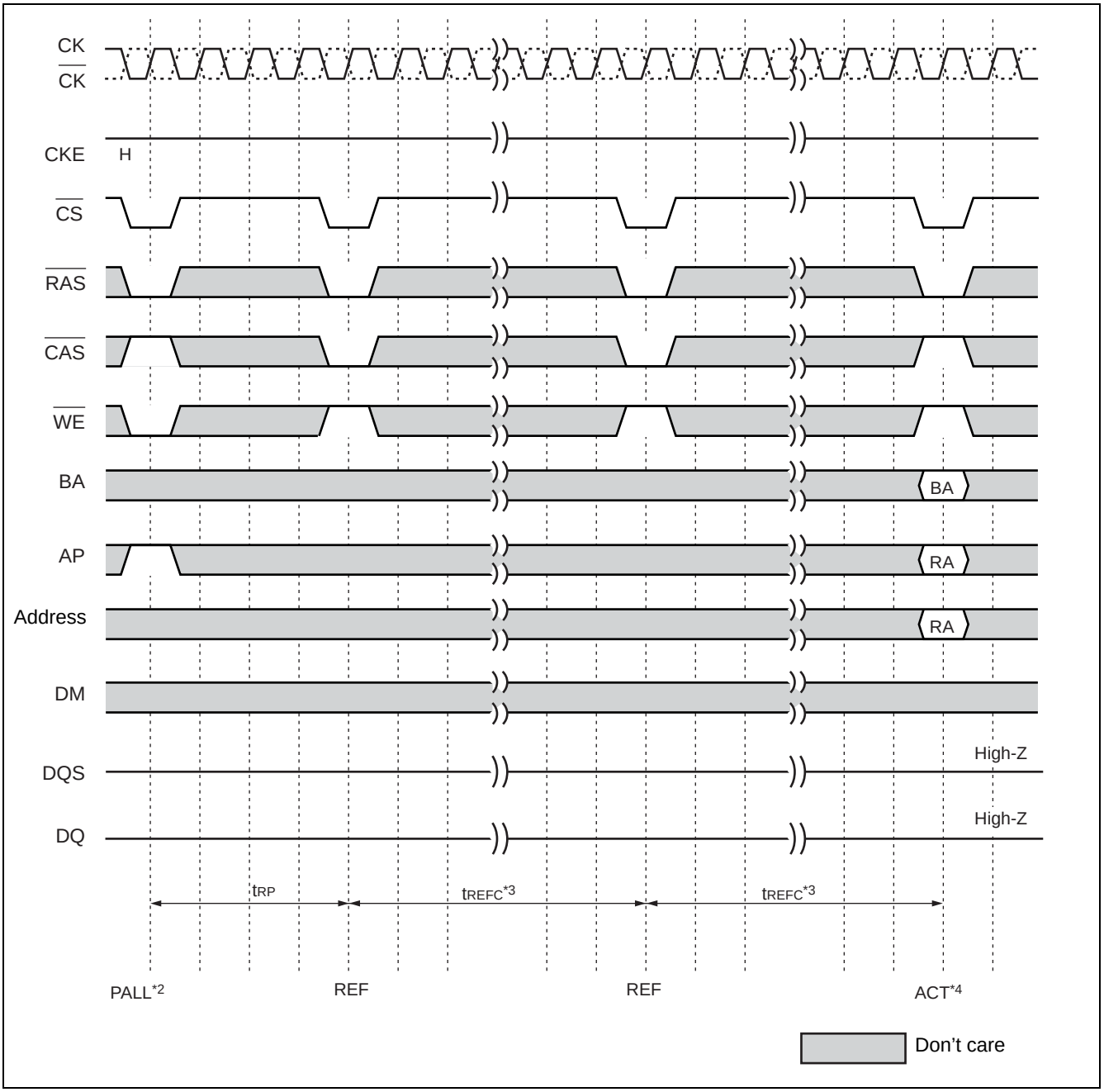
13. DM Control Write *1 (Assuming BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : When DM is registered High, the corresponding data will be masked.

14. Auto Refresh *1



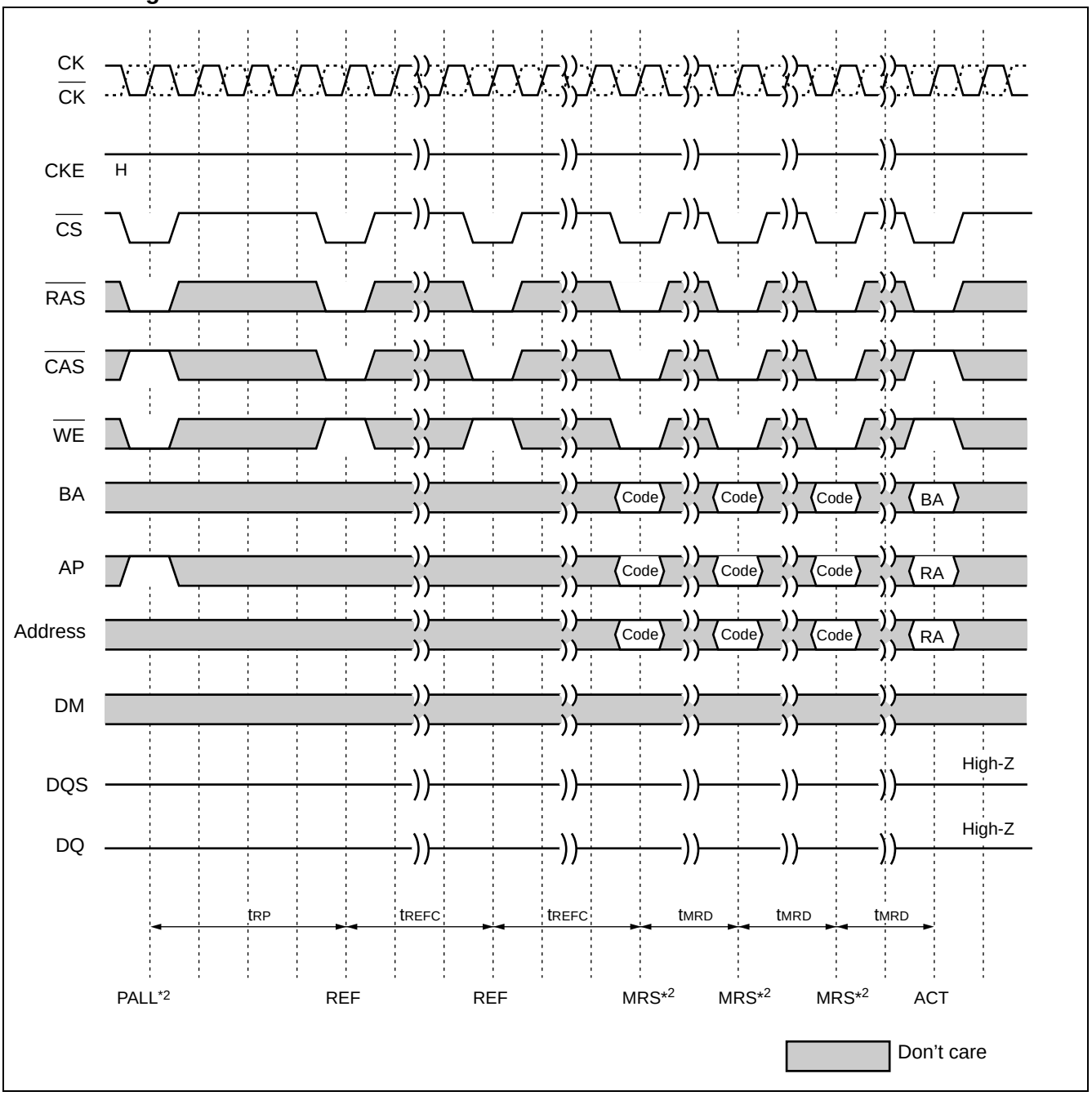
*1 : RA = Row Address, BA = Bank Address, AP = Auto Precharge

*2 : All banks must be precharged prior to the AUTO REFRESH command (REF).

*3 : Either NOP or DESL command should be asserted during t_{REFC} period.

*4 : ACT or MRS or REF command should be asserted after t_{REFC} from REF command.

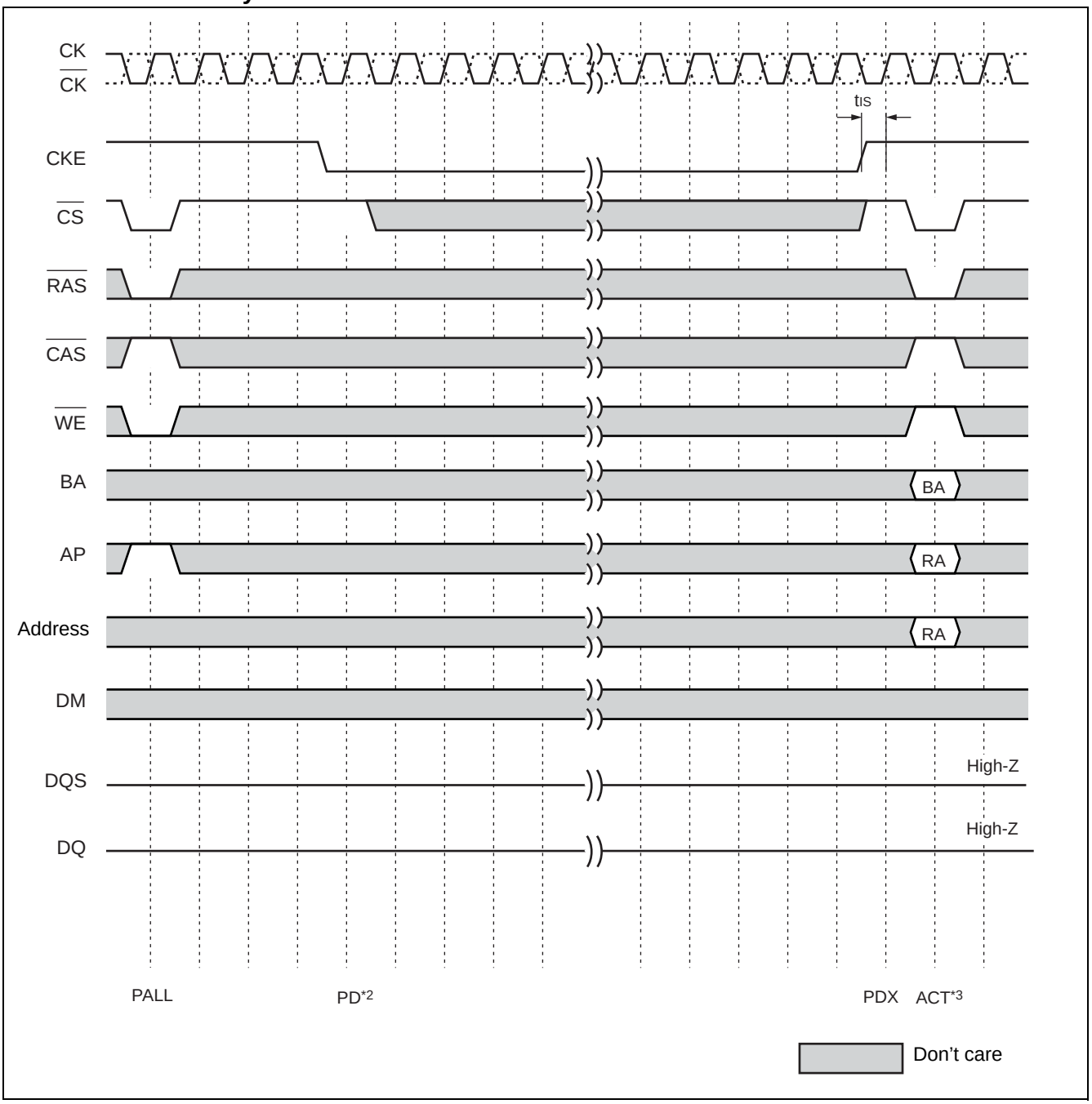
16. Mode Register Set*1



*1 : RA = Row Address, BA = Bank Address, AP = Auto Precharge

*2 : MODE REGISTER SET (MRS) command must be asserted after all banks have been precharged and all DQ are in High-Z.

17. Power Down Entry and Exit *1

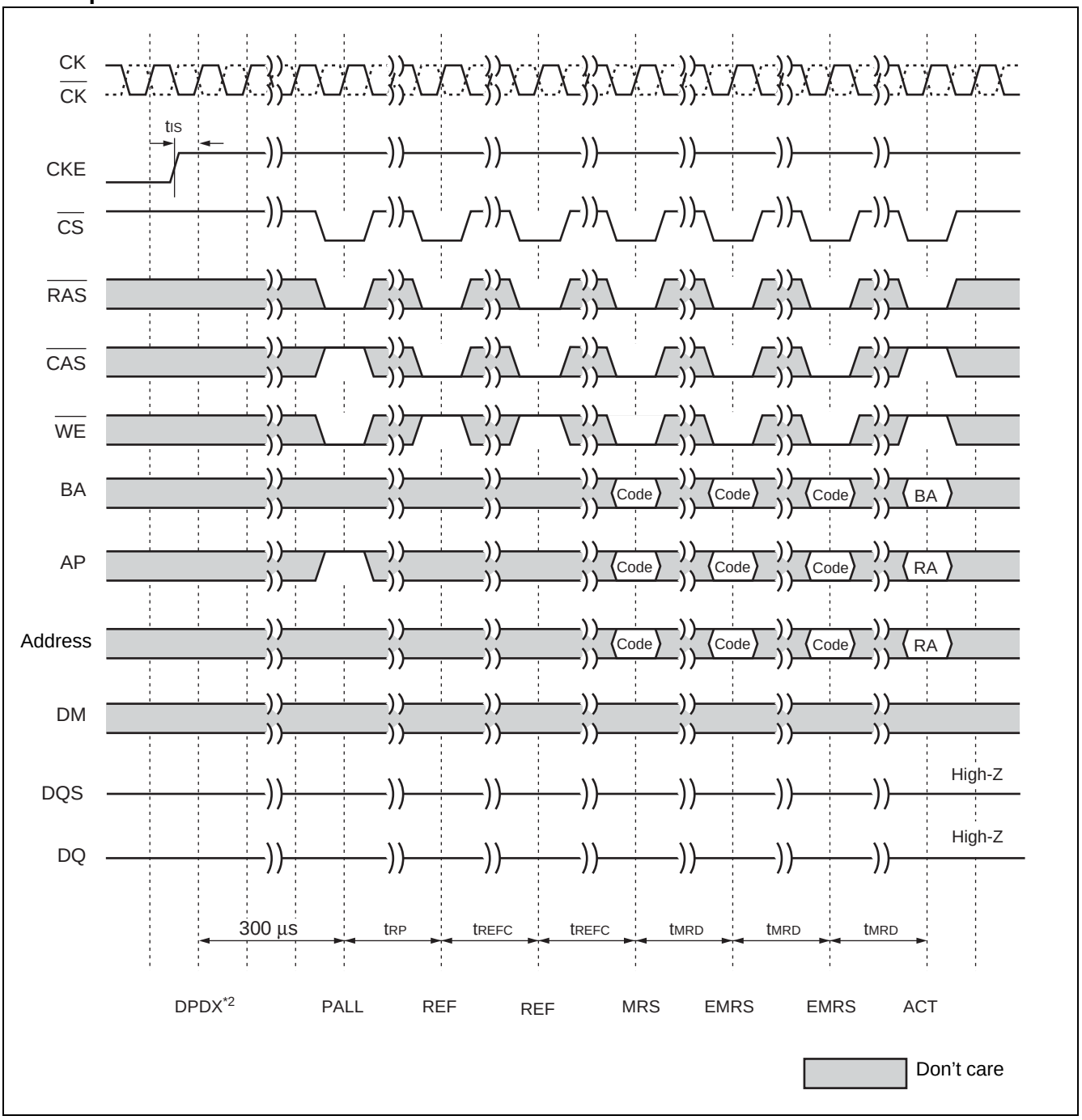


*1 : RA = Row Address, BA = Bank Address, AP = Auto Precharge

*2 : PD command can be issued after all DQ are in High-Z.

*3 : ACT command can be issued after 1 clock from POWER DOWN EXIT (PDX) command.

19. Deep Power Down Exit *1



*1: RA = Row Address, BA = Bank Address, AP = Auto Precharge

*2: Power up initialization procedure must be performed after DPDX command.